FSA Suppliers Expo & TECHNICAL CONFERENCE

Design Modeling Workshop

"60nm and 90nm Interconnect Modeling Challenges"

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OEA International, Inc.

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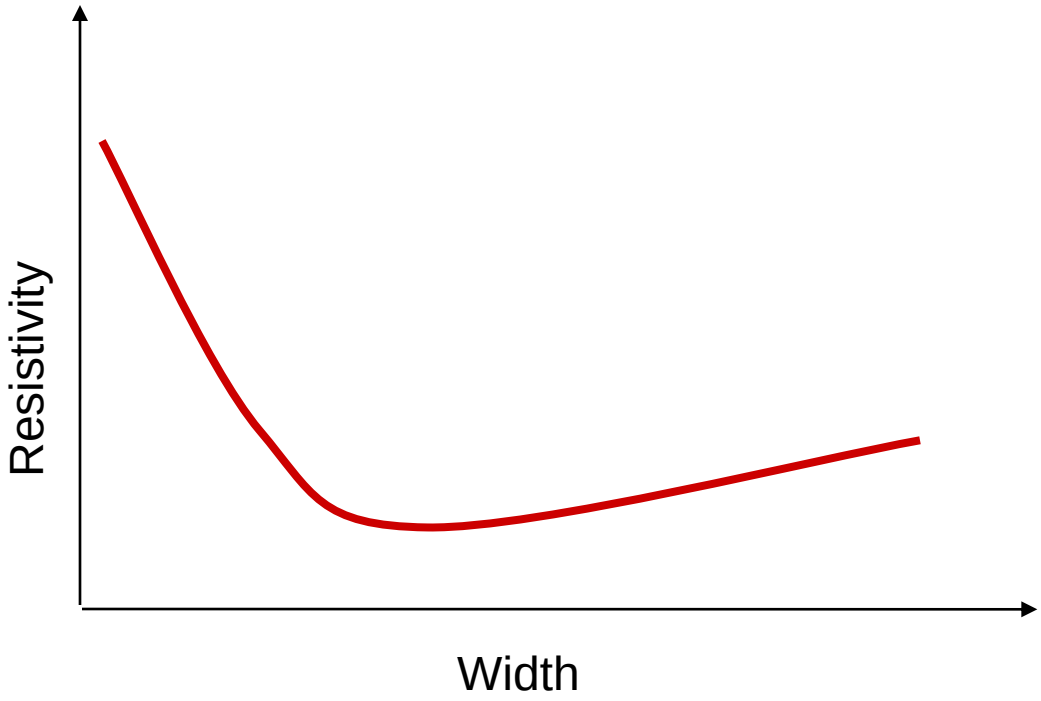
  - Louie Nguyen
  - Edmund Soo
  - Jerry Tallinger
  - Alla Toy

Agenda

- Section 1 - DSM Effects on RF Modeling
  - Simple versus Complex Modeling Issues
  - Dummy Metal and Slotting Effects - Spiral Inductor Example
- Section 2 - DSM Modeling on Interconnects
  - Dummy Metal Effects on Delay and Cross-talk for Long Interconnects
- Section 3 - Power Delivery Inductance effects on Large Digital IC performance
  - Solving RCLK models for VDD and VSS network combined
  - Determining the size and placement of on-chip decoupling capacitances

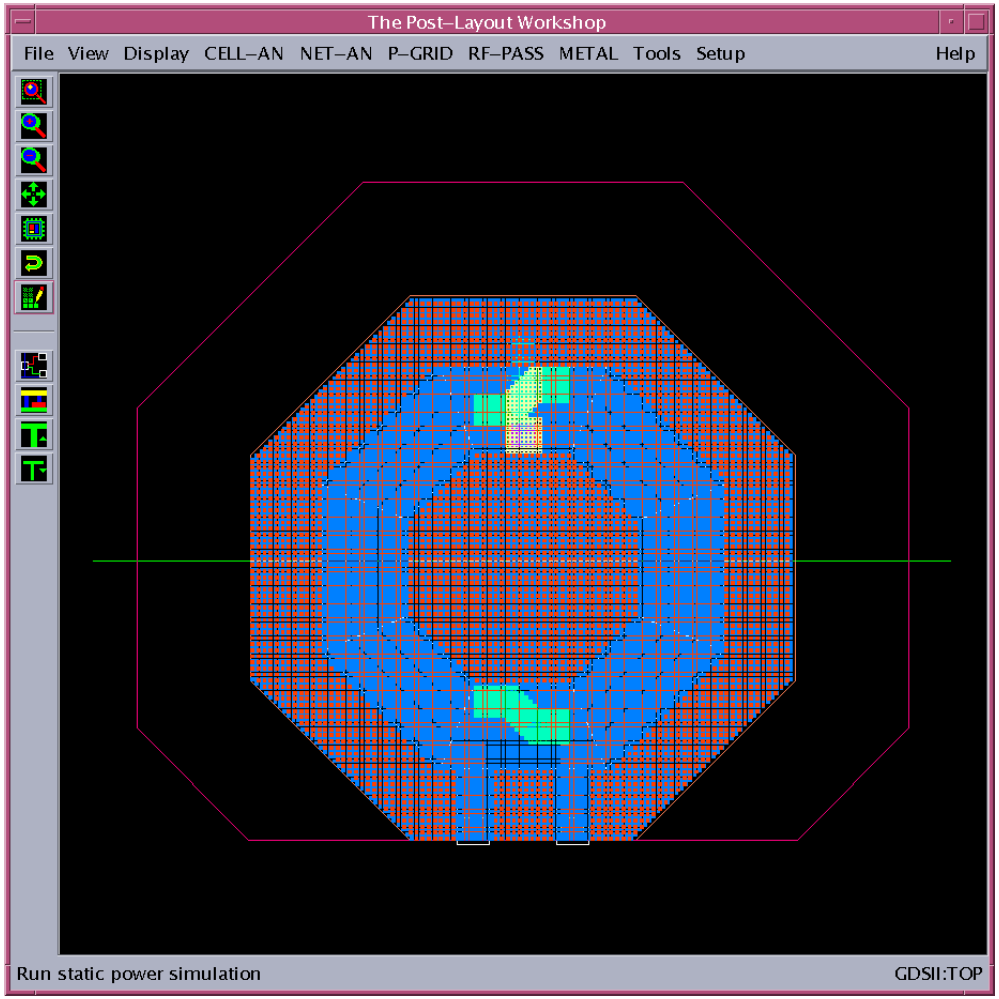
‘Simpler to Model’ RCLK Effects on the Interconnect with Shrinking Dimensions

1. Effective Metal Resistance Becomes the Function of Width (Dishing, Barrier Metal, Scattering Effects)



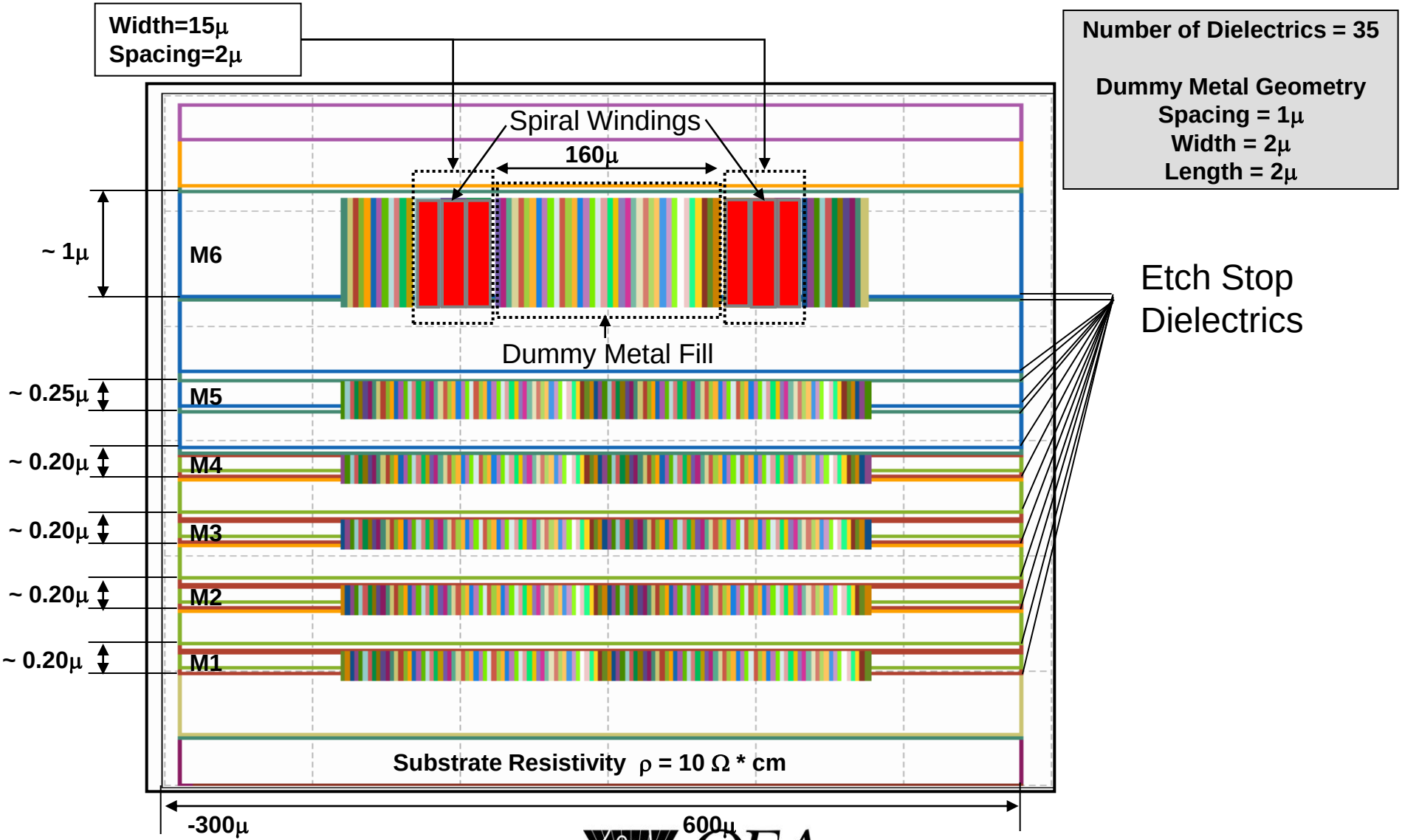
2. Metal Thickness Becomes a Function of Width & Spacing & Regional Density (CMP)

Full GDSII View of Differential Spiral with No Slots with 'Dummy Metal'

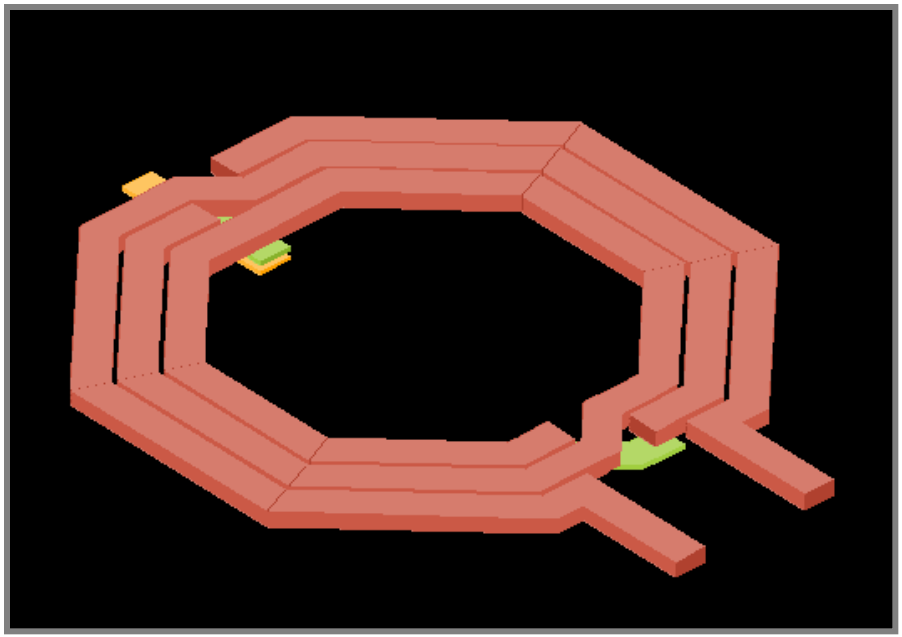


Dummy Metal Changes Capacitance and Thus Electrical Performance

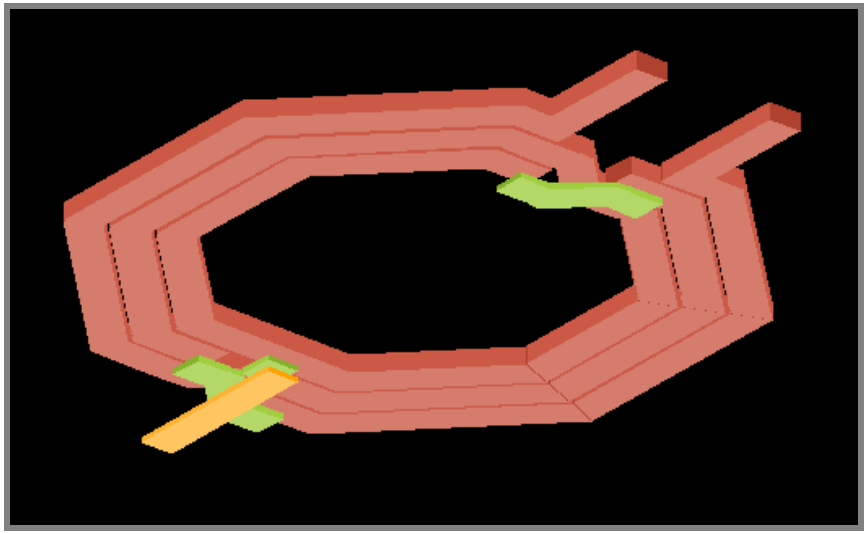
Metal Cross Section in the Center of the Spiral



3D Top & Bottom View of the Not Slotted Spiral

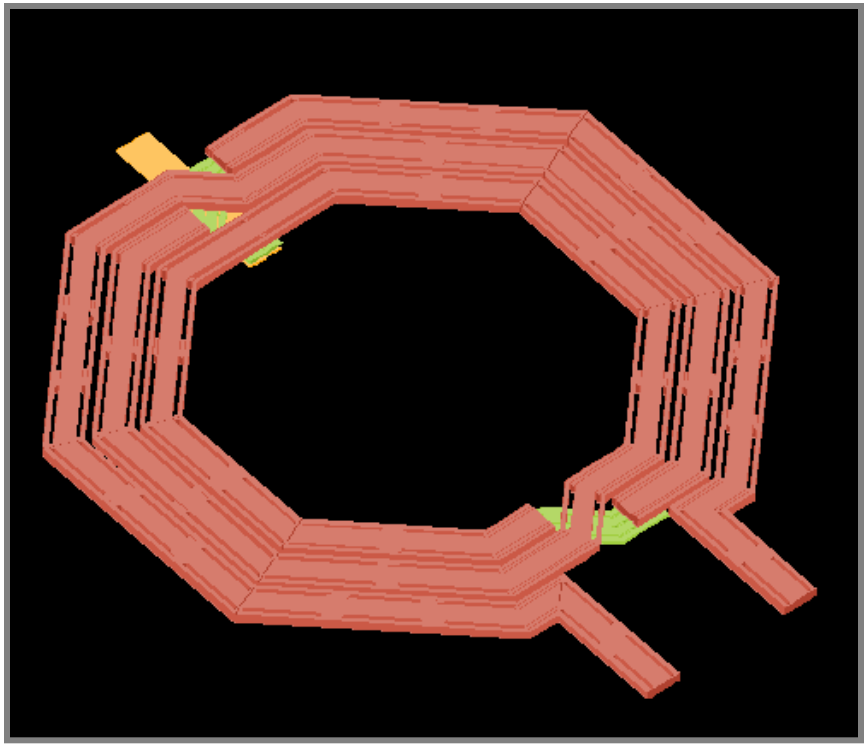


Not Slotted Spiral 3D View Top



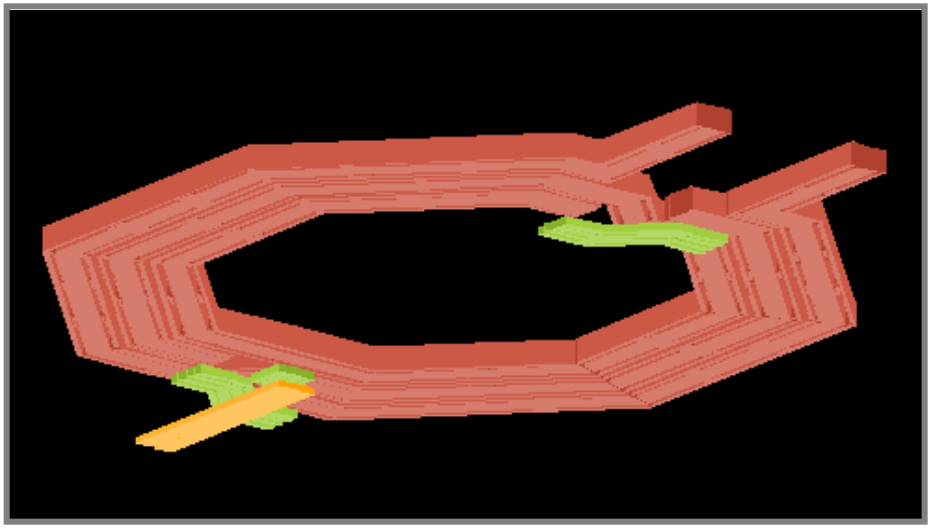
Not Slotted Spiral 3D View Bottom

3D Top & Bottom View of the Slotted Spiral



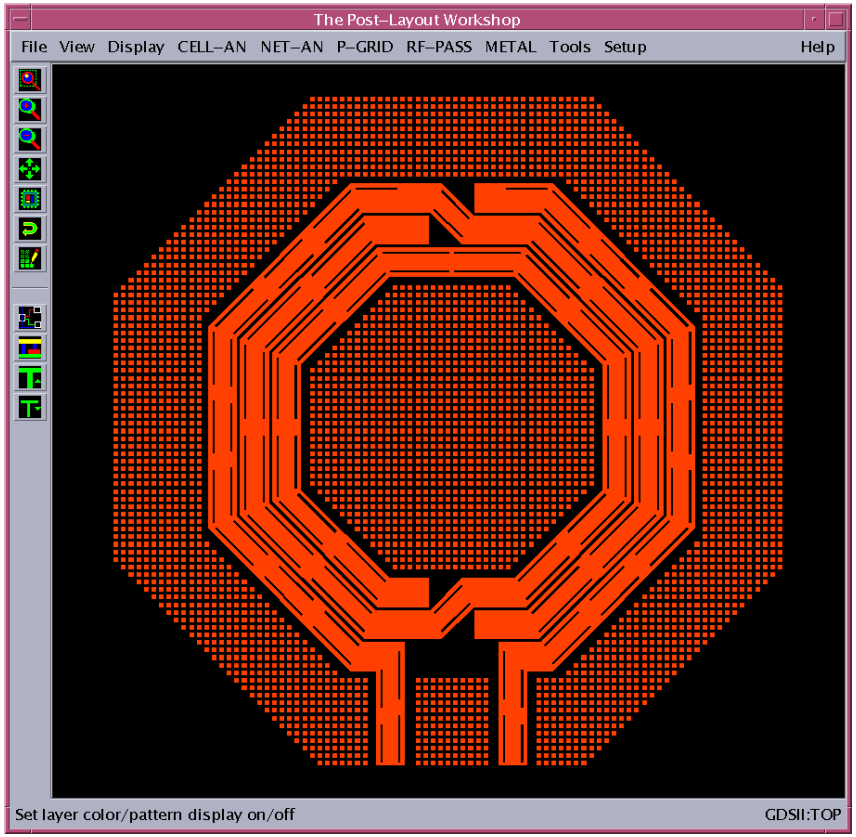
Slotted Spiral 3D Top

Wide Metal Slotting Rules Changes RCLK and Thus Electrical Model

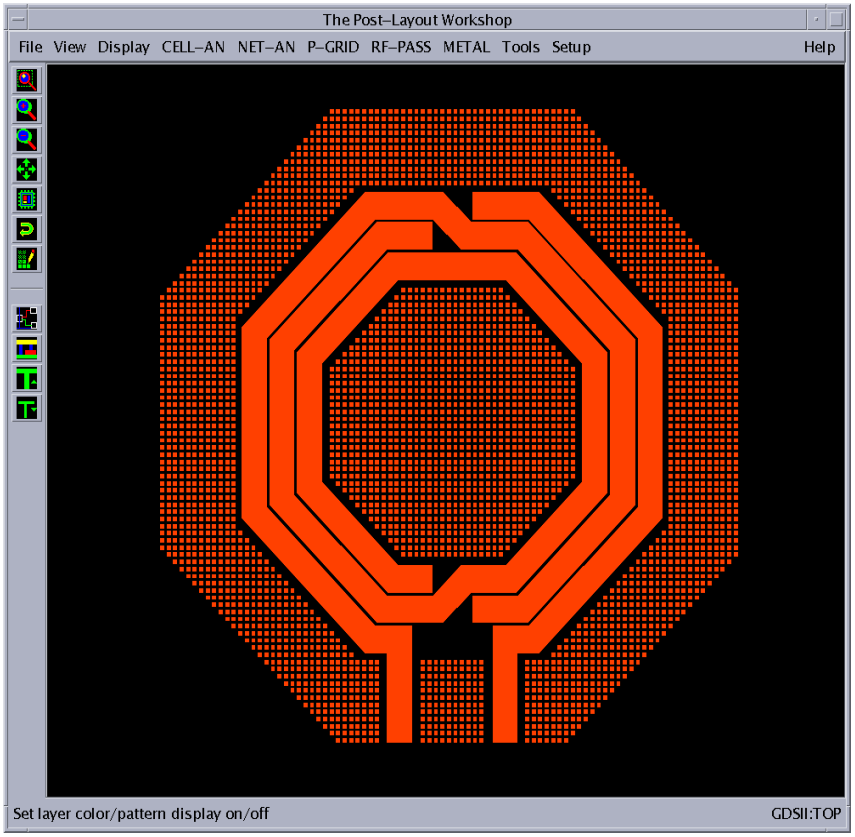


Slotted Spiral 3D Bottom

M6 GDSII View of Slotted & Not Slotted Spiral

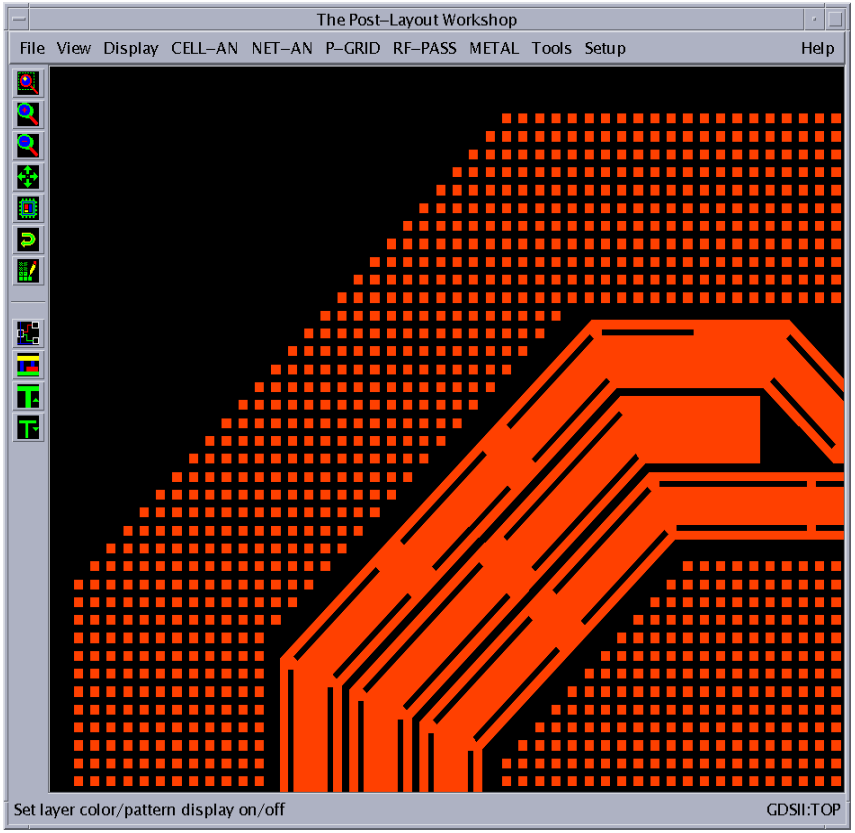


M6 with Slotted Spiral

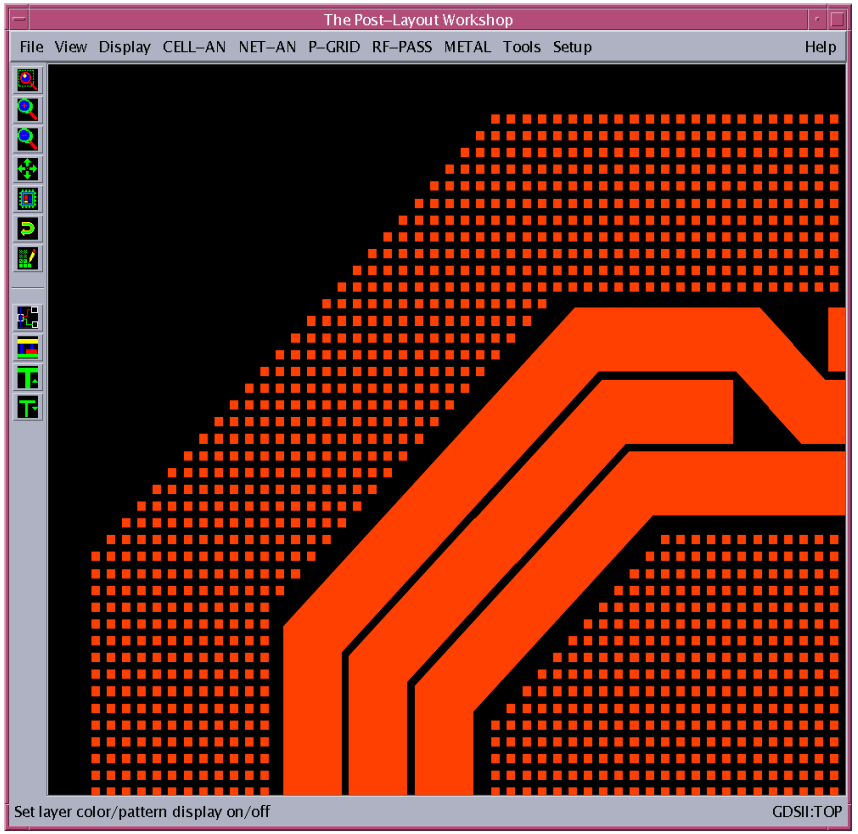


M6 Not Slotted Spiral

Zoomed in M6 GDSII View of Slotted & Not Slotted Spiral

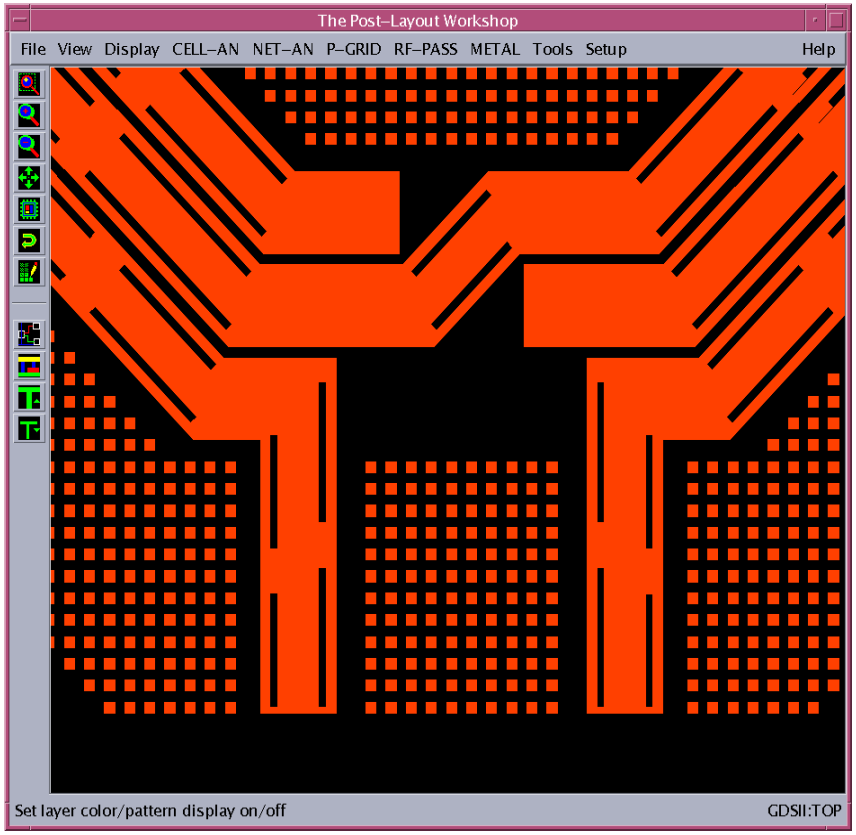


Zoomed in M6 with Slotted Spiral Upper Left Corner

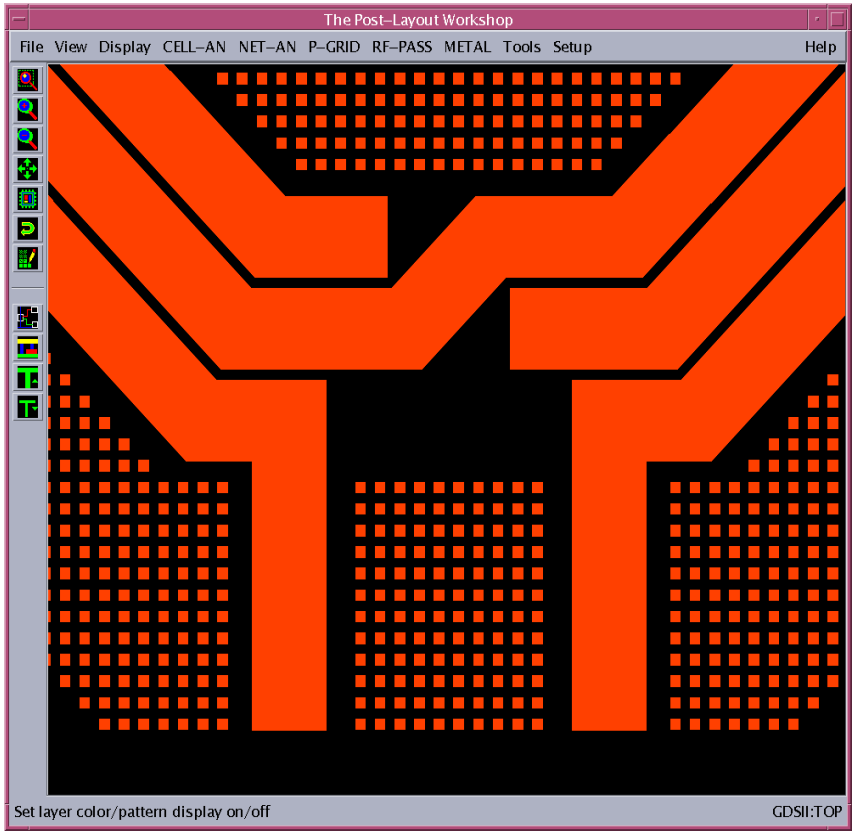


Zoomed in M6 with Not Slotted Spiral Upper Left Corner

Zoomed in M6 GDSII Bottom View of Slotted & Not Slotted Spiral

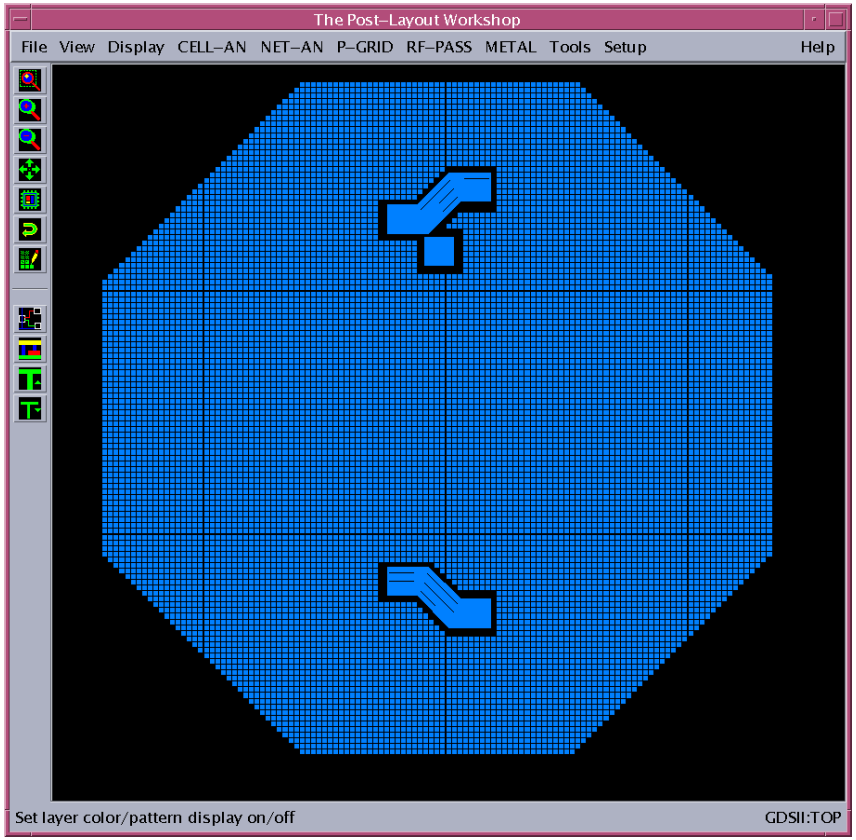


M6 with Slotted Spiral Bottom View Legs

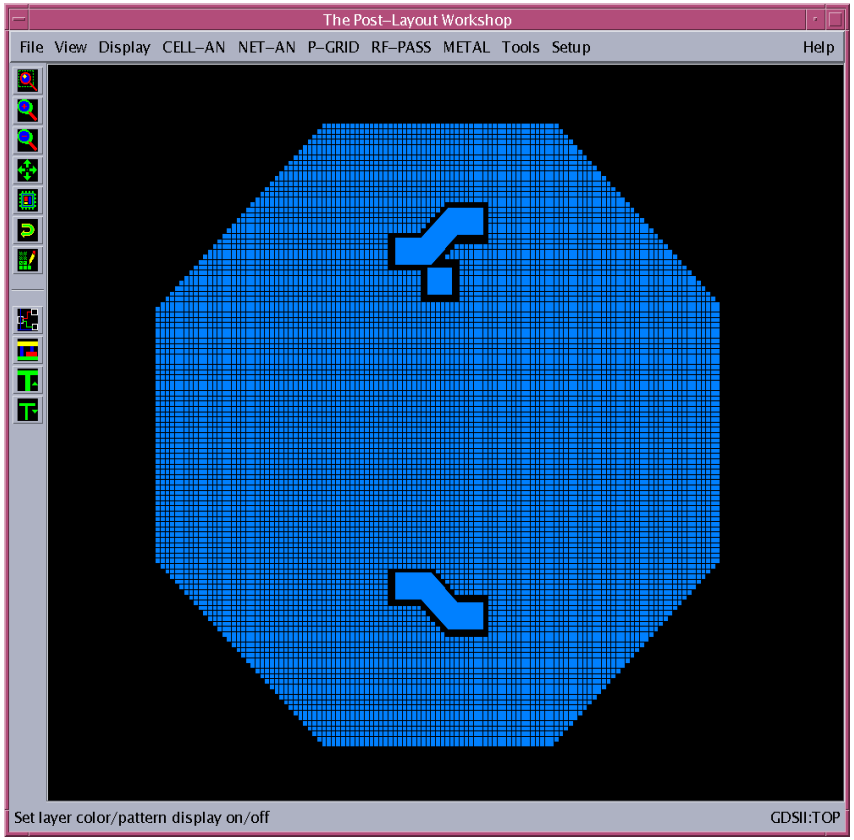


M6 Not Slotted Spiral Bottom View Legs

M5 GDSII View of Slotted & Not Slotted Spiral

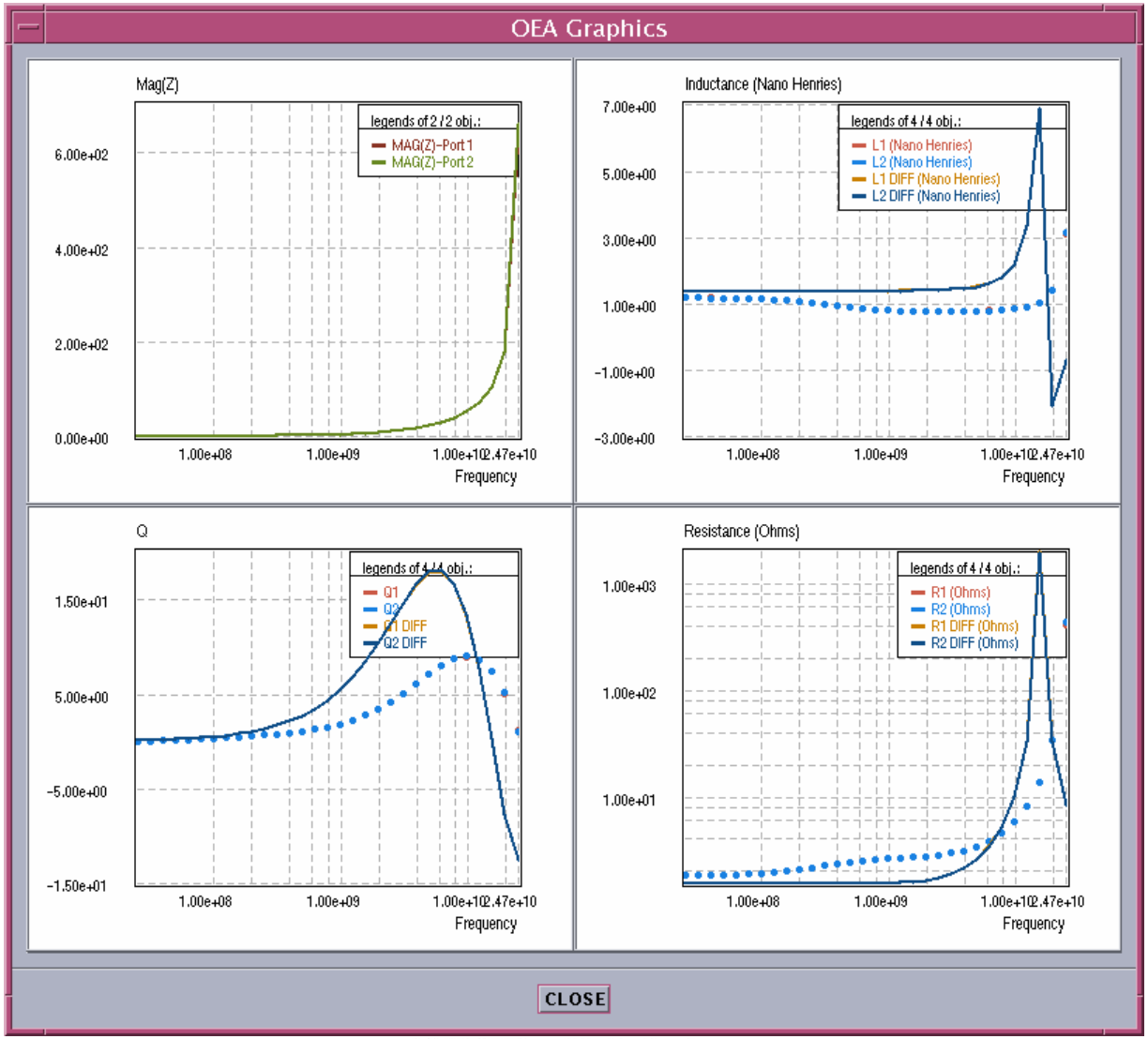


M5 with Slotted Spiral

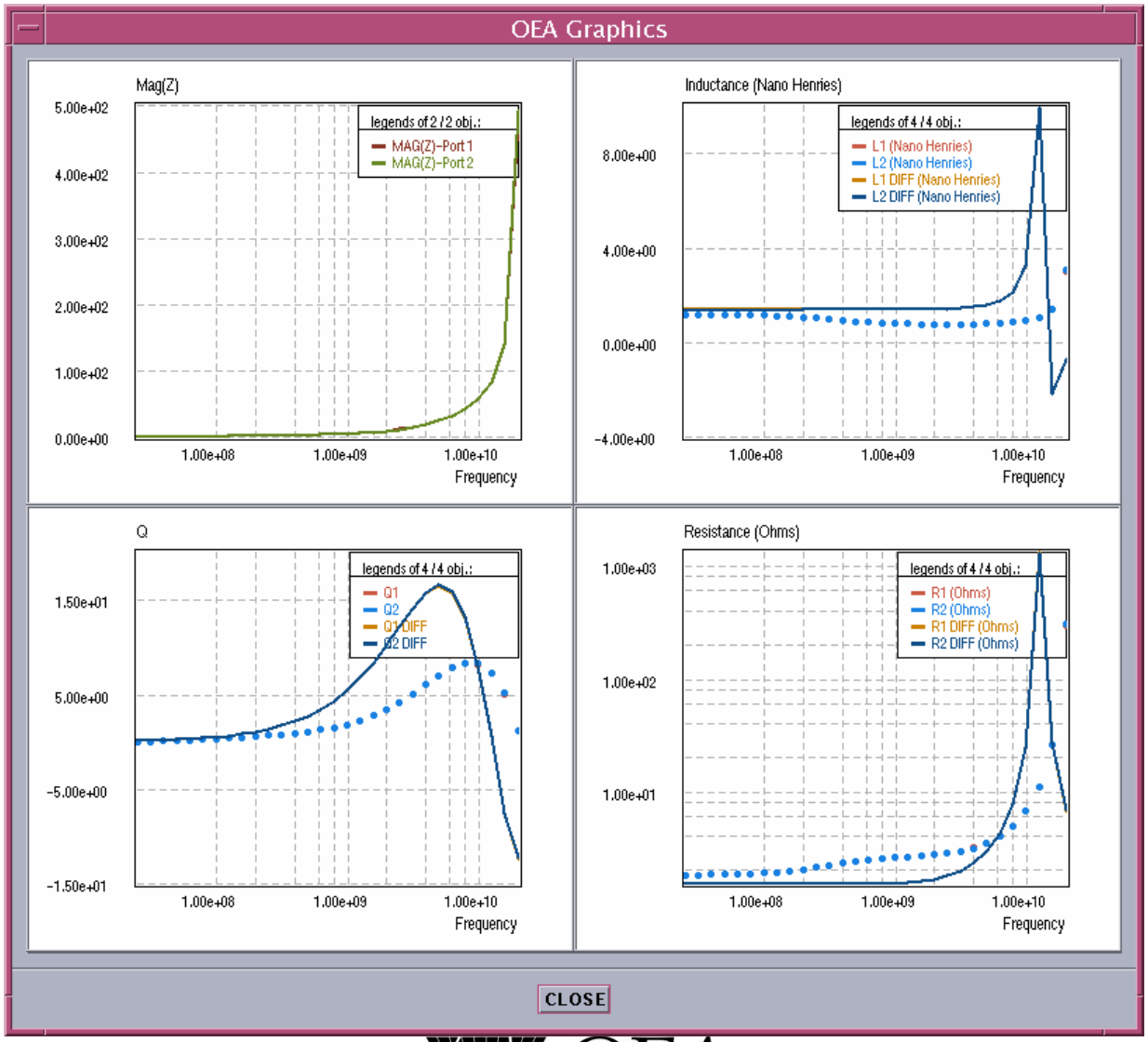


M5 Not Slotted Spiral

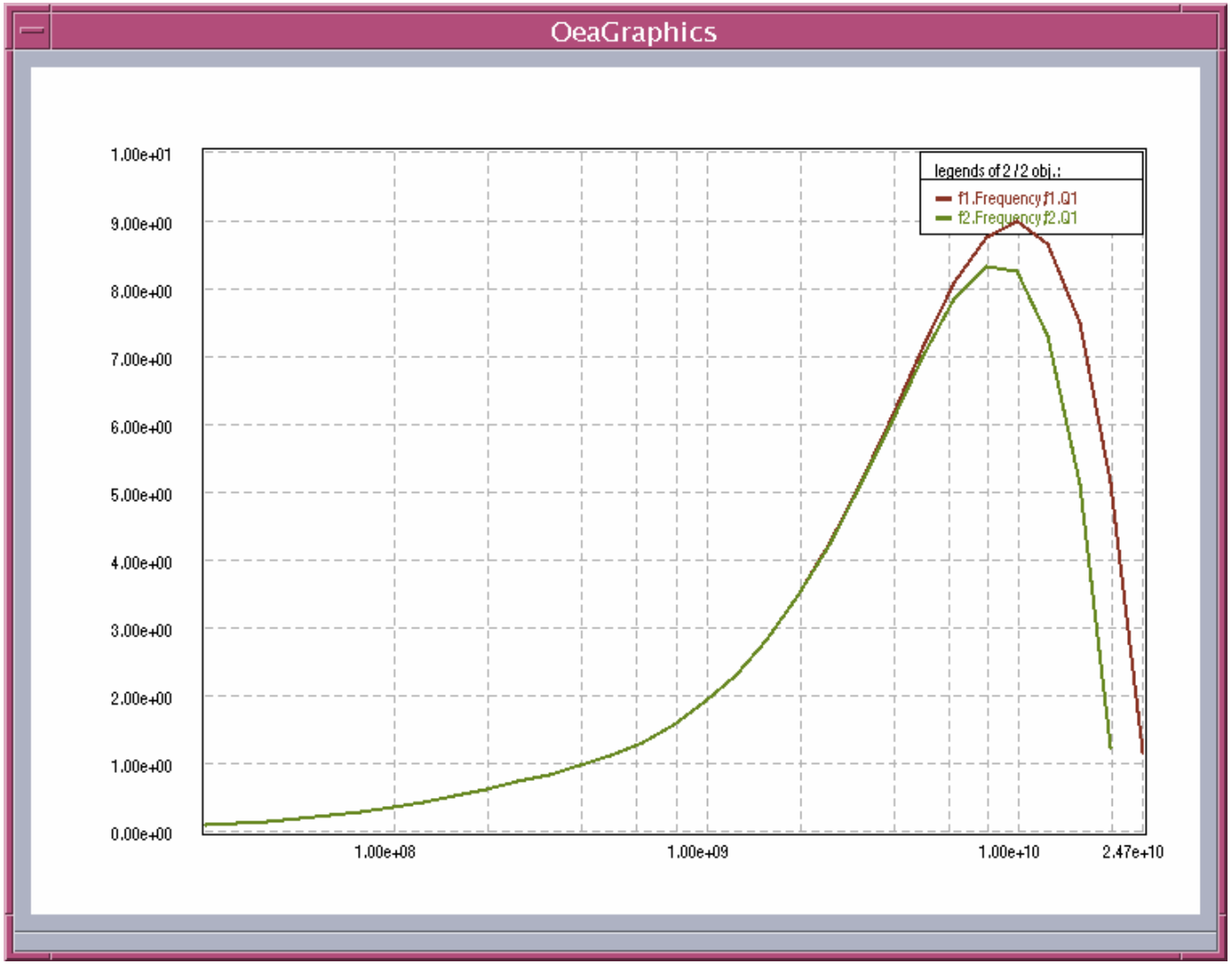
Spiral LRQ Without Dummy Metal



Spiral LRQ With Dummy Metal



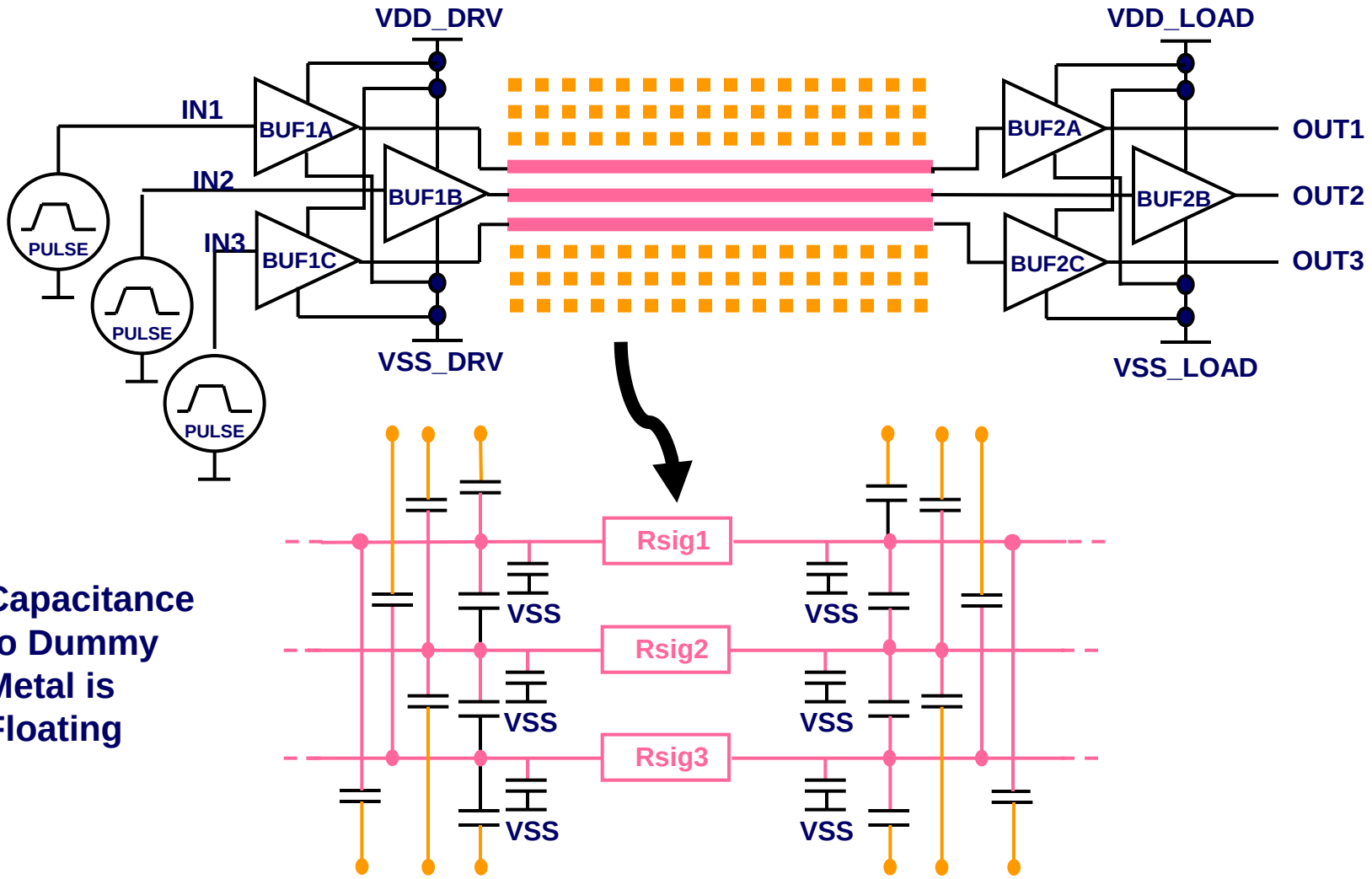
Spiral Q With and Without Dummy Metal



Section 2

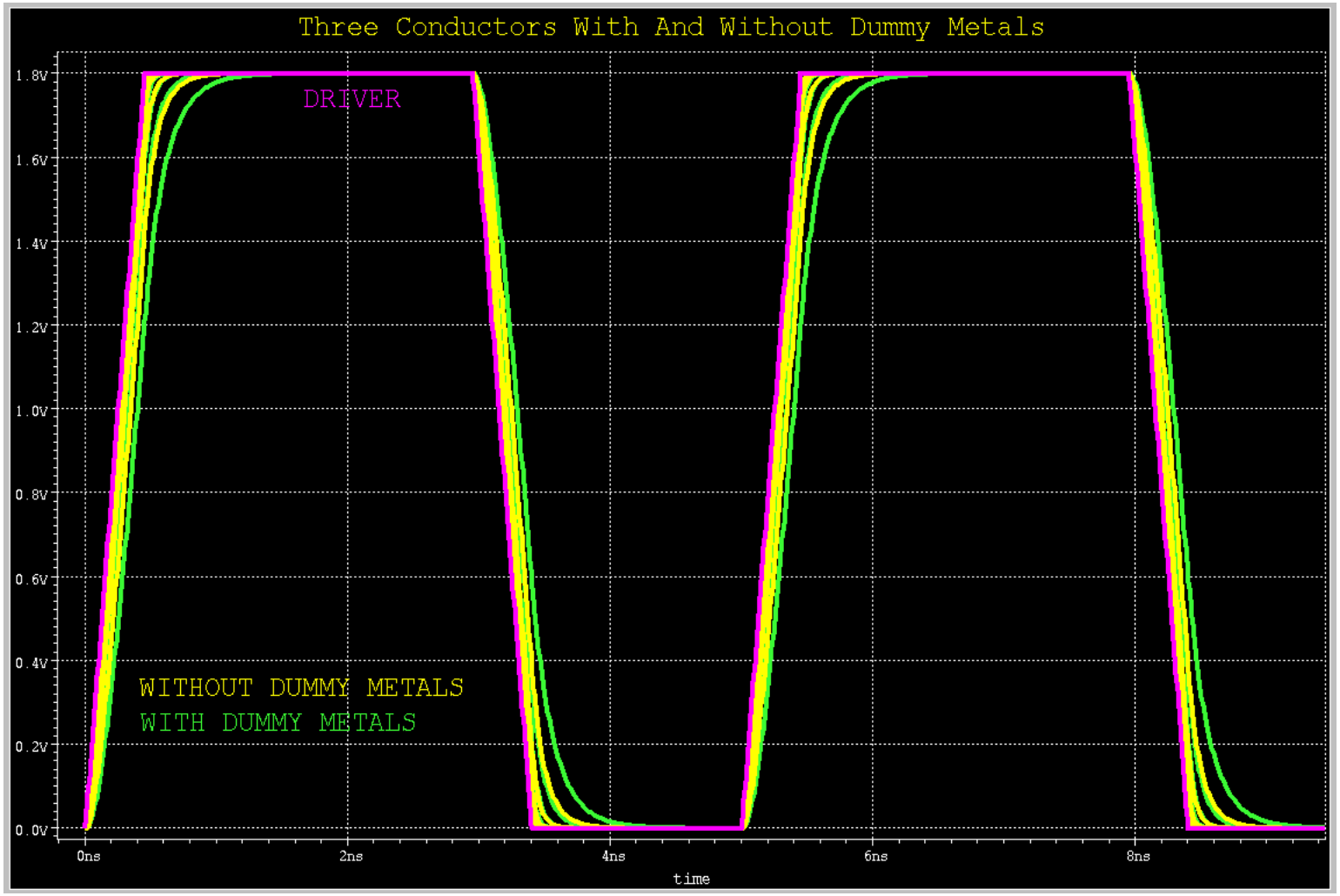
- Dummy Metal Effects on Long Interconnects
  - Modeling 1000um to 8000um Lines
  - Delay Differences
  - Effect on Noise to Neighboring Nets

A Look at How Dummy Metal Affects Long Interconnects

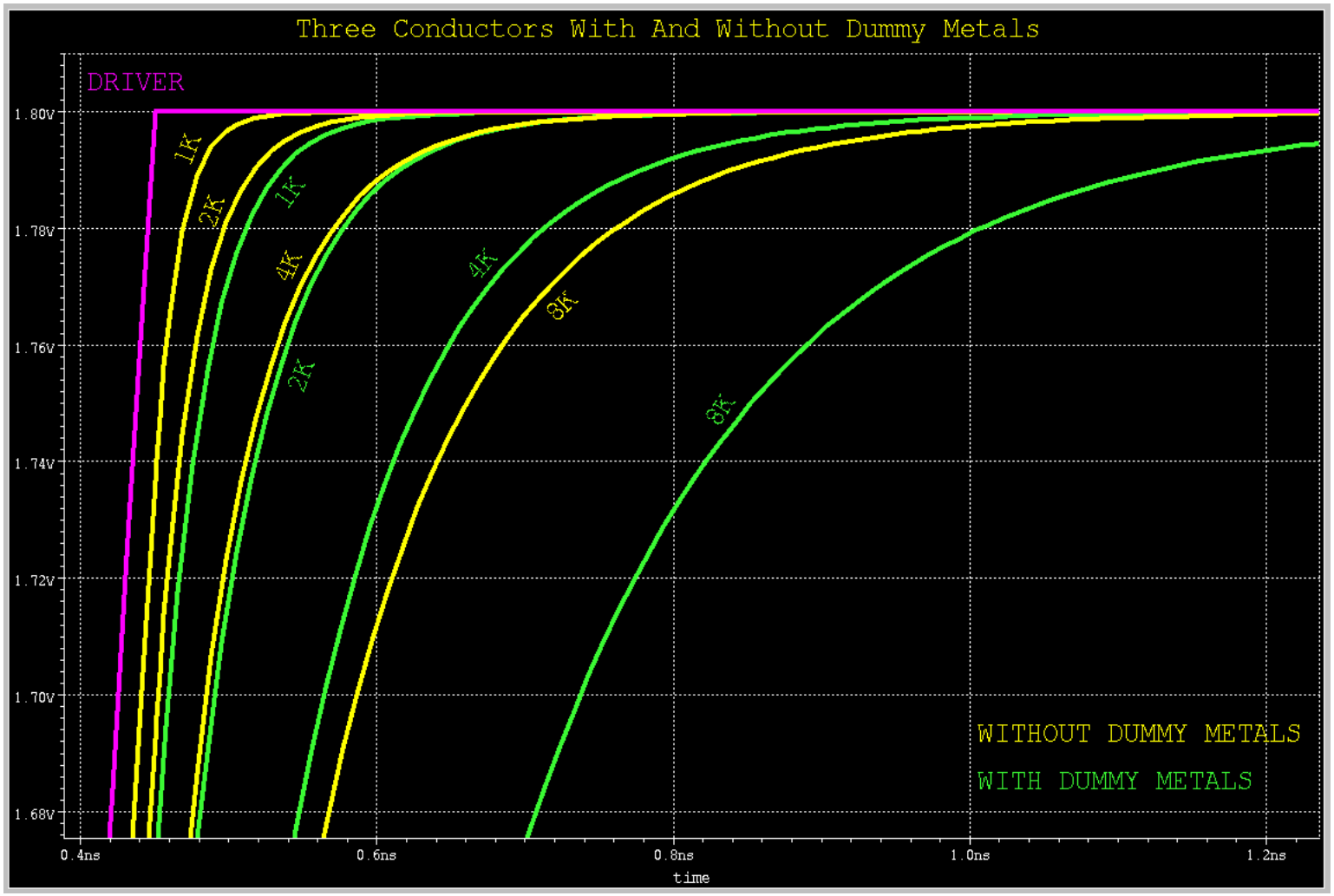


Capacitance to Dummy Metal is Floating

3 Conductors With & Without Dummy Metal of Lengths 1000u, 2000u, 4000u, and 8000u



3 Conductors With & Without Dummy Metal of Lengths 1000u, 2000u, 4000u, and 8000u



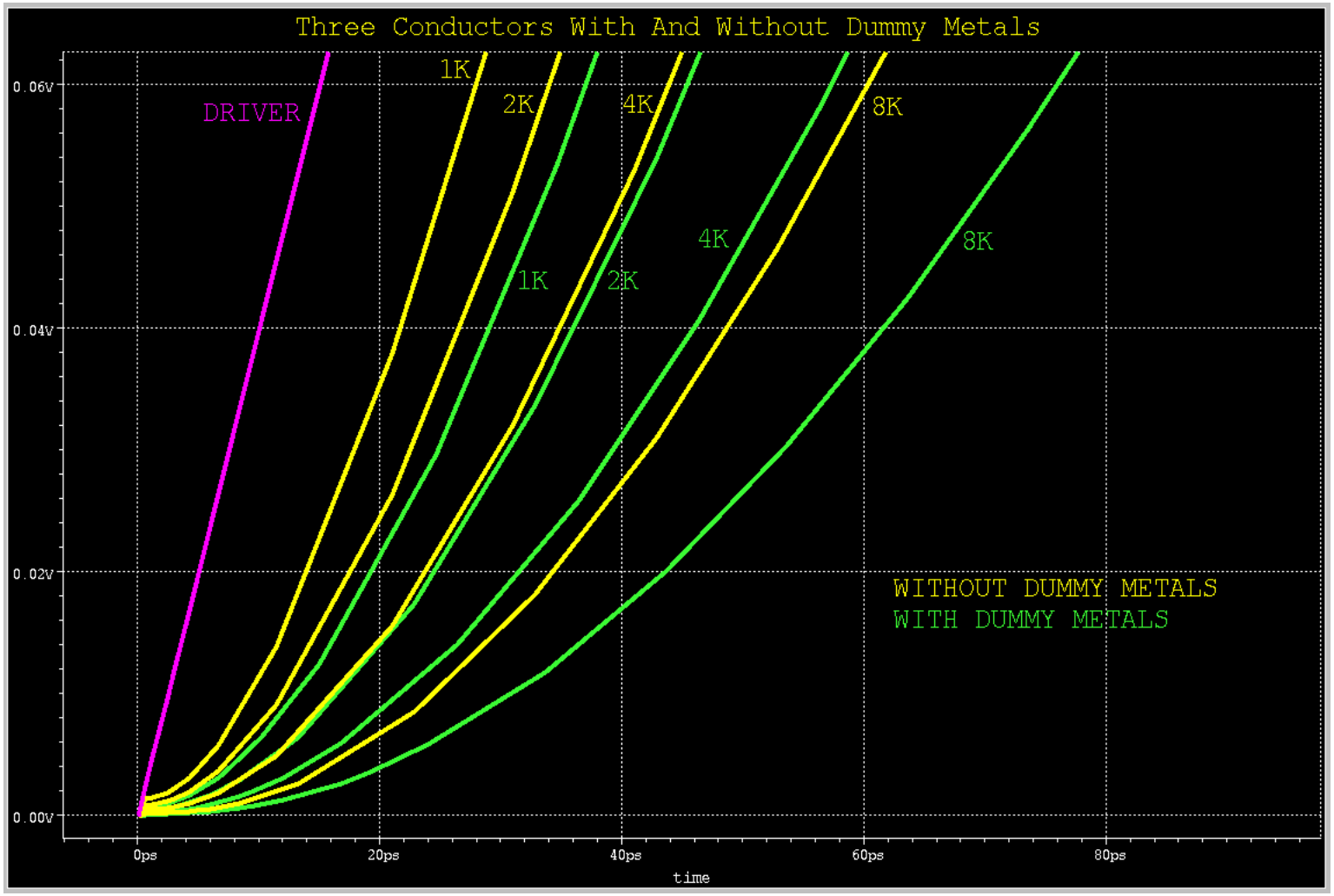
1.80V

1.68V

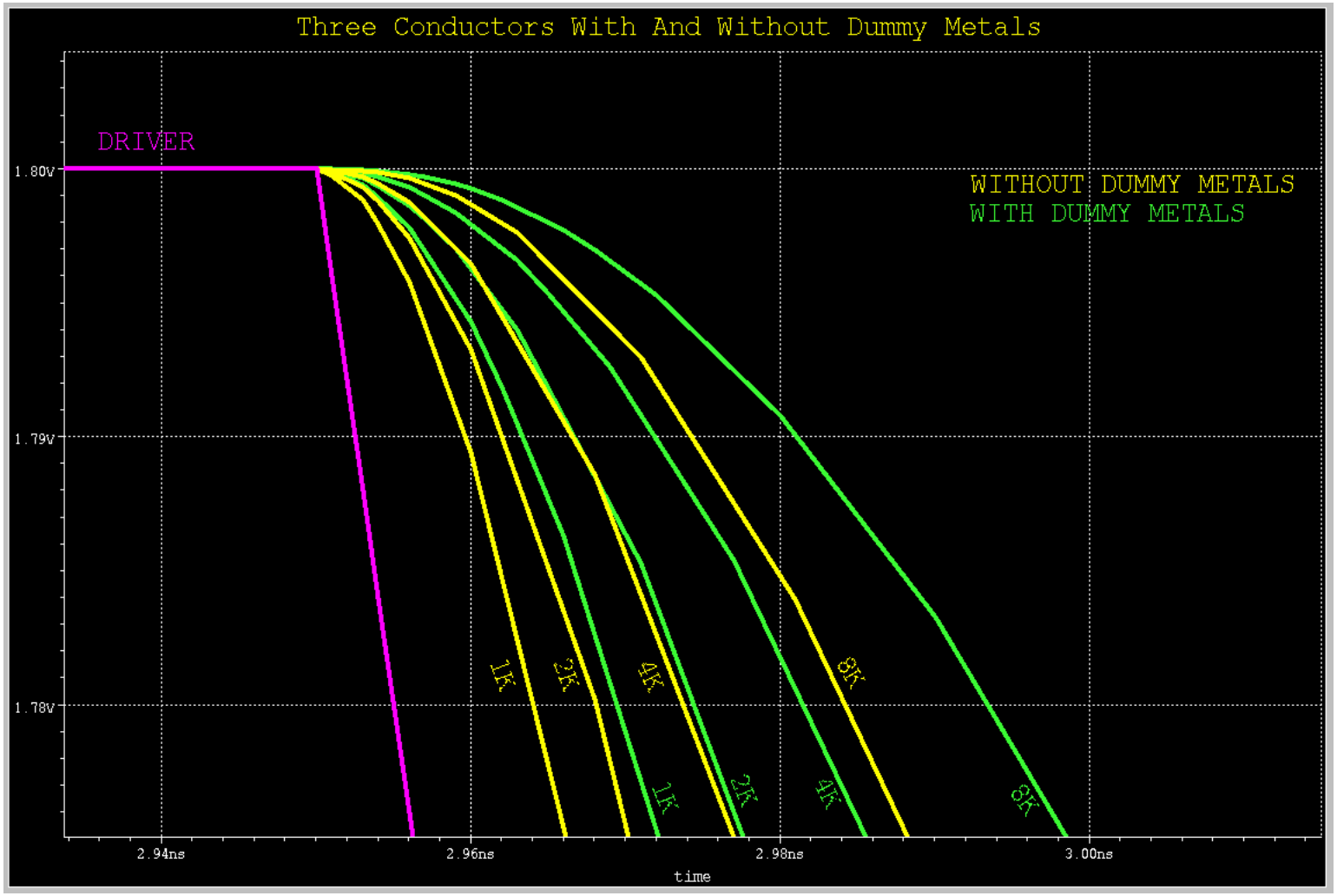
400ps

1200ps

3 Conductors With & Without Dummy Metals of Lengths 1000u, 2000u, 4000u, and 8000u



3 Conductors With & Without Dummy Metal of Lengths 1000u, 2000u, 4000u, and 8000u



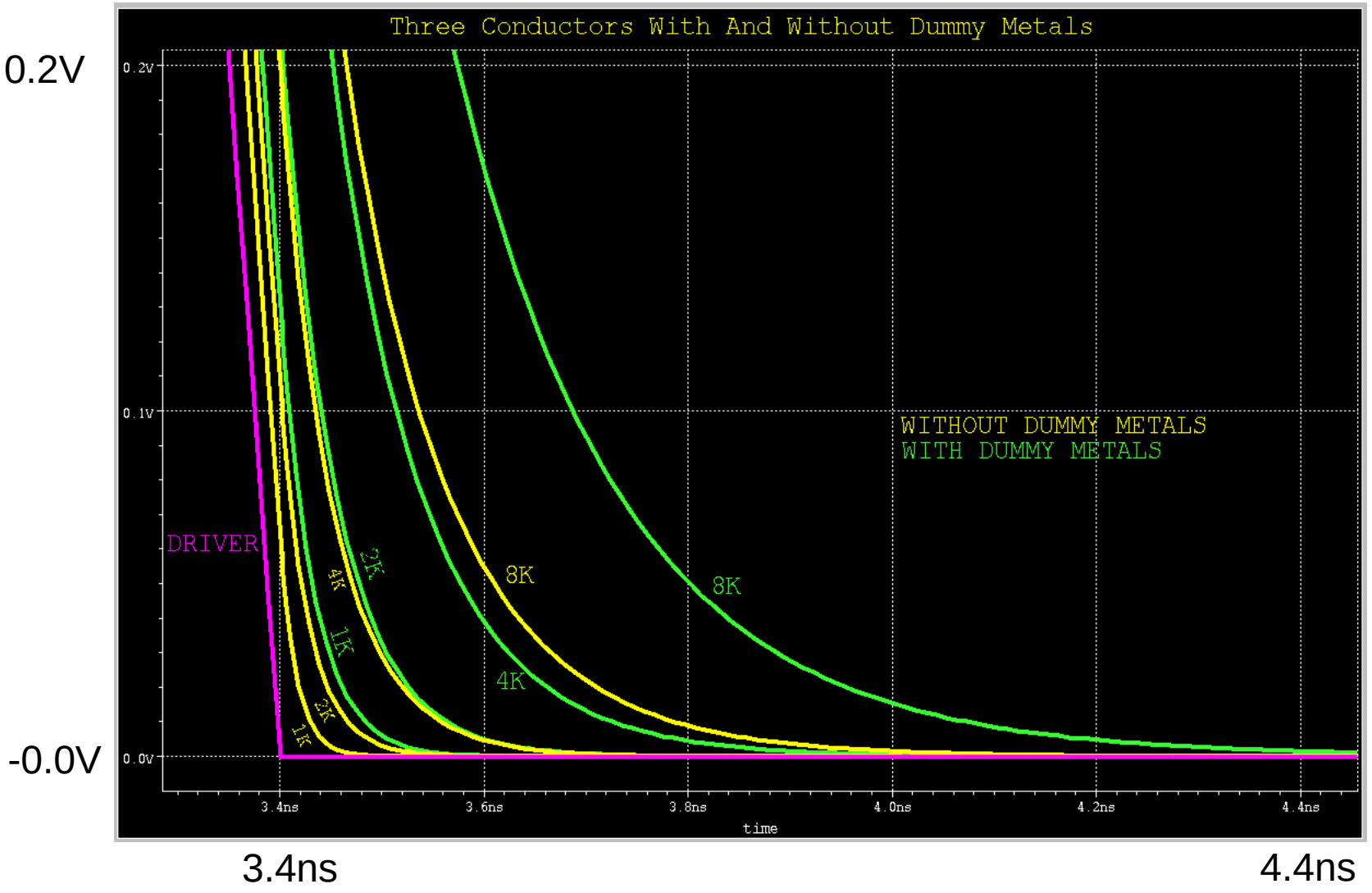
1.80V

1.78V

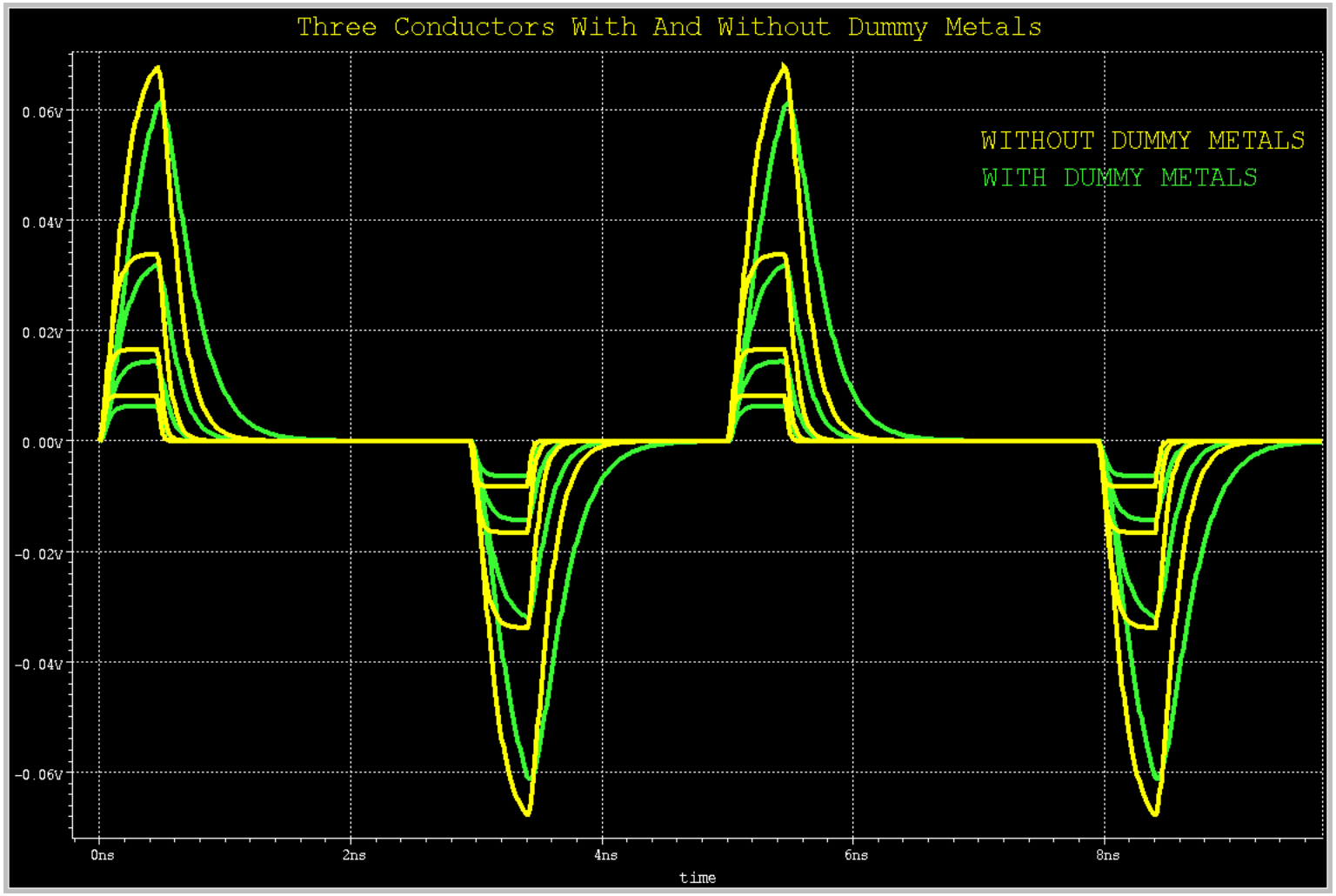
2.94ns

3.00ns

3 Conductors With & Without Dummy Metal of Lengths 1000u, 2000u, 4000u, and 8000u



3 Conductors With & Without Dummy Metal of Lengths 1000u, 2000u, 4000u, and 8000u



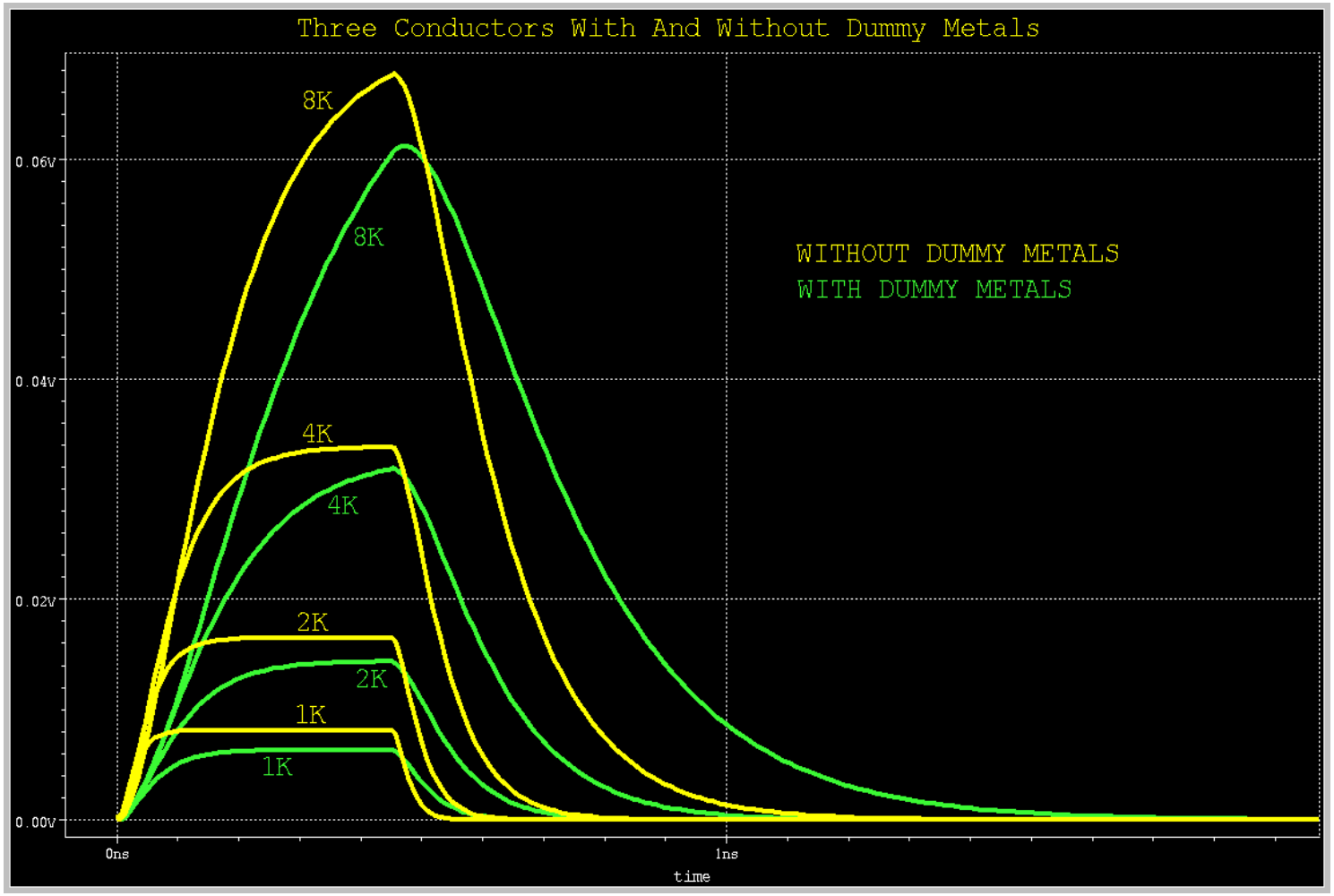
0.06V

-0.06V

0.0ns

8ns

3 Conductors With & Without Dummy Metal of Lengths 1000u, 2000u, 4000u, and 8000u



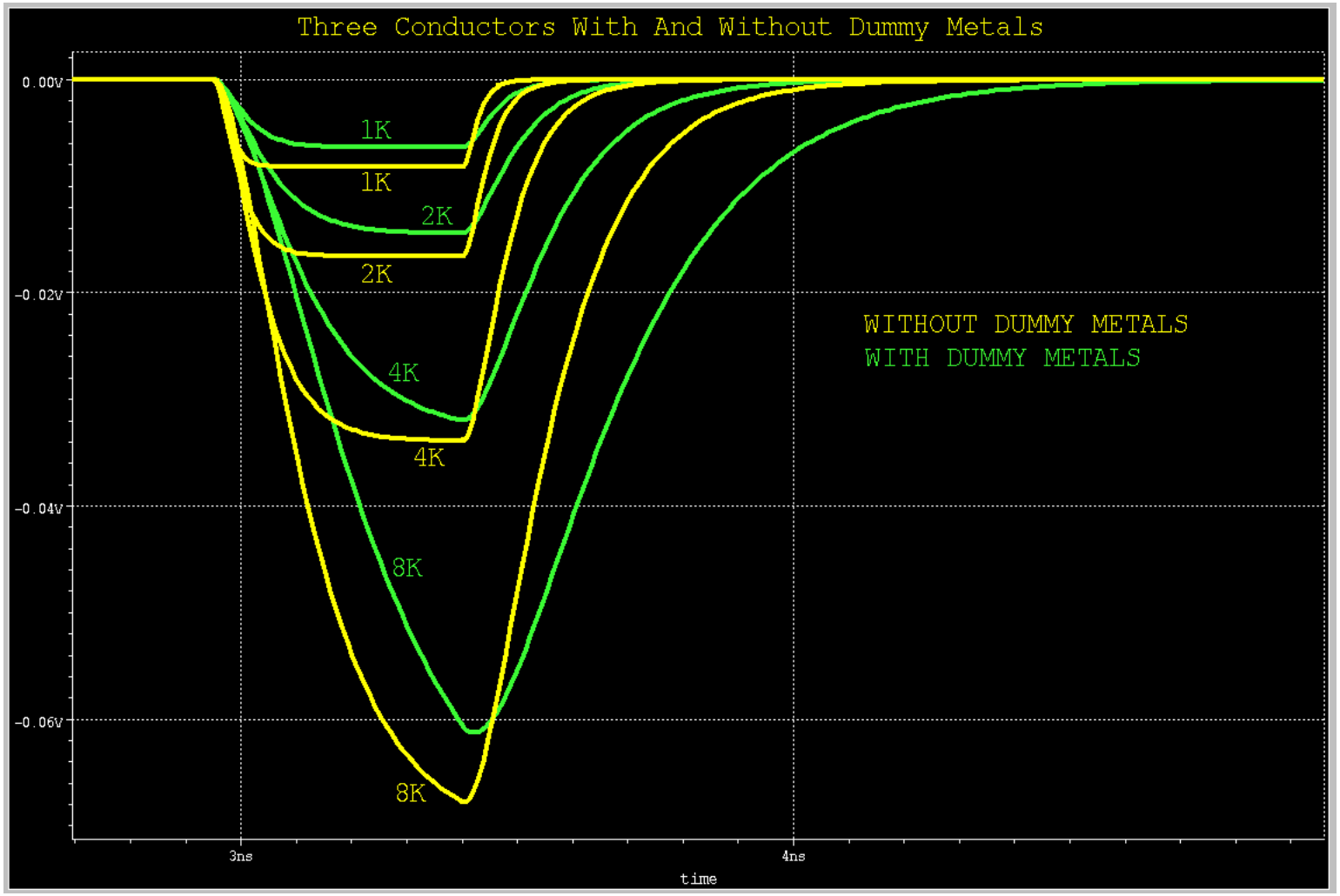
0.06V

0.00V

0ns

1ns

3 Conductors With & Without Dummy Metal of Lengths 1000u, 2000u, 4000u, and 8000u



0.00V

-0.06V

3ns

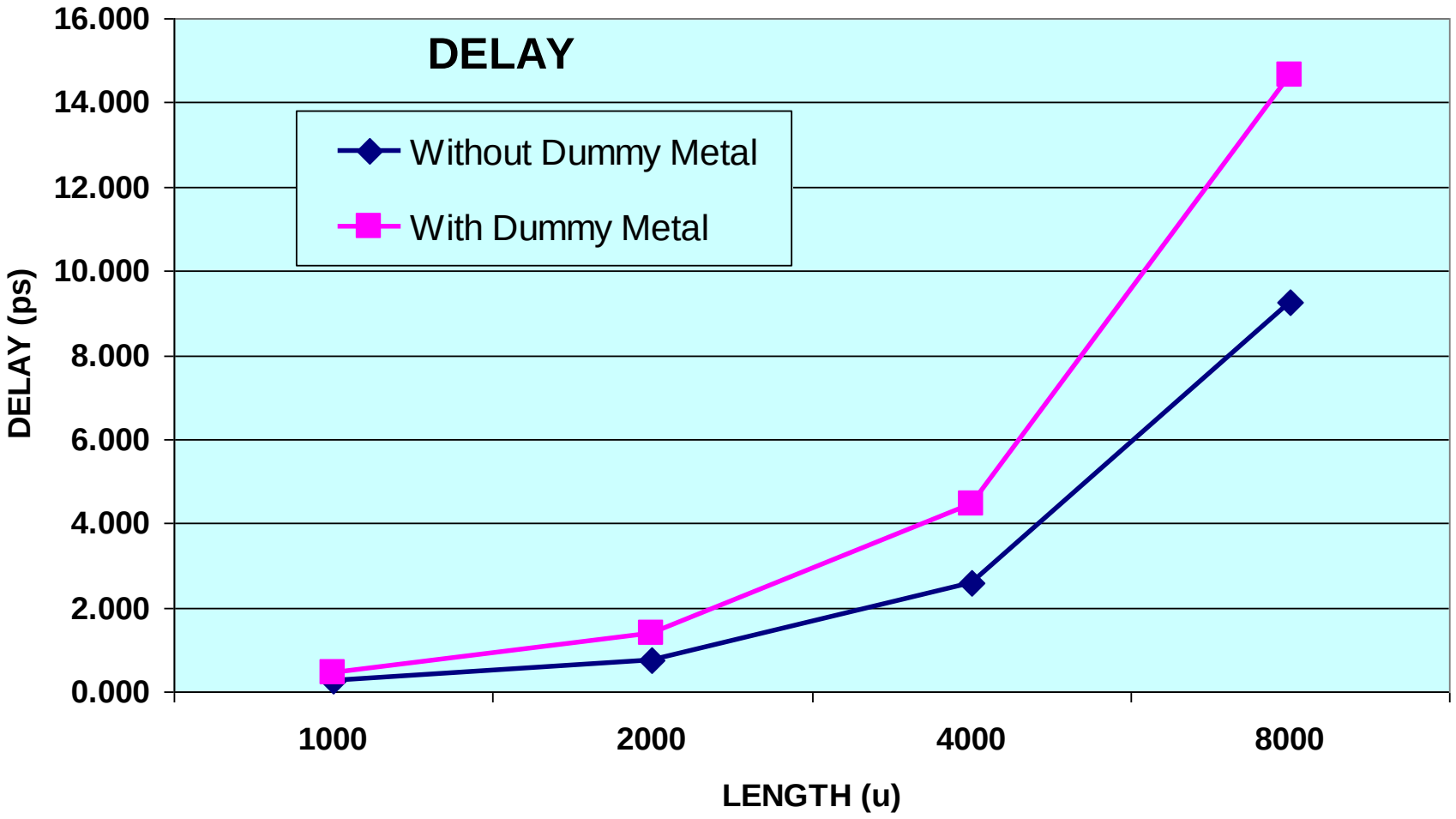
4ns

Summary of 3 Conductor Cases

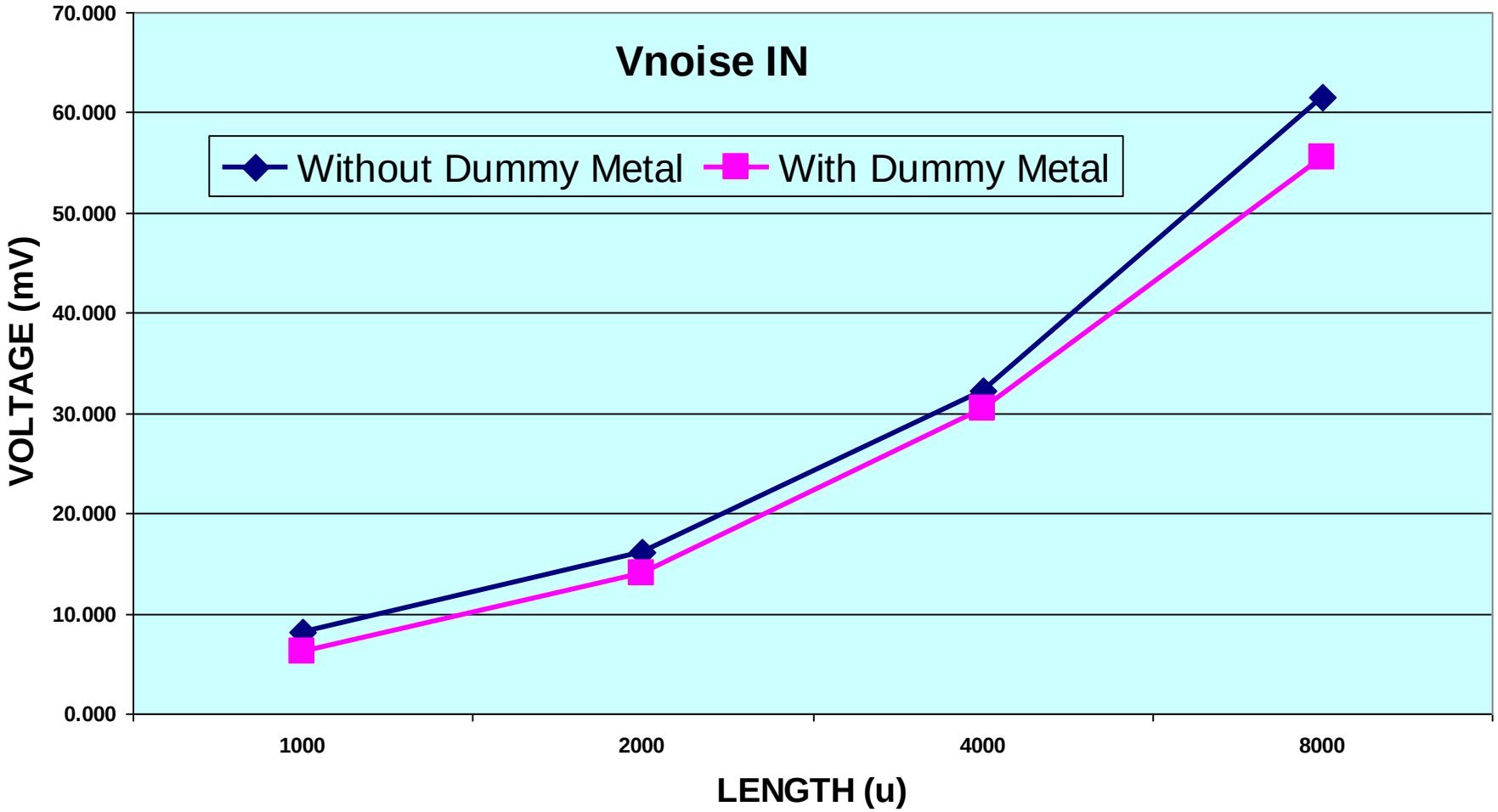
LENGTH	DELAY	Vnoise_IN	Vnoise_OUT
Without Dummy Metal	ps	mV	mV
1000	0.254	8.074	8.174
2000	0.768	16.150	16.550
4000	2.576	32.210	33.800
8000	9.255	61.540	67.710

LENGTH	DELAY	Vnoise_IN	Vnoise_OUT
With Dummy Metal	ps	mV	mV
1000	0.459	6.164	6.240
2000	1.401	14.010	14.360
4000	4.444	30.420	31.930
8000	14.650	55.570	61.200

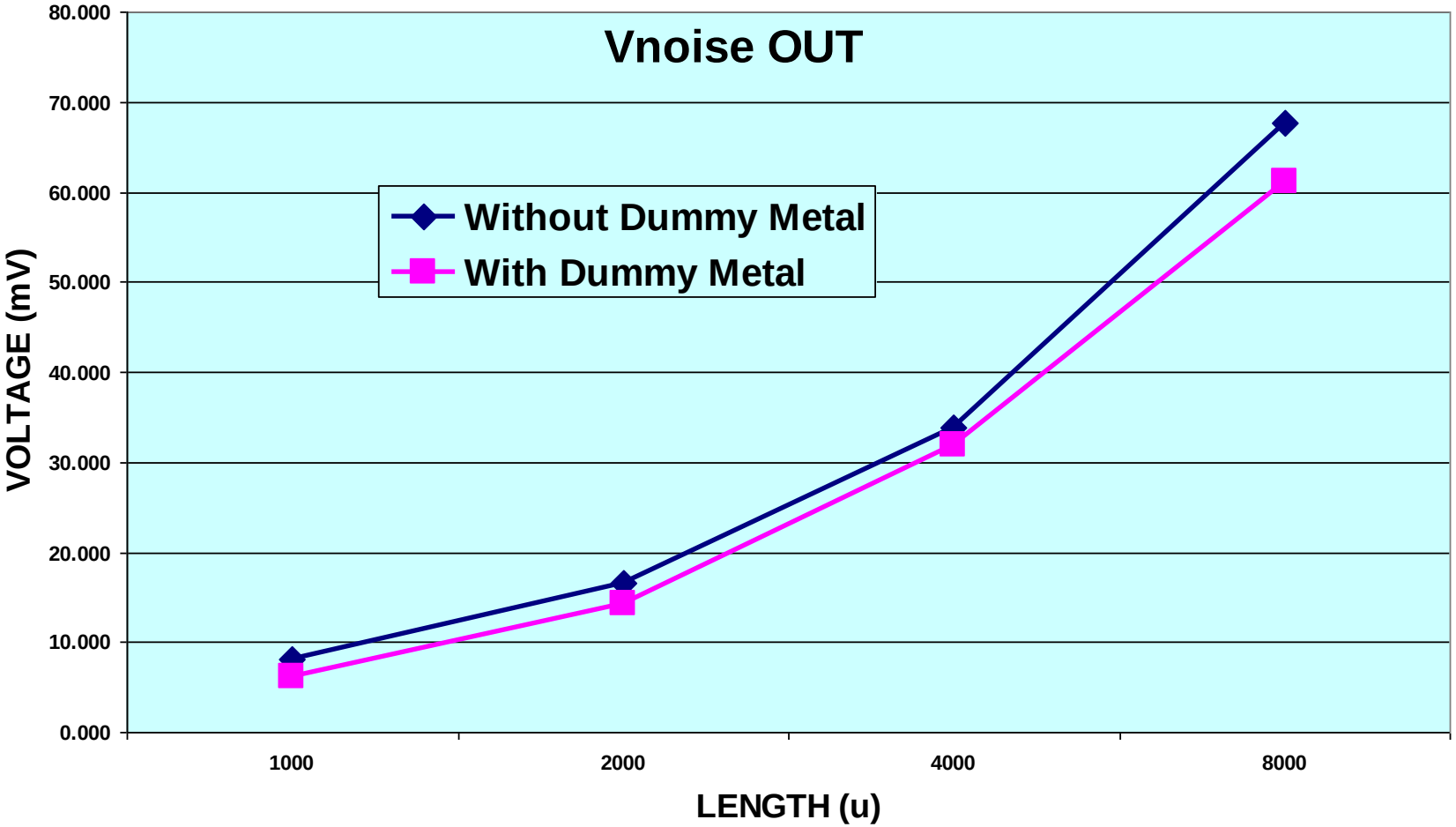
Summary of 3 Conductor Case



Summary of 3 Conductor Case



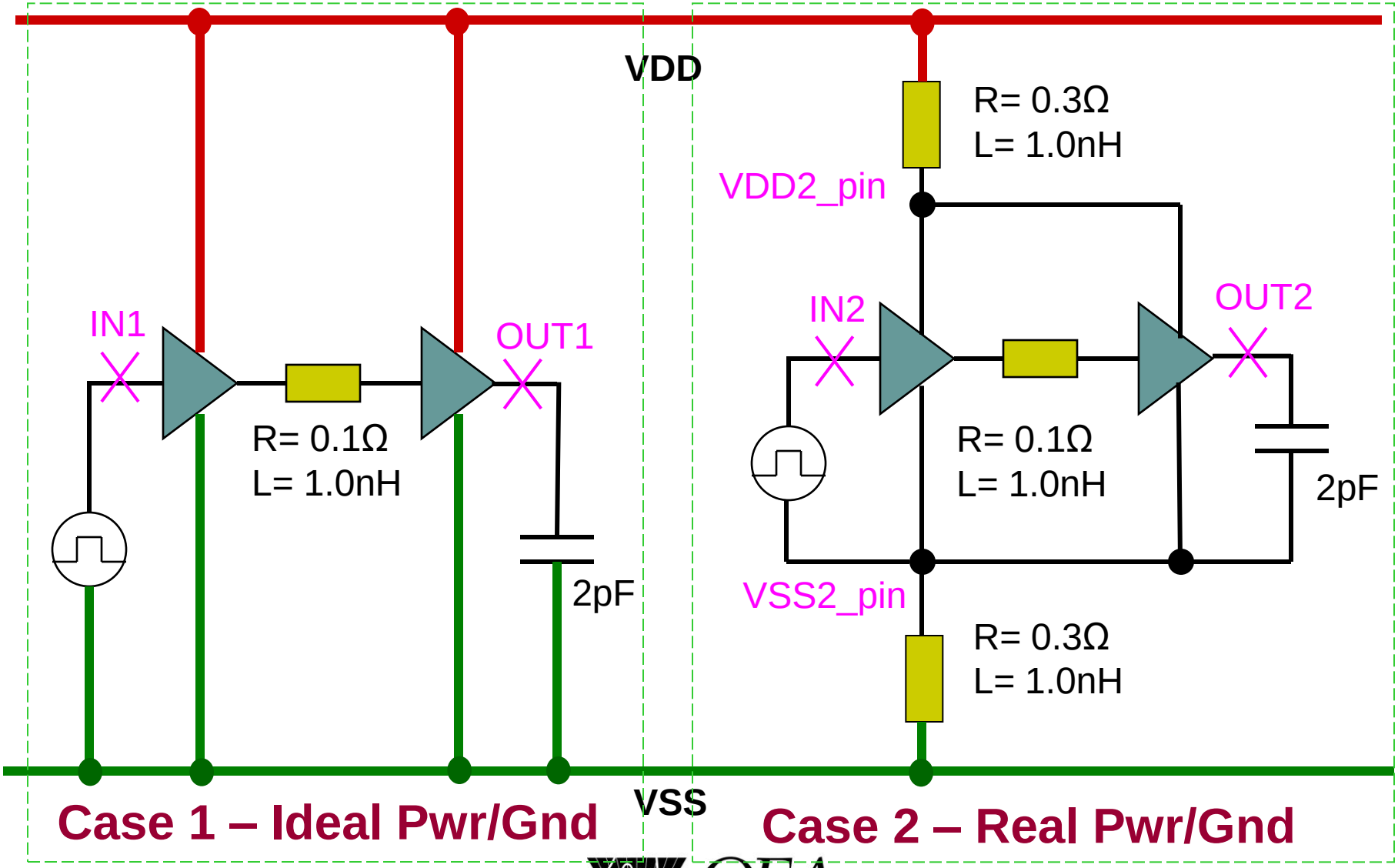
Summary of 3 Conductor Case



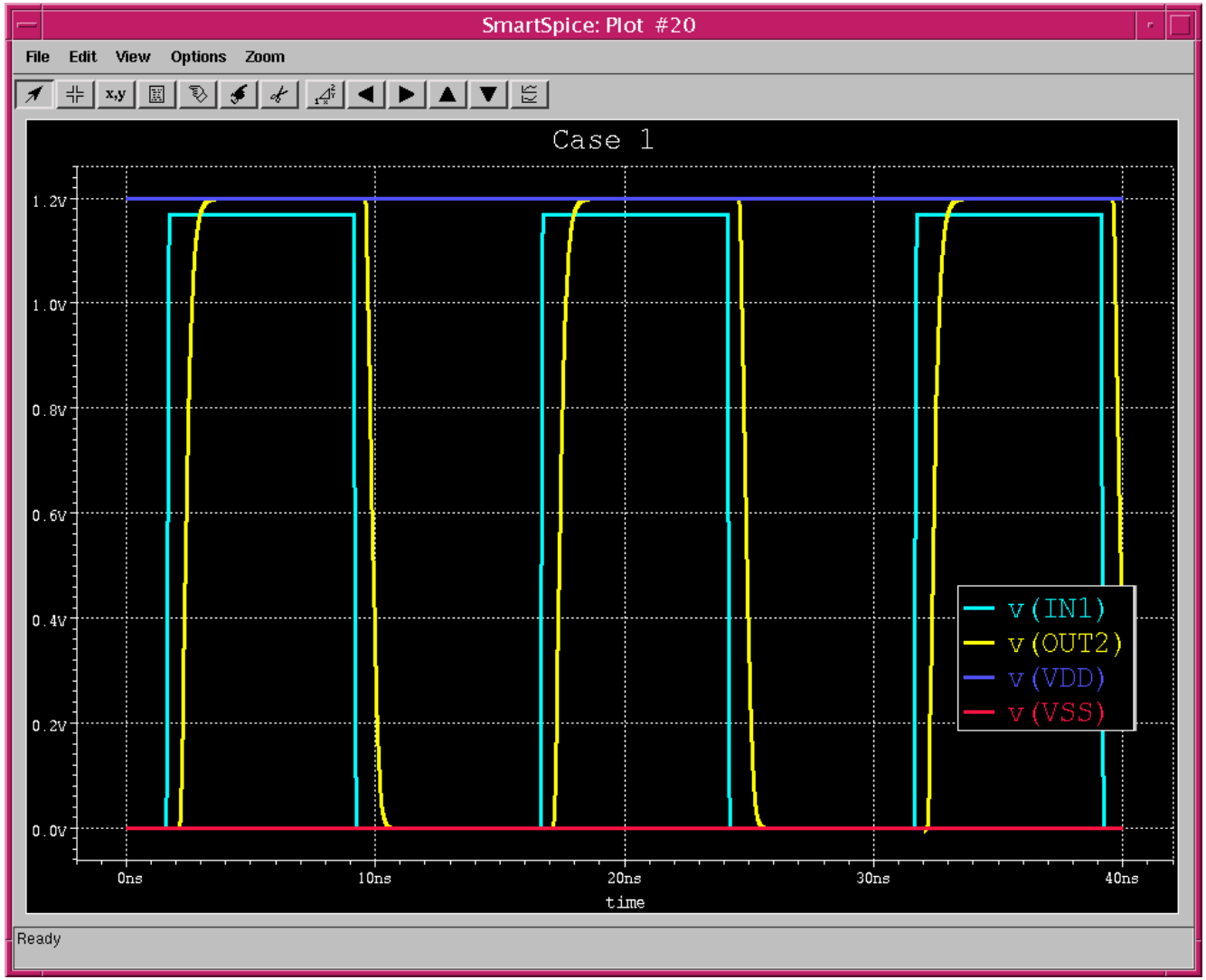
Section 3

- Power Net Delivery Issues
  - Power Network Modeling
    - Ideal Power/Ground versus Real Impedance of Power/Ground
    - By-Pass Effects
  - Simulation of Power Delivery Grid
    - Effective Impedance
    - Importance of Mutual Inductance in Calculation

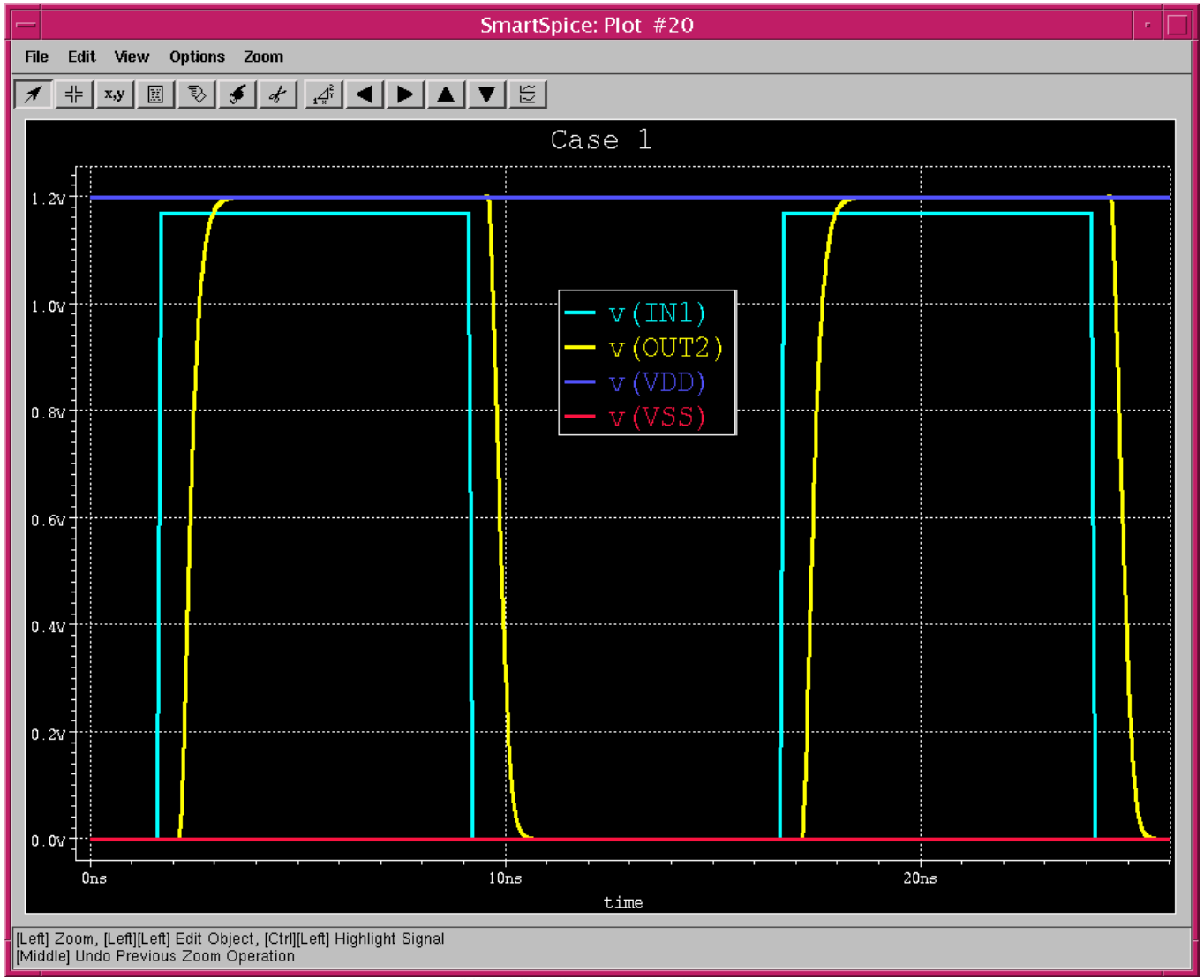
Modeling Power Impedances



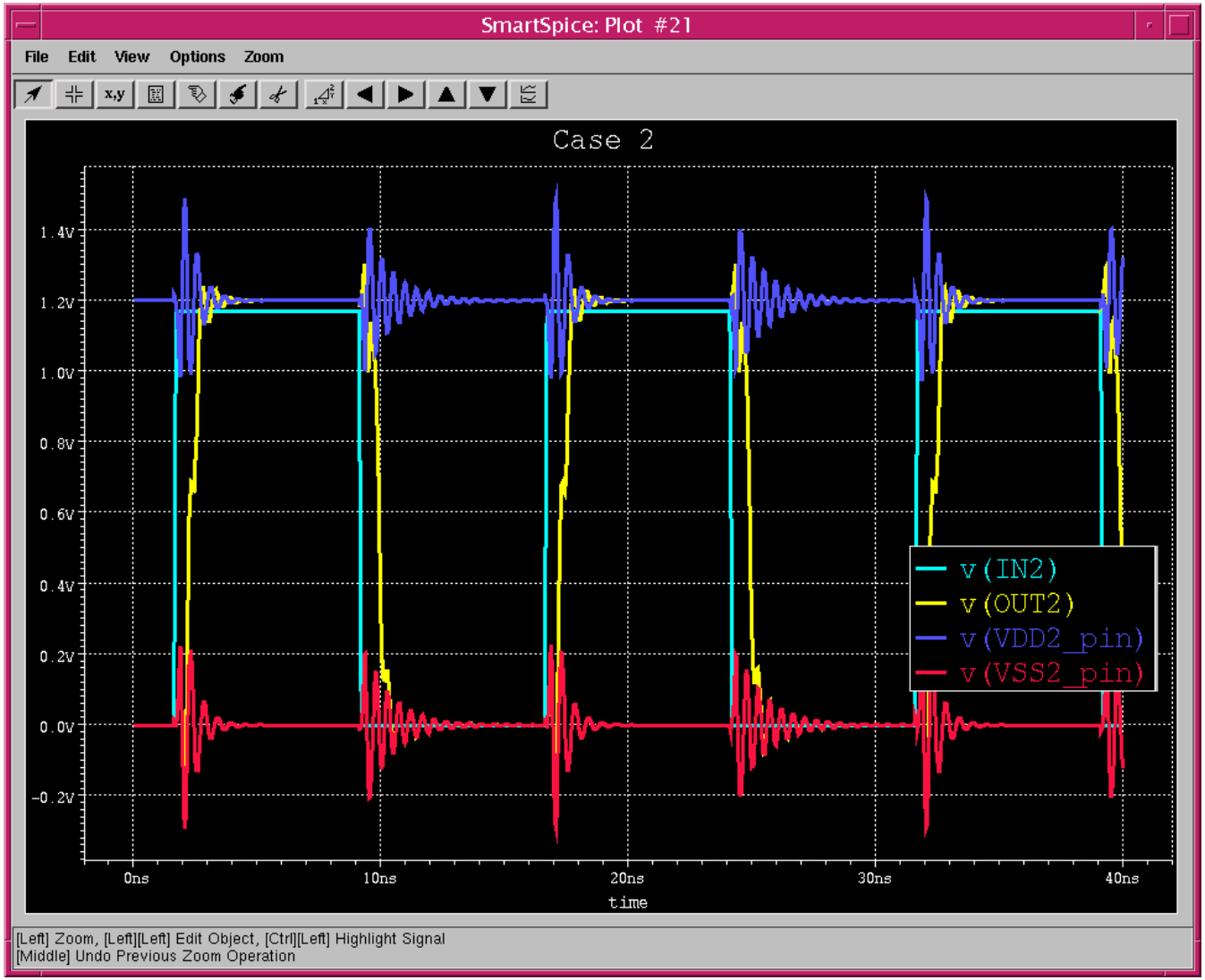
Spice Simulation Result For Case 1



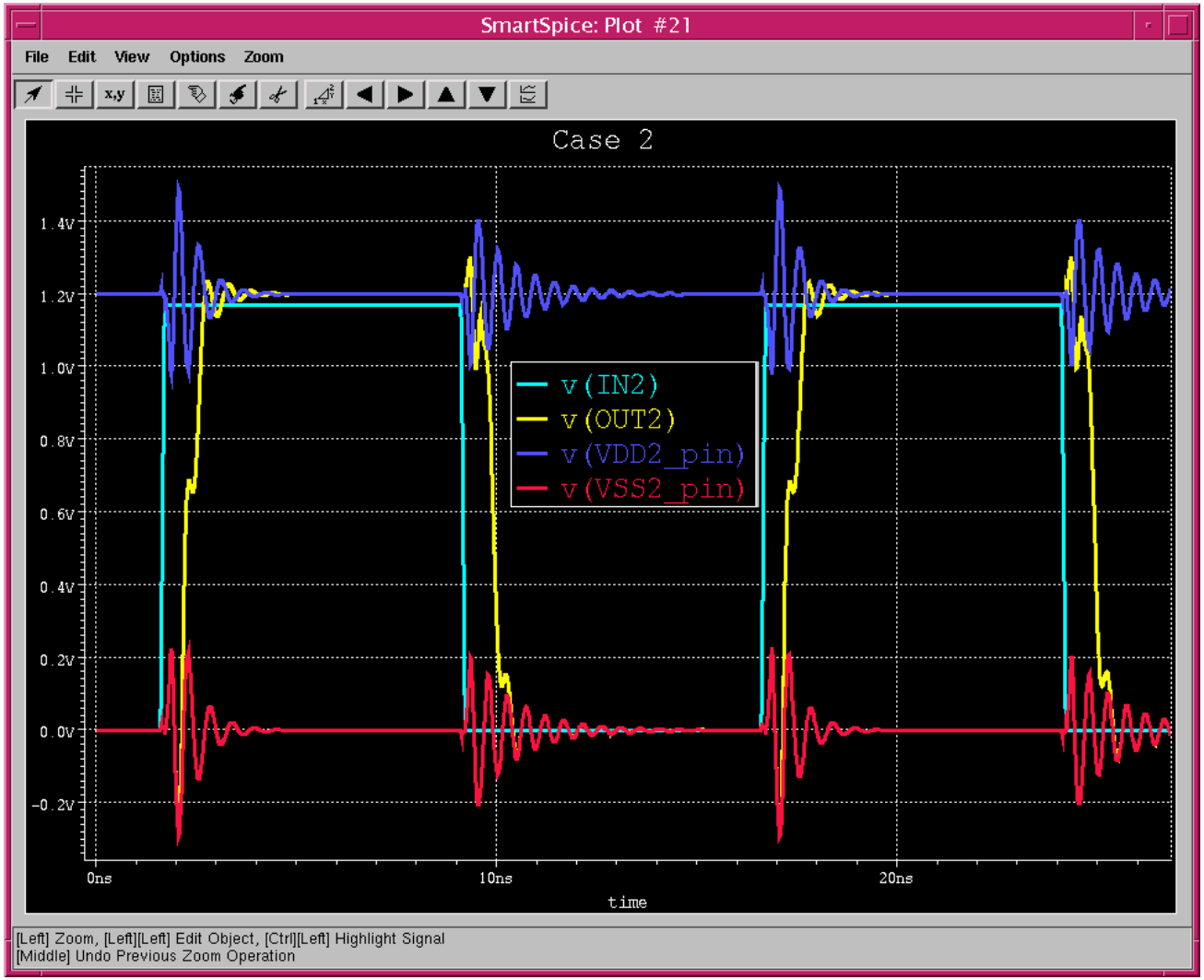
Spice Simulation Result For Case 1 (cont.)



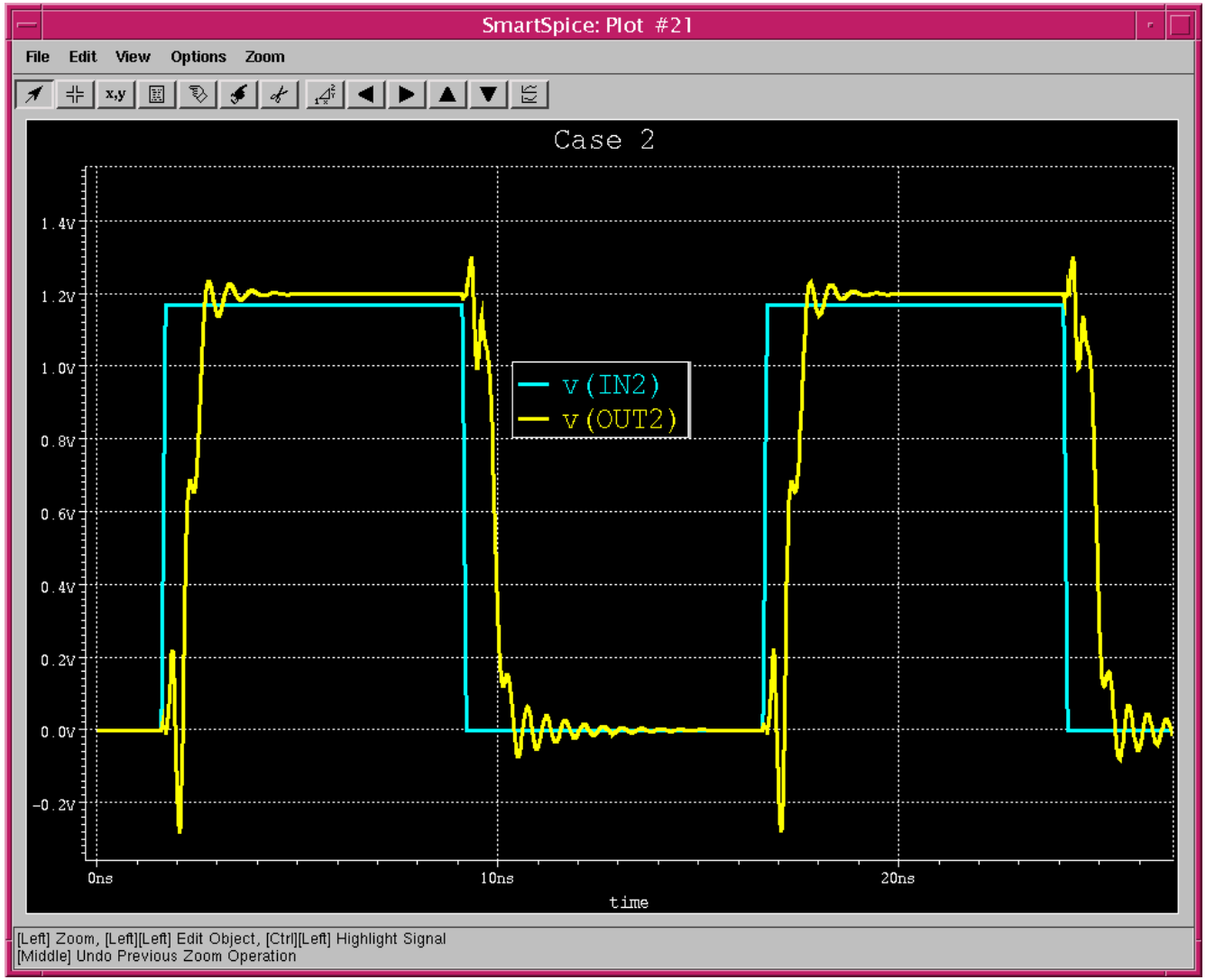
Simulation Result For Case 2



Simulation Result For Case 2 (cont.)

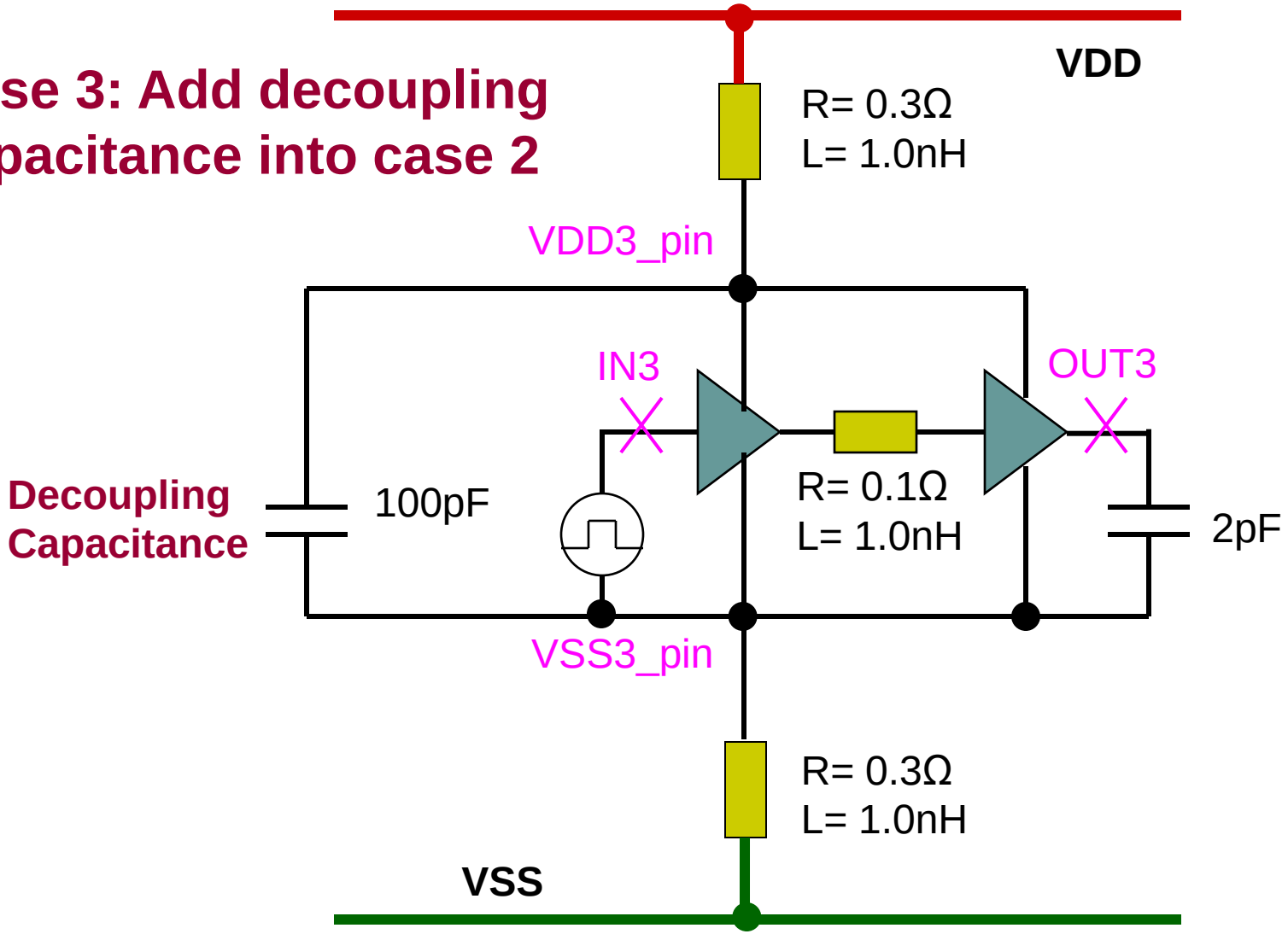


Simulation Result For Case 2 (cont.)

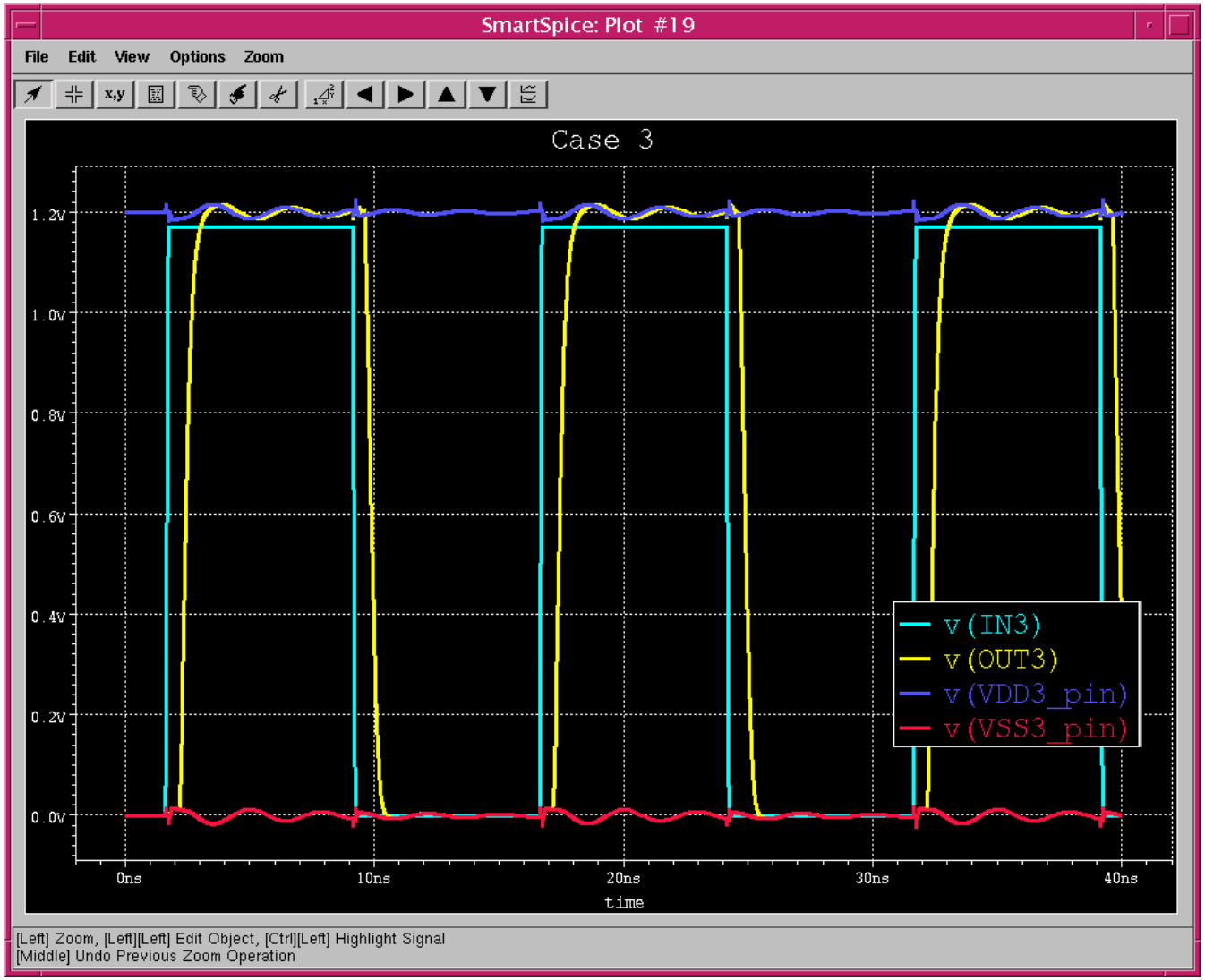


Adding By-Pass Capacitors to the Simulation

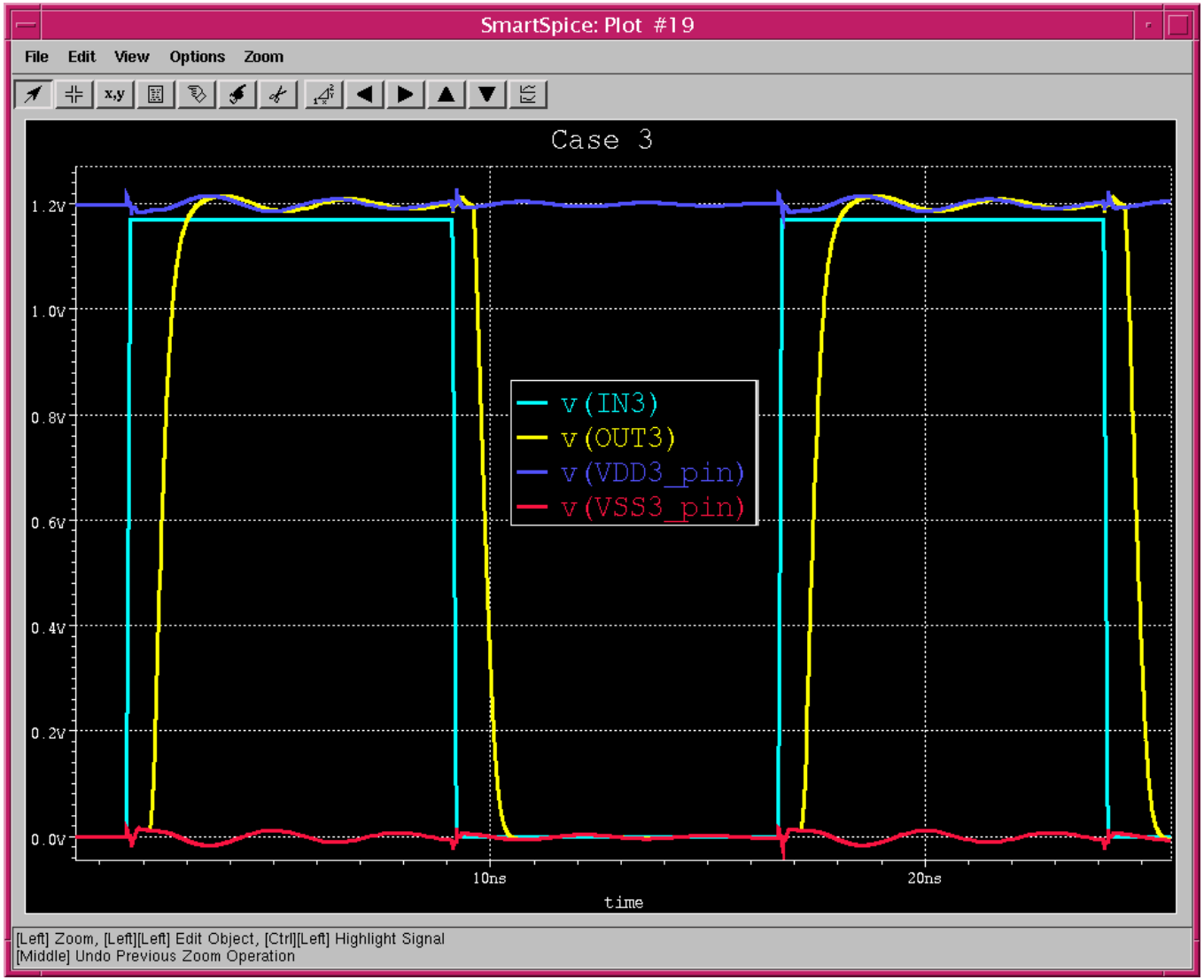
Case 3: Add decoupling capacitance into case 2



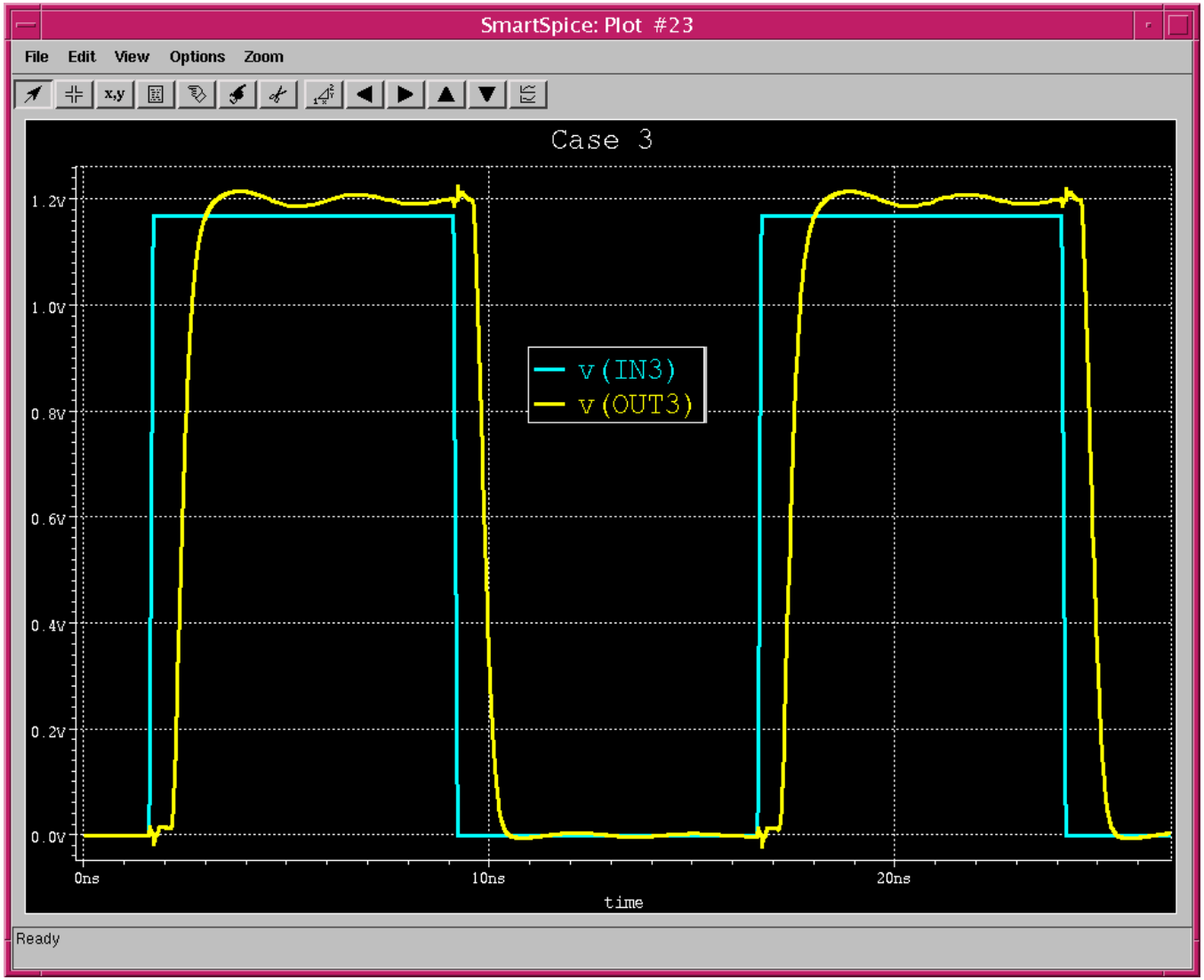
Simulation Result For Case 3



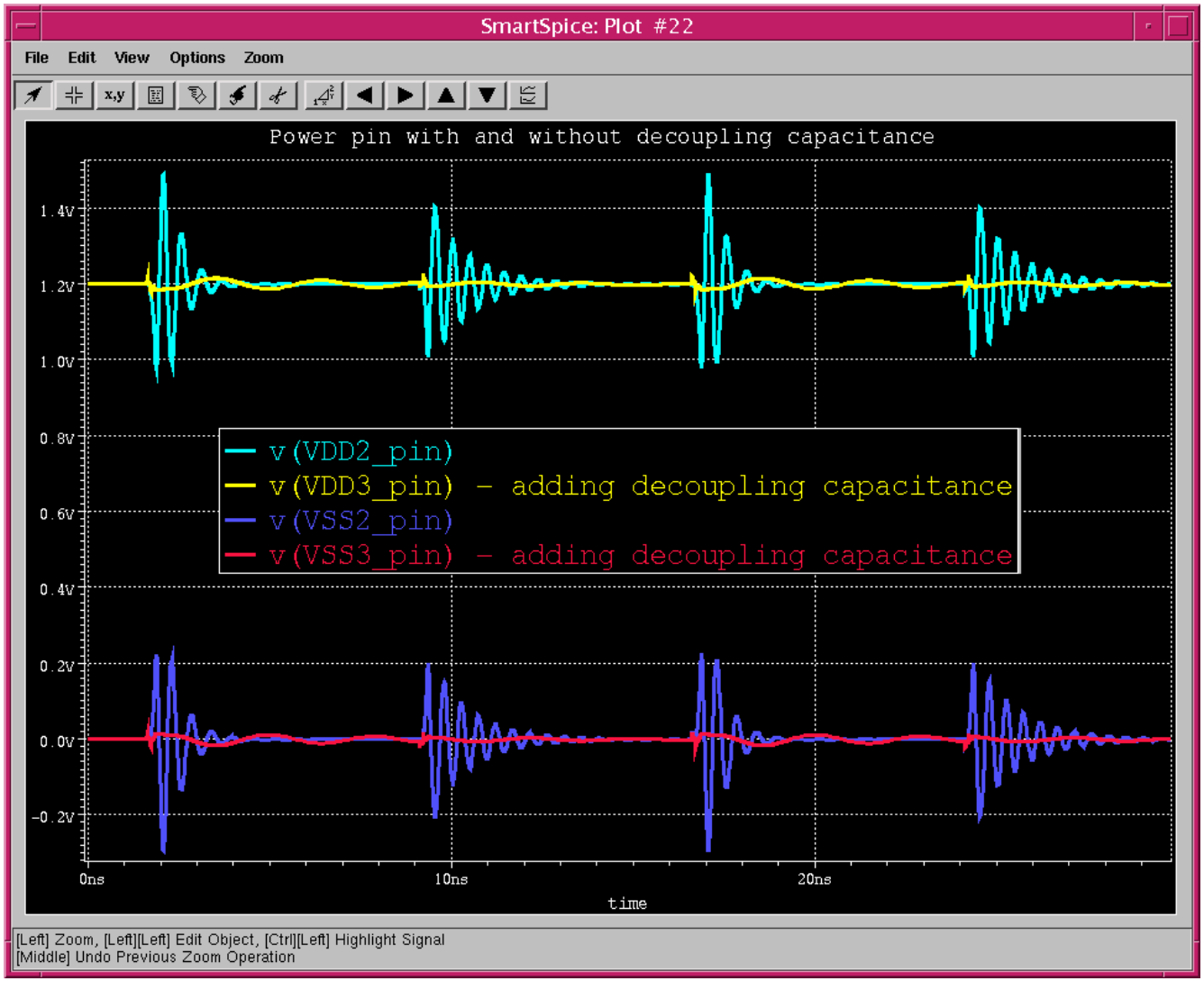
Simulation Result For Case 3 (cont.)



Simulation Result For Case 3 (cont.)

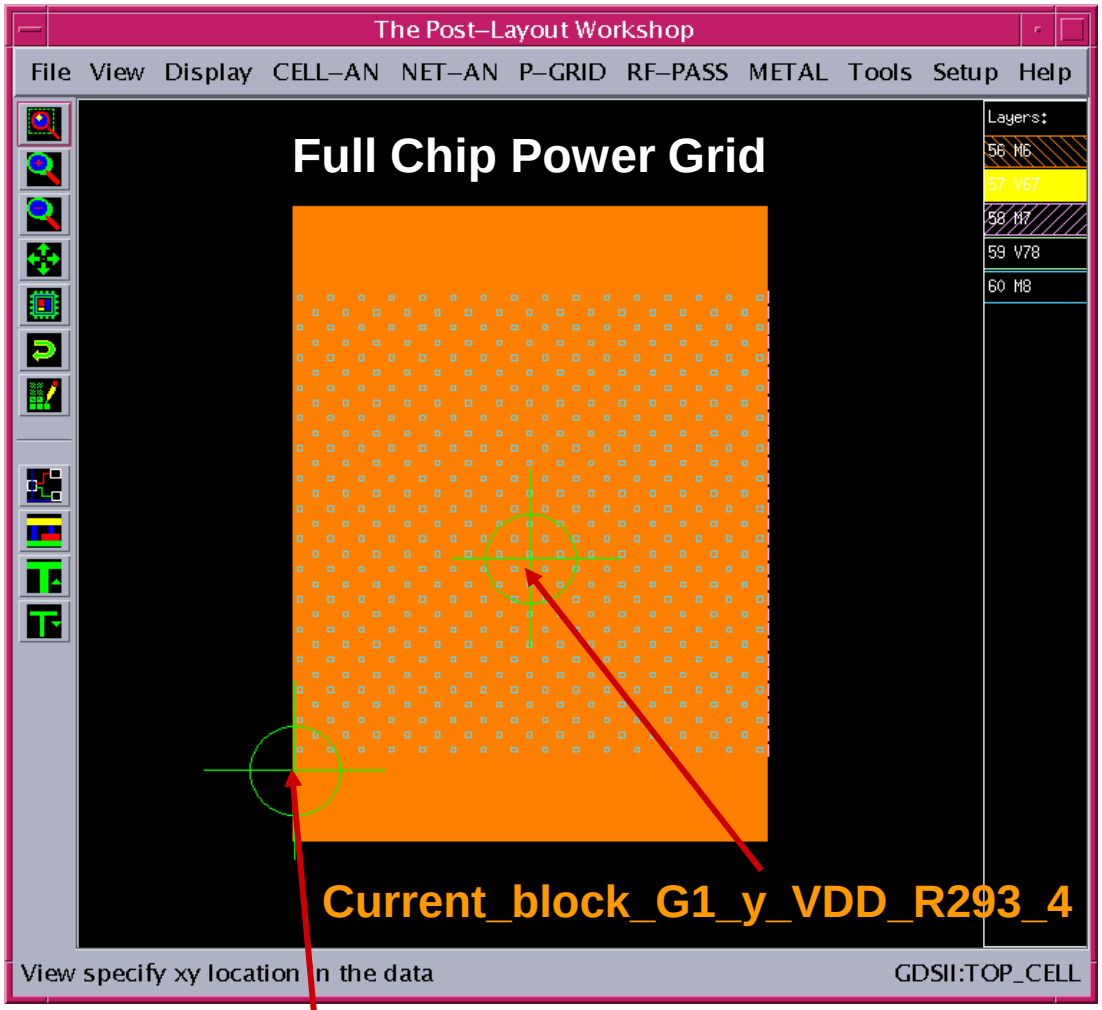


Simulation Result For Case 3 (cont.)



Test Case Power Delivery Network

Measurement Points

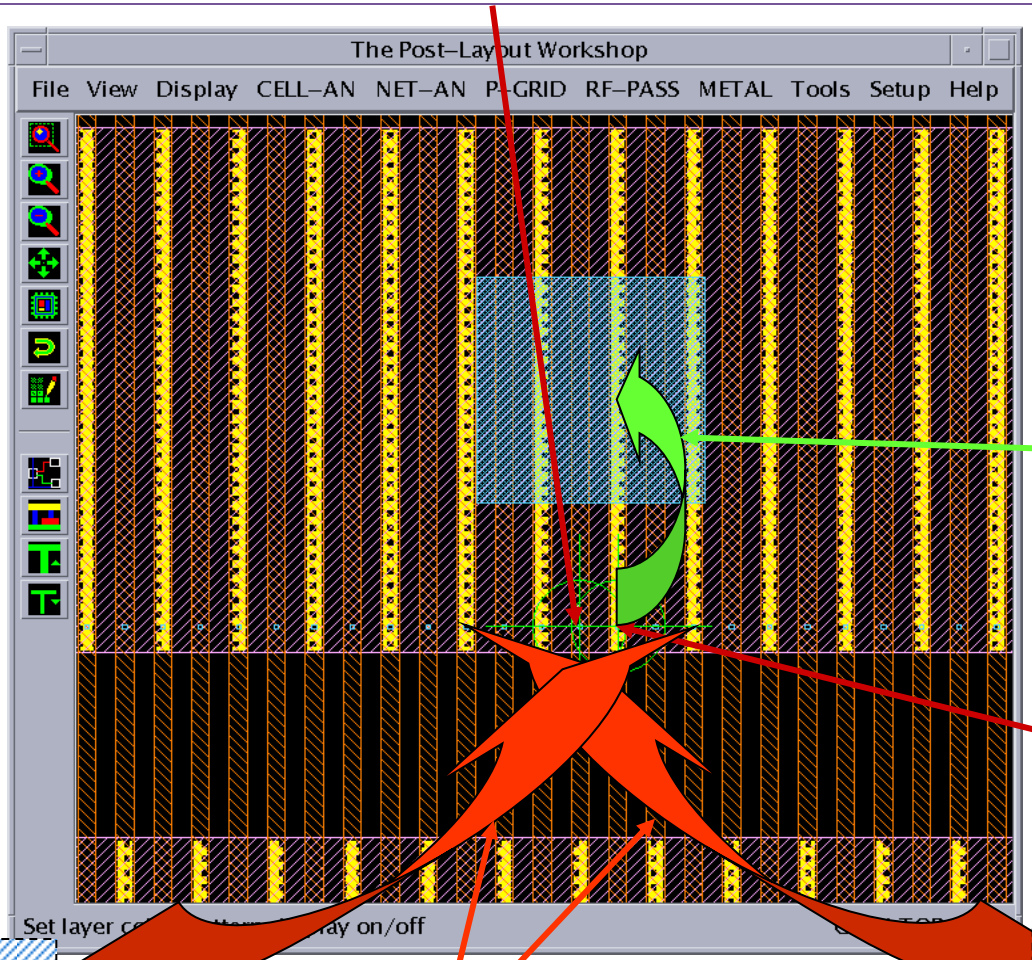


Simulation Statistics

GDSII File:	3.38 MB
3D Model File:	1.79 MB
Extraction (NET-AN) :	60.2 min.
Spice file:	48.96 MB
Resistors:	252,715
Capacitors:	3,402
Self-Inductors:	59,533
Mutual-Inductors:	801,477
Lmin:	0.21nH
Lmax:	0.52pH
Kmax:	0.76
Transient Simulation (PANTHER):	7.0 min. (234 wave-forms)
Supply Power Ports:	236
Buffer Power Ports :	16,336

Center Point Current Paths

When currents travel in the same direction the mutual inductance is not always helpful

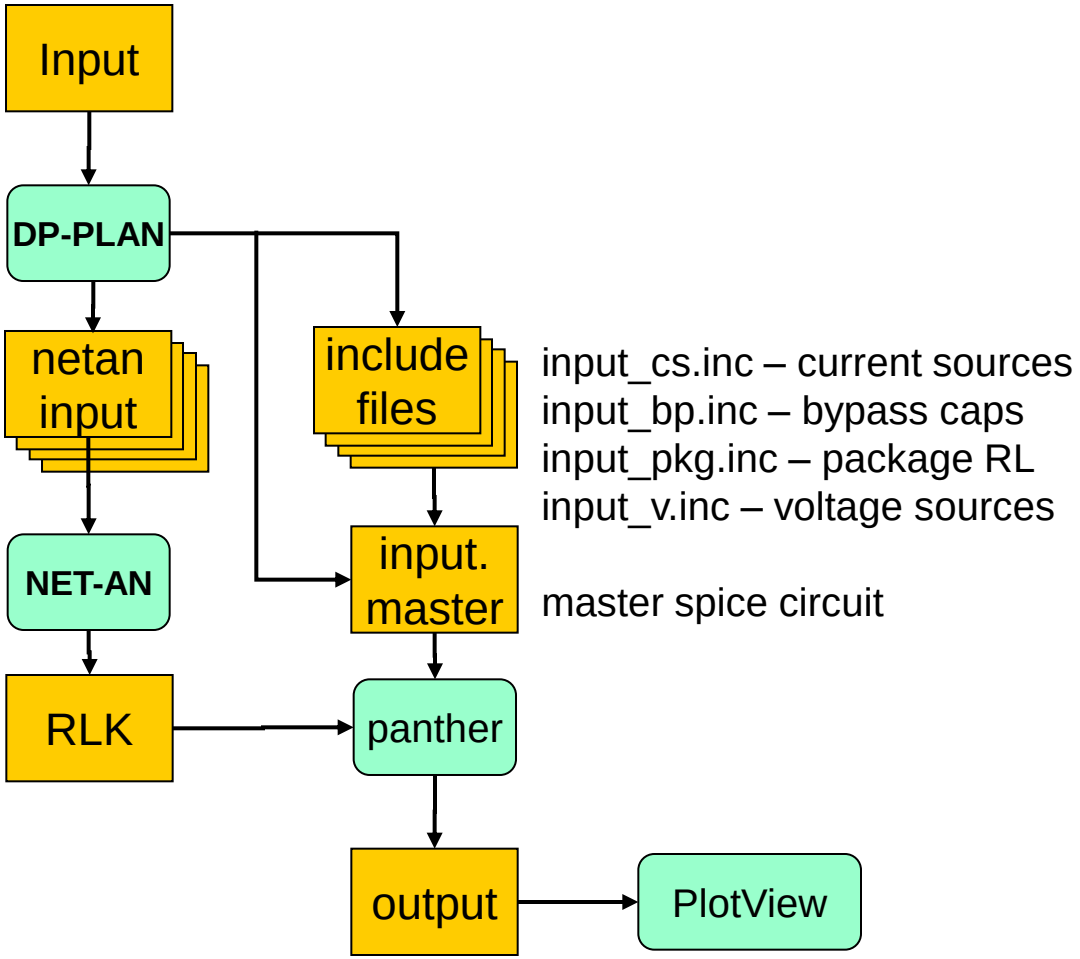


Products Used for Power Delivery Test Case

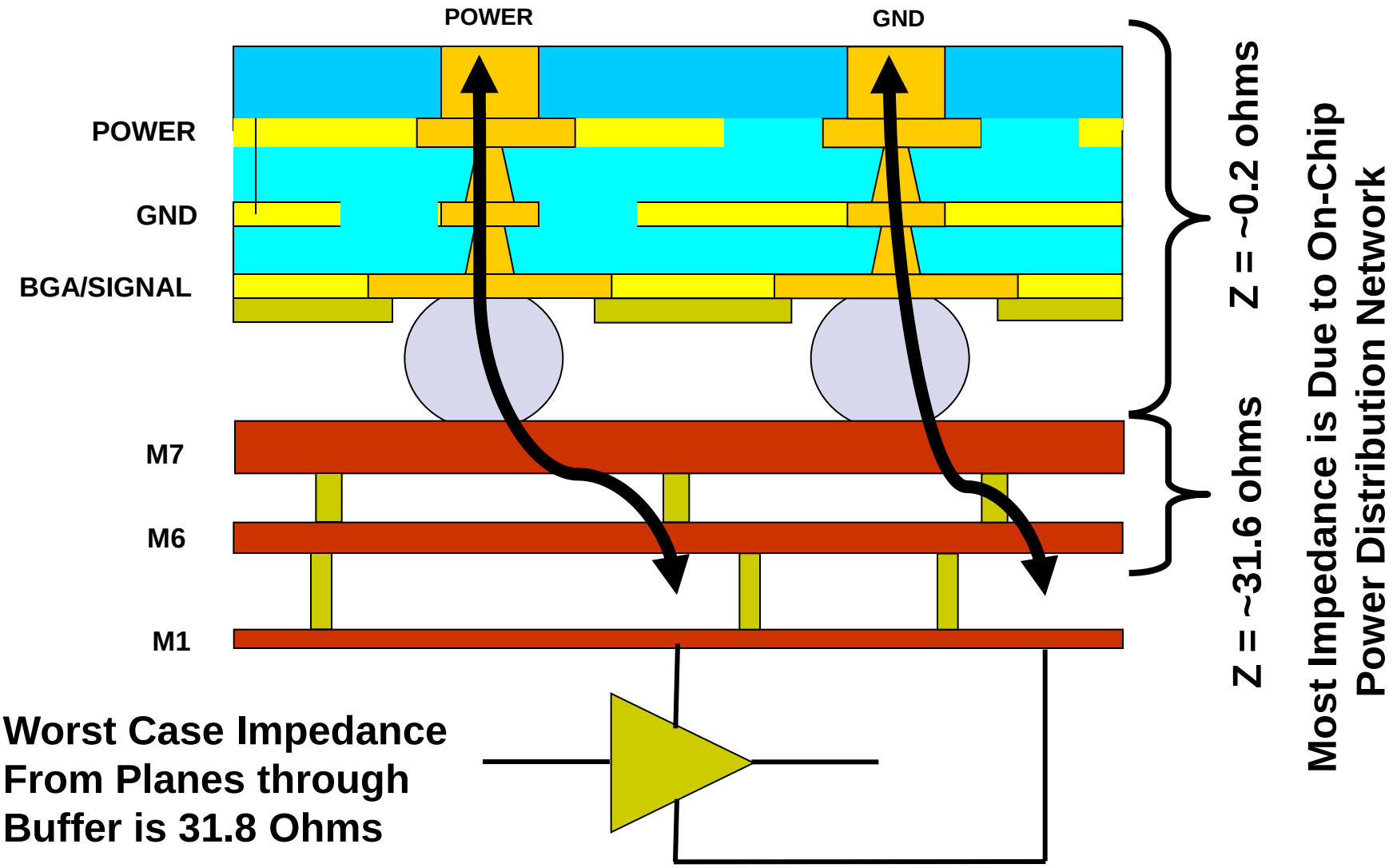
- **DP-PLAN** (OEA International)
  - Full Chip Dynamic Power Planner and Analysis Tool
  - Used to:
    - Model Existing Power Delivery Network
    - Simulate Individual Power Pin Electrical Behavior
- **NET-AN** (OEA International)
  - Critical Net Extraction and Analysis Tool
  - Used for Power Pin RCLK Effective Impedance Modeling
- Required Features/Capabilities
  - Real Physical Interconnect Modeling
    - Full 3D Extraction Delivers RCLK Impedance Model – Especially K!
  - Full-Chip, Very Fast, Very Accurate Signal Integrity Analysis
    - Able to Simulate Gigantic Interconnect RCLK Model

Dynamic Power Plan Analysis Flow

Using General Data Provided on Chip Rails and Package Construction



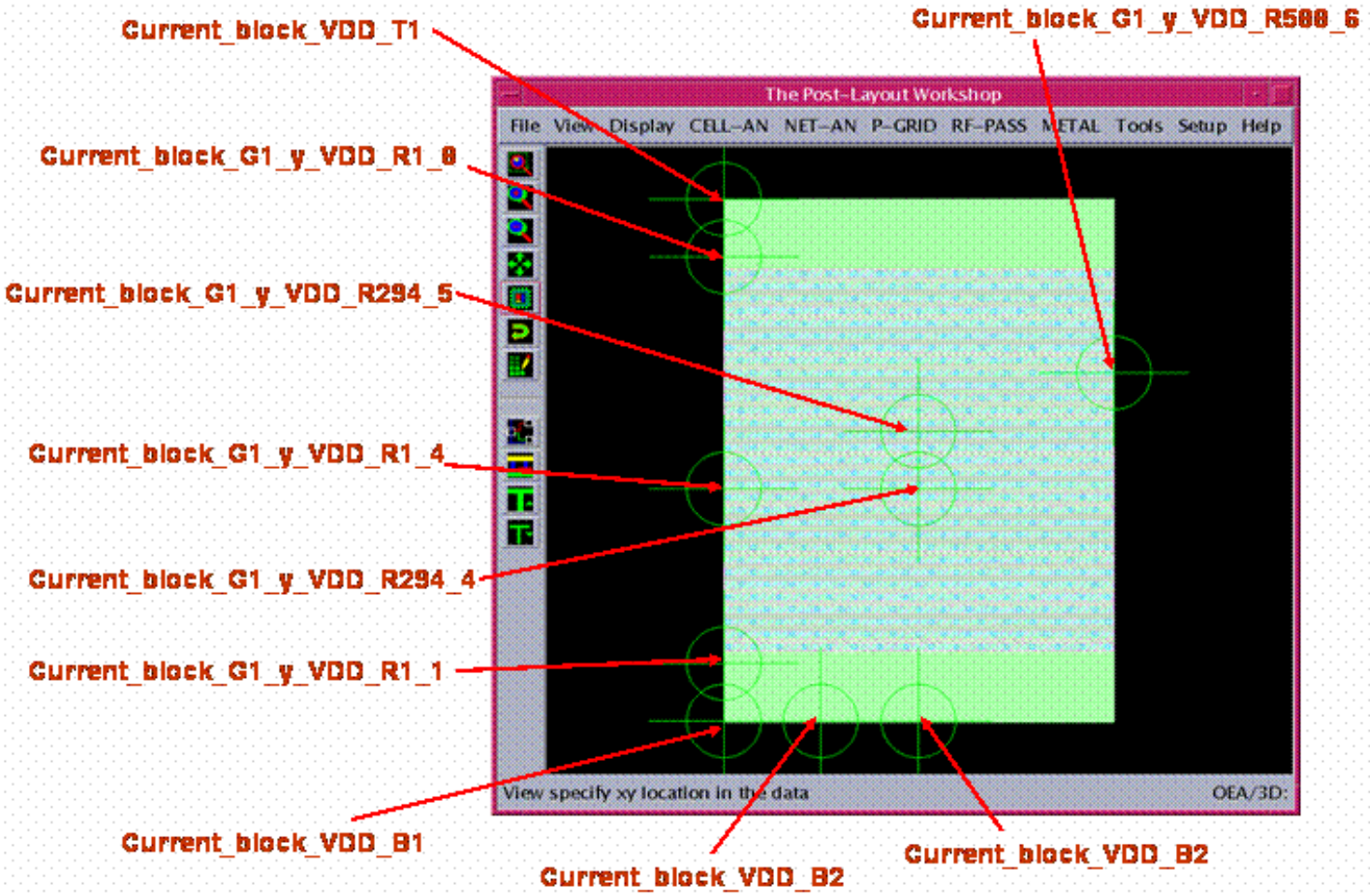
Impedance Illustration



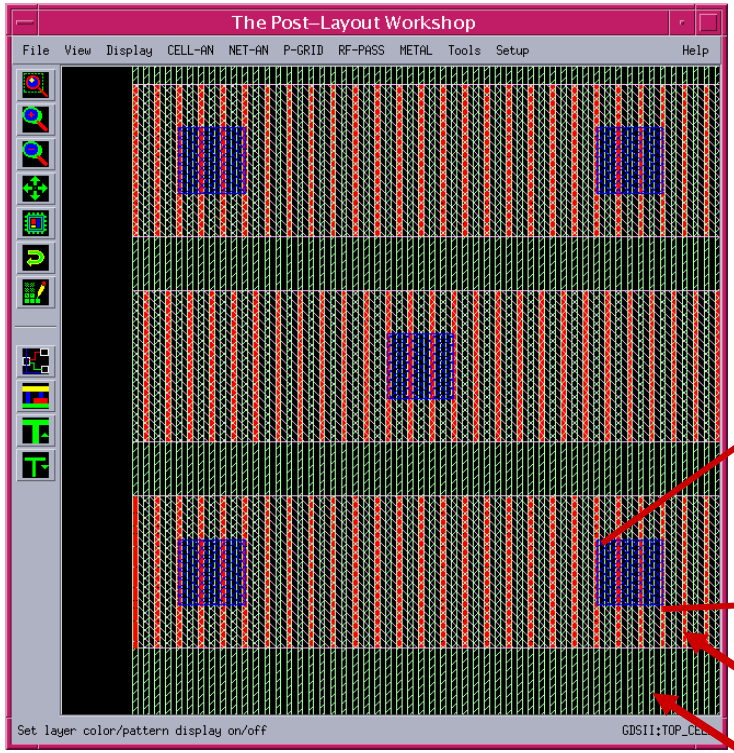
Worst Case Impedance From Planes through Buffer is 31.8 Ohms

Test Case Power Delivery Network

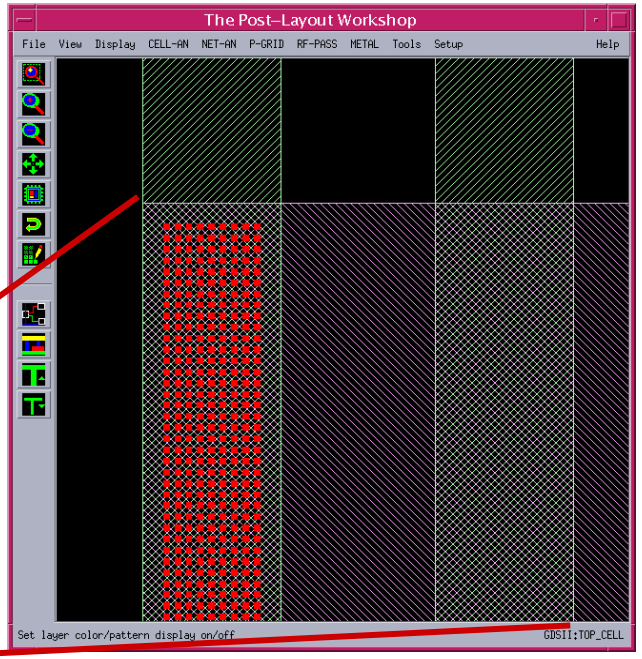
Measurement Points



Power Delivery Network Model
Accurate Physical Modeling



Real Physical Dimensions & Metal Layer Electrical Characteristics



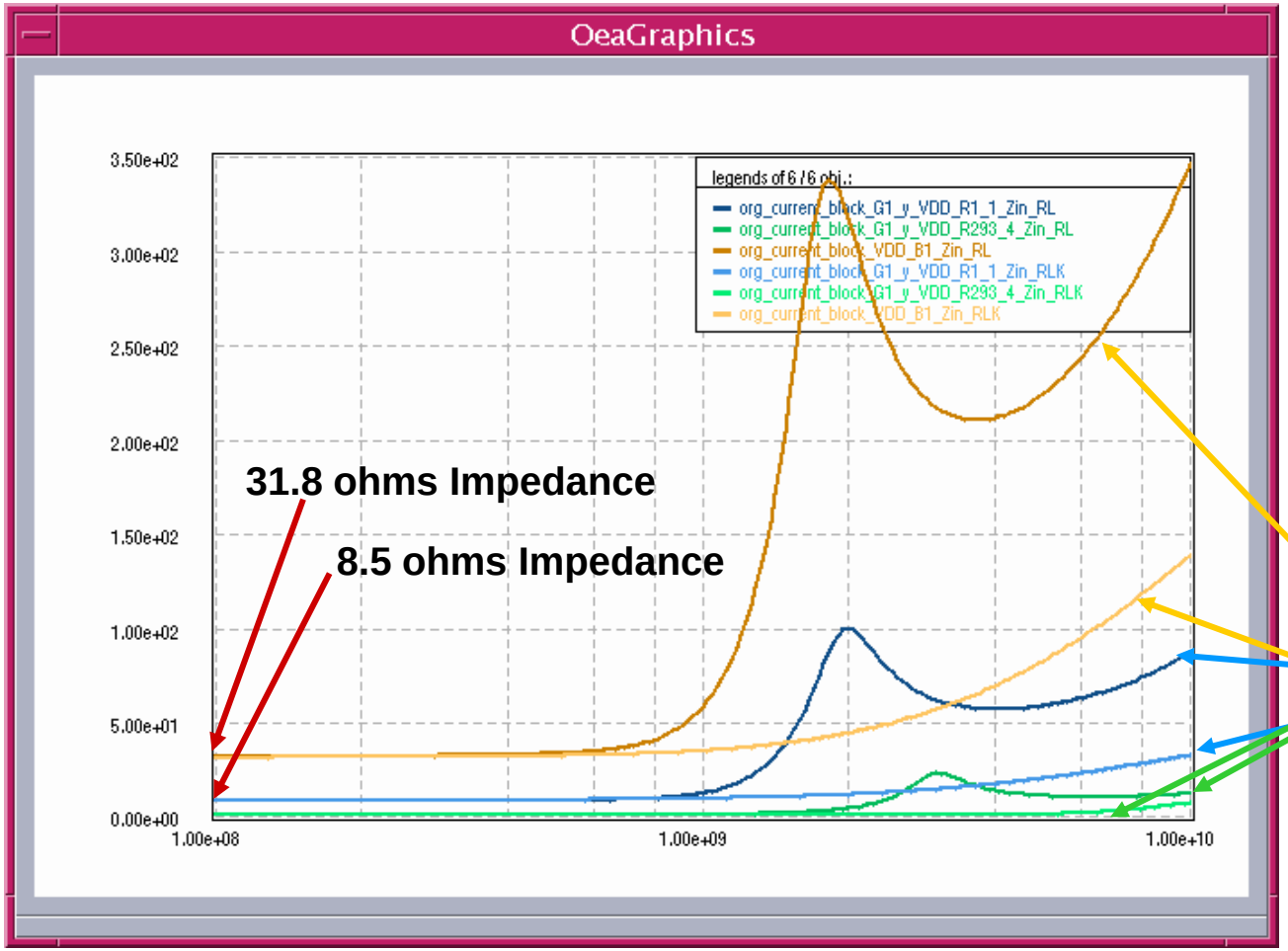
Automatic Via Array Generation

M7 232.5um Horizontal Stripes @ Bump Pitch

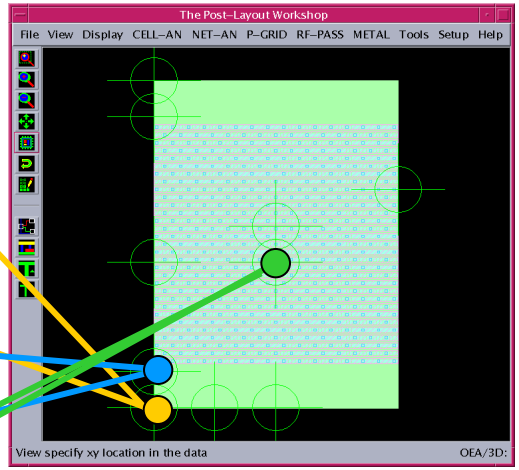
M6 7.82um Vertical Stripes @ 33.12um Pitch

(not shown M1 0.5um Horizontal Stripes @ 3.69um Pitch)

Selected Power Pin Simulations

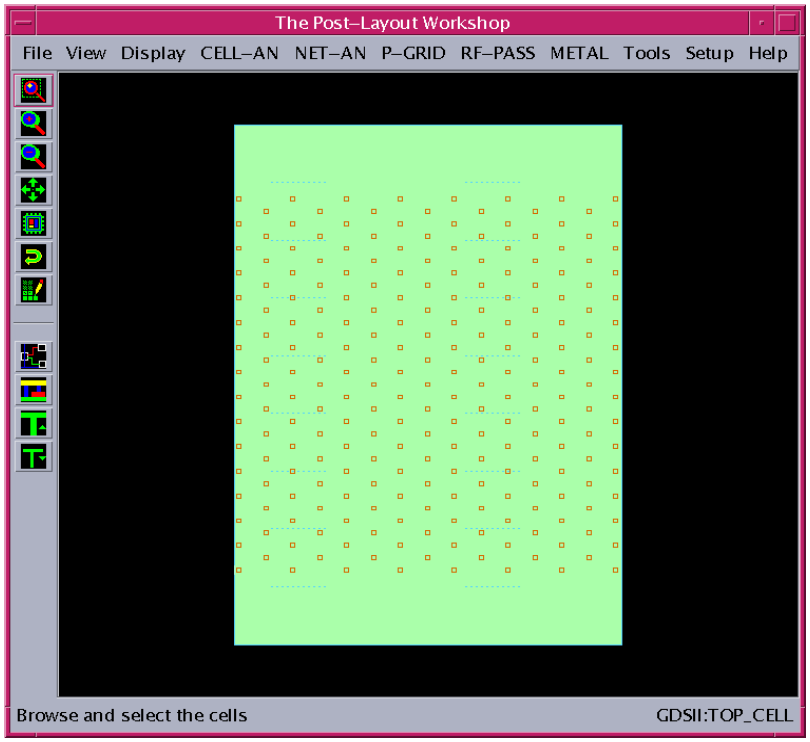


Simulated Area without M1



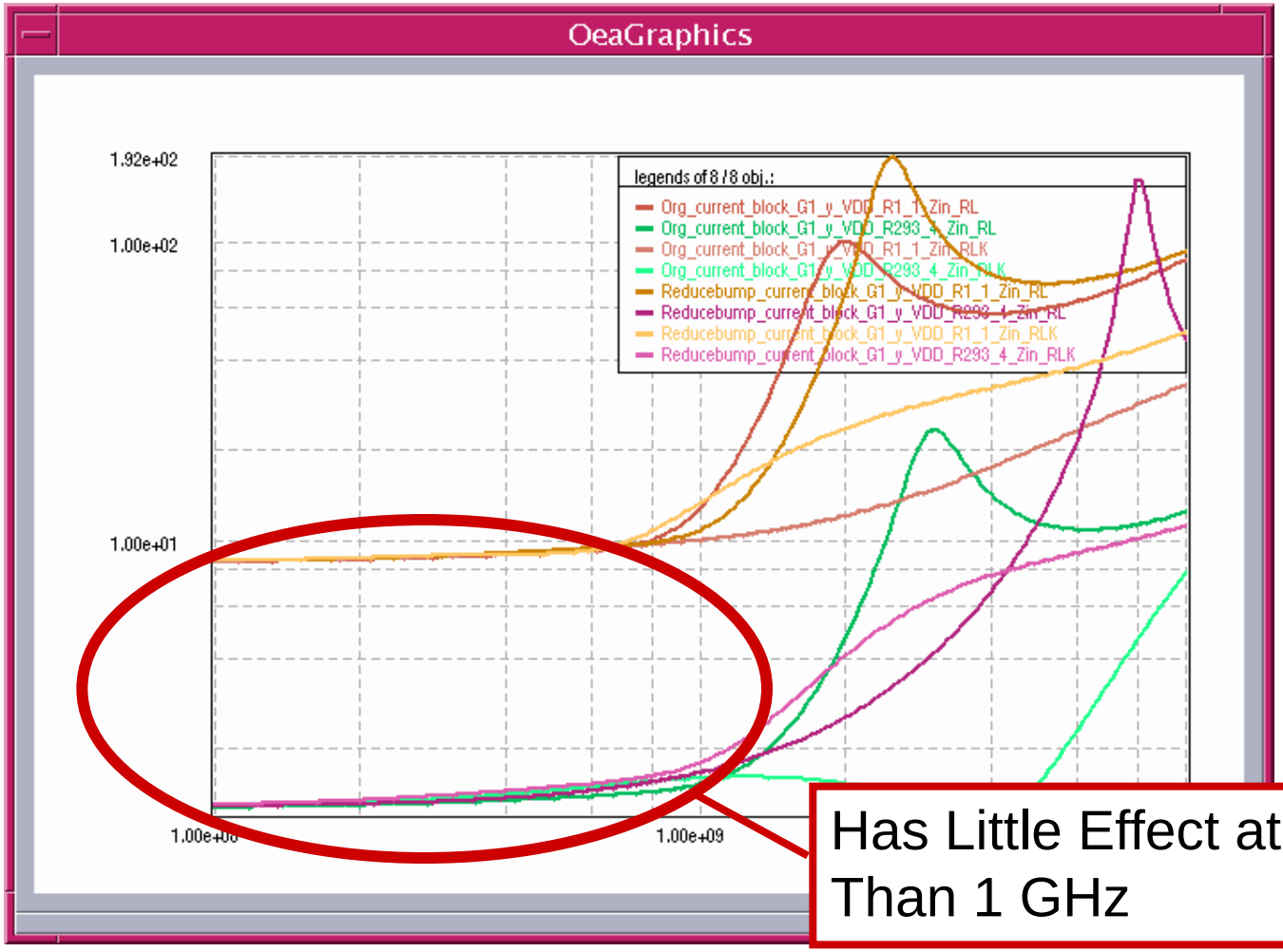
Experiment with Reduced Power Bumps to See if it is Significant

- Package/Bump Power Delivery Network is Adequate
- Reduce Power Pin Count
  - Has Little Effect on Effective Impedance
  - Removal of Pins May Reduce Package Cost or Allow Internal Connections



Reduced Power Bumps to Half of Original

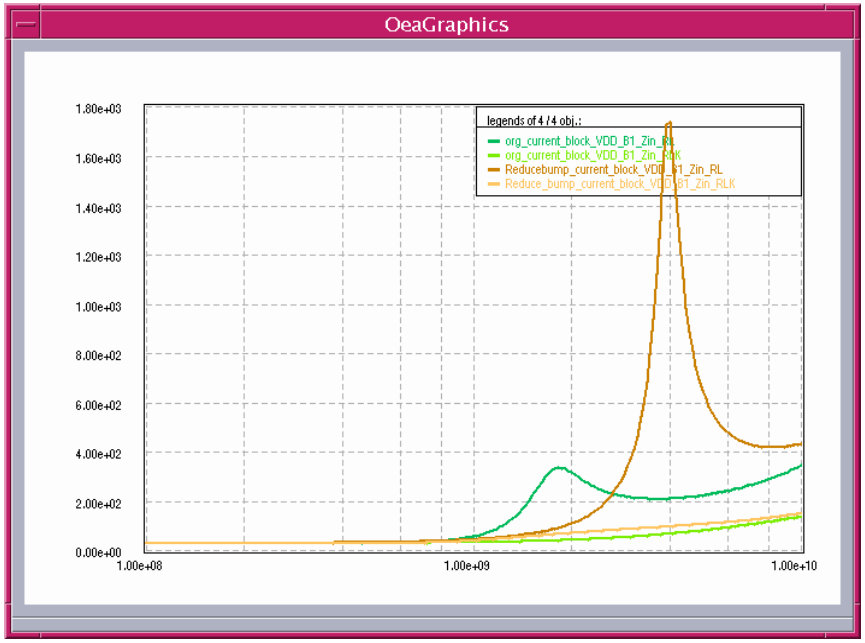
Original Pin Count vs Reduced Bumps Comparison



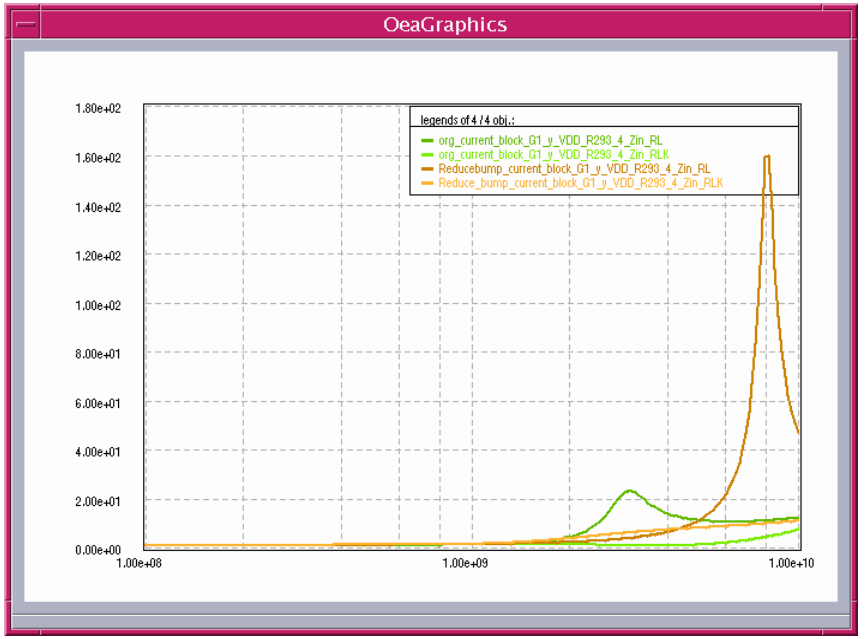
Has Little Effect at Less Than 1 GHz

Reduced Power Pin Out

Similar Electrical Performance < 1 GHz

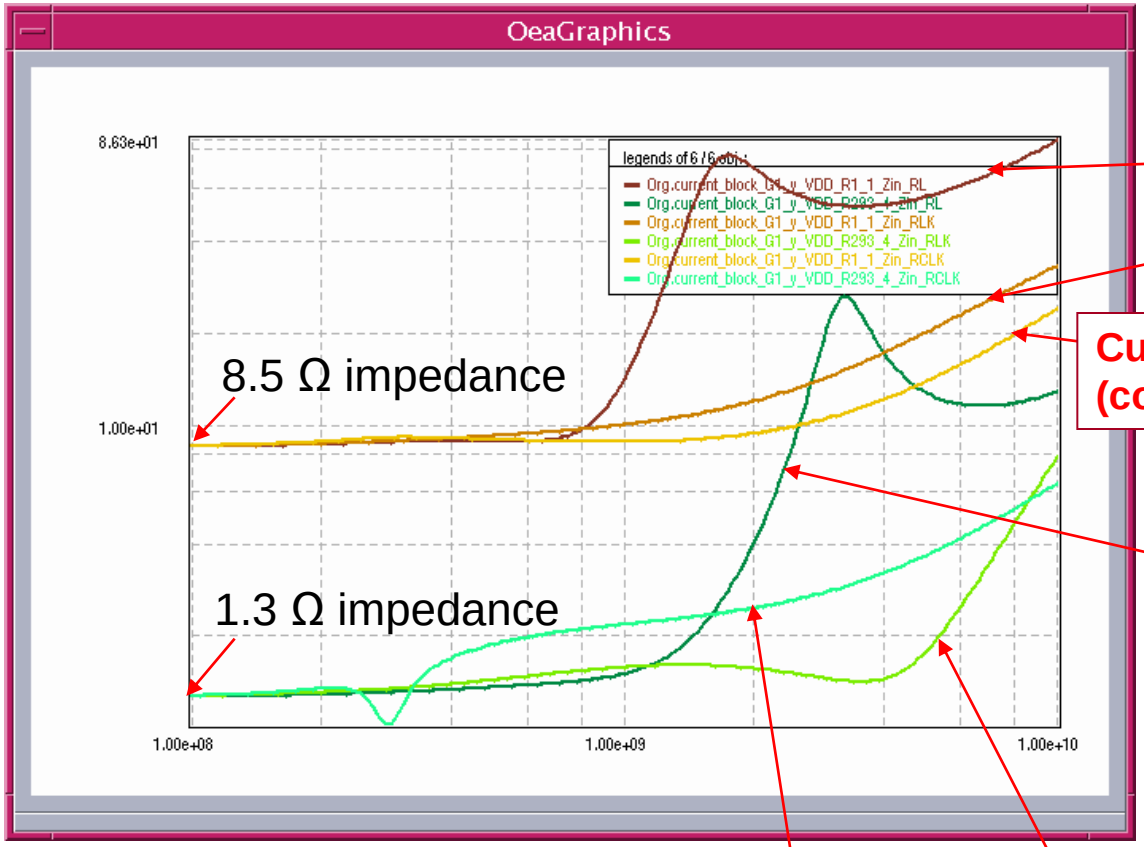


Vdd_B1_node
Lower Left-Hand Corner



Vdd_R293_4_node
Chip Center

Supplying 30.30 nF Bypass Capacitance
Evenly Distributed On The Whole Power Network



Current_block_G1_y_VDD_R1_1_RL

Current_block_G1_y_VDD_R1_1_RLK

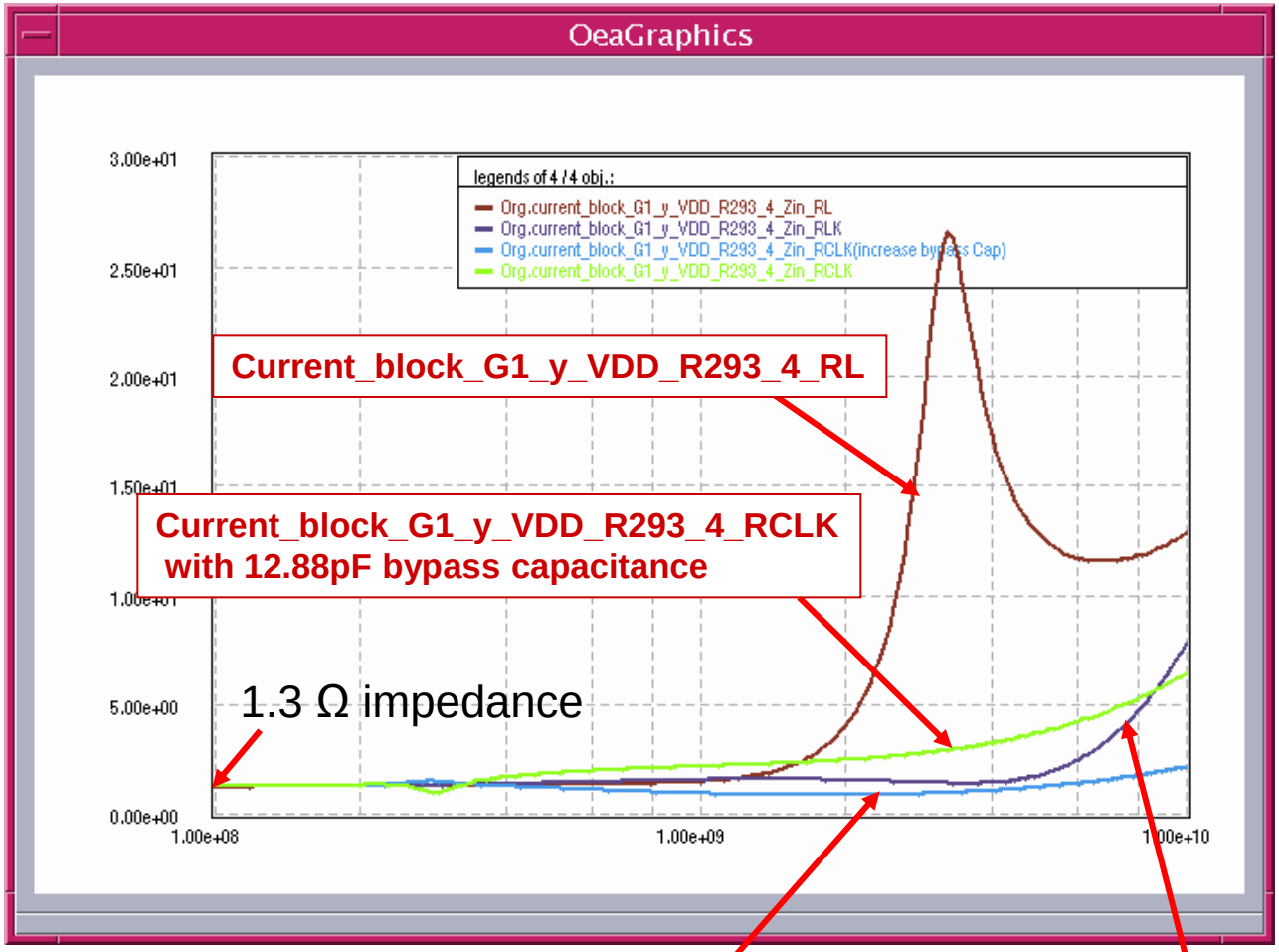
Current_block_G1_y_VDD_R1_1_RCLK (correct waveform)

Current_block_G1_y_VDD_R293_4_RL

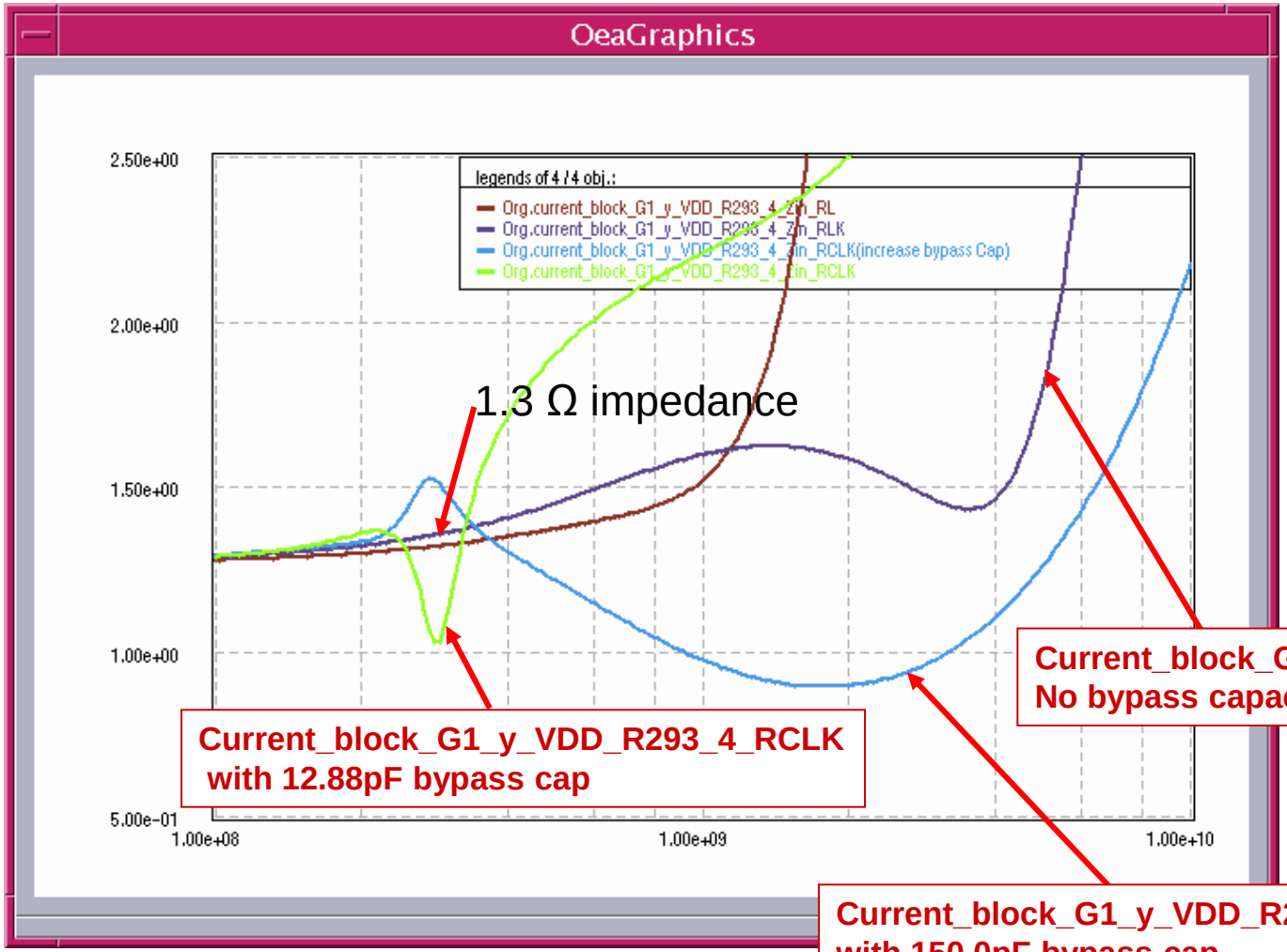
Current_block_G1_y_VDD_R293_4_RCLK (correct waveform)

Current_block_G1_y_VDD_R293_4_RLK

Increasing Bypass Capacitance On Node Current_block_G1_y_VDD_R293_4

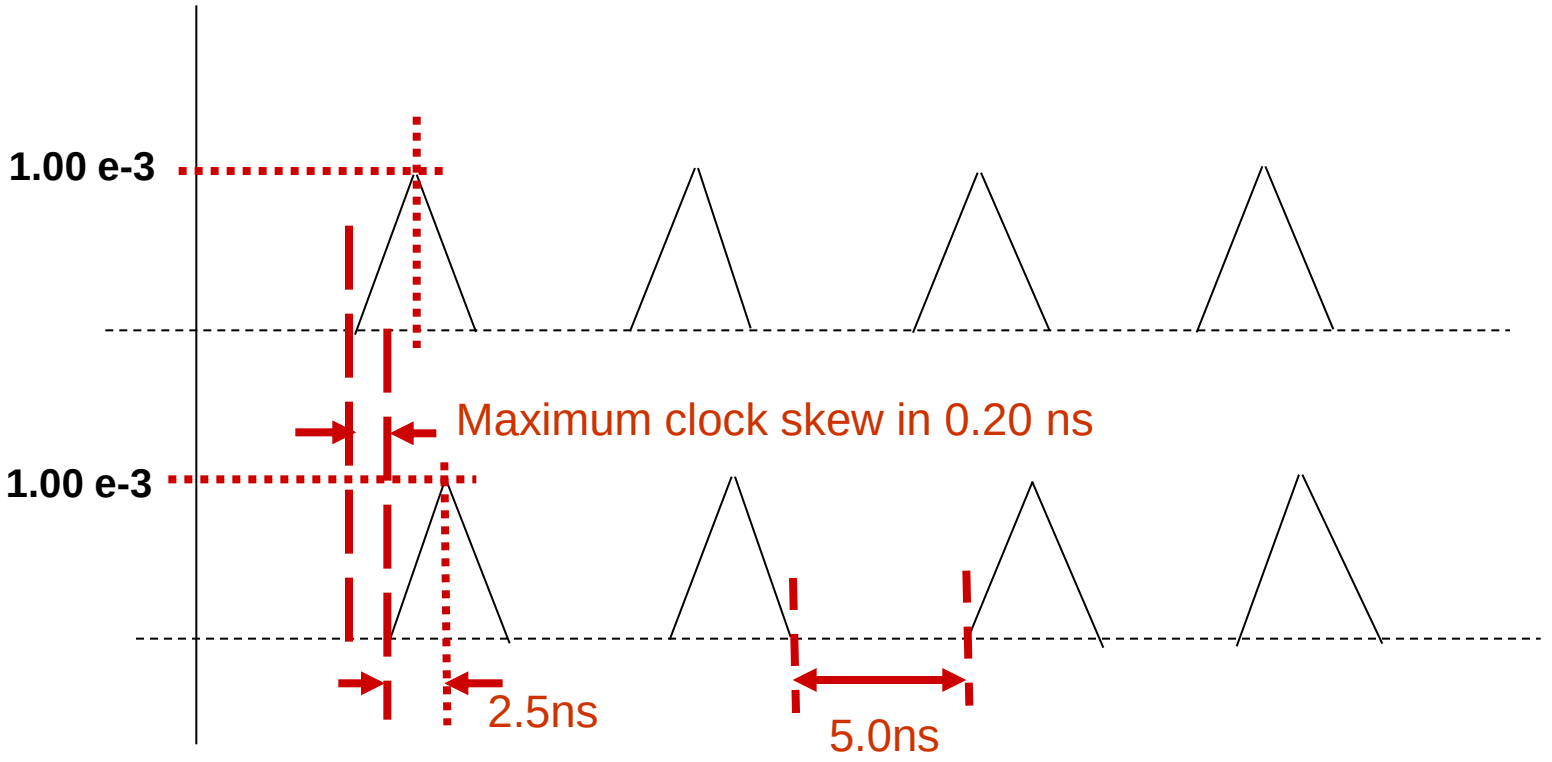


Increasing Bypass Capacitance On Node
Current_block_G1_y_VDD_R293_4 (cnt.)



Current Profile Used

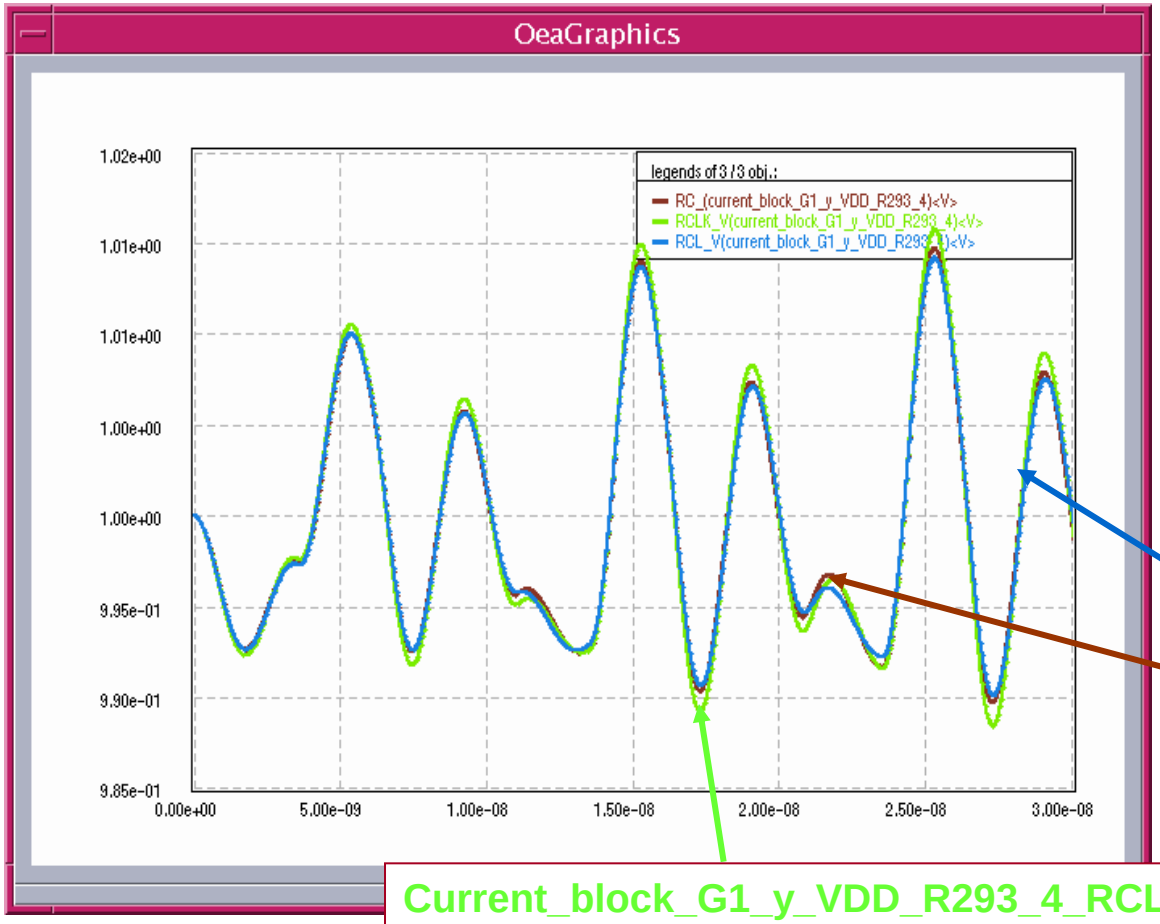
Assuming Each Transistor Drawing 1.0 mA

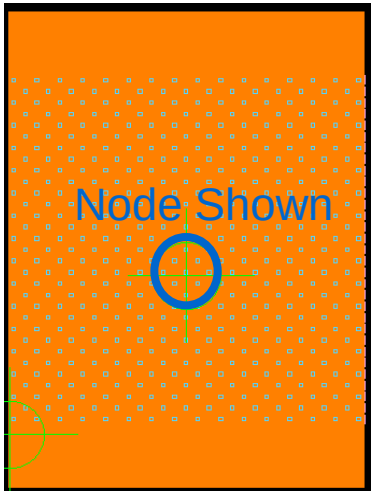


Total number of current source contact VDD/VSS = 2352

Transient Simulation Plot for VDD nodes

Supplying 30.30 nF Bypass Capacitance





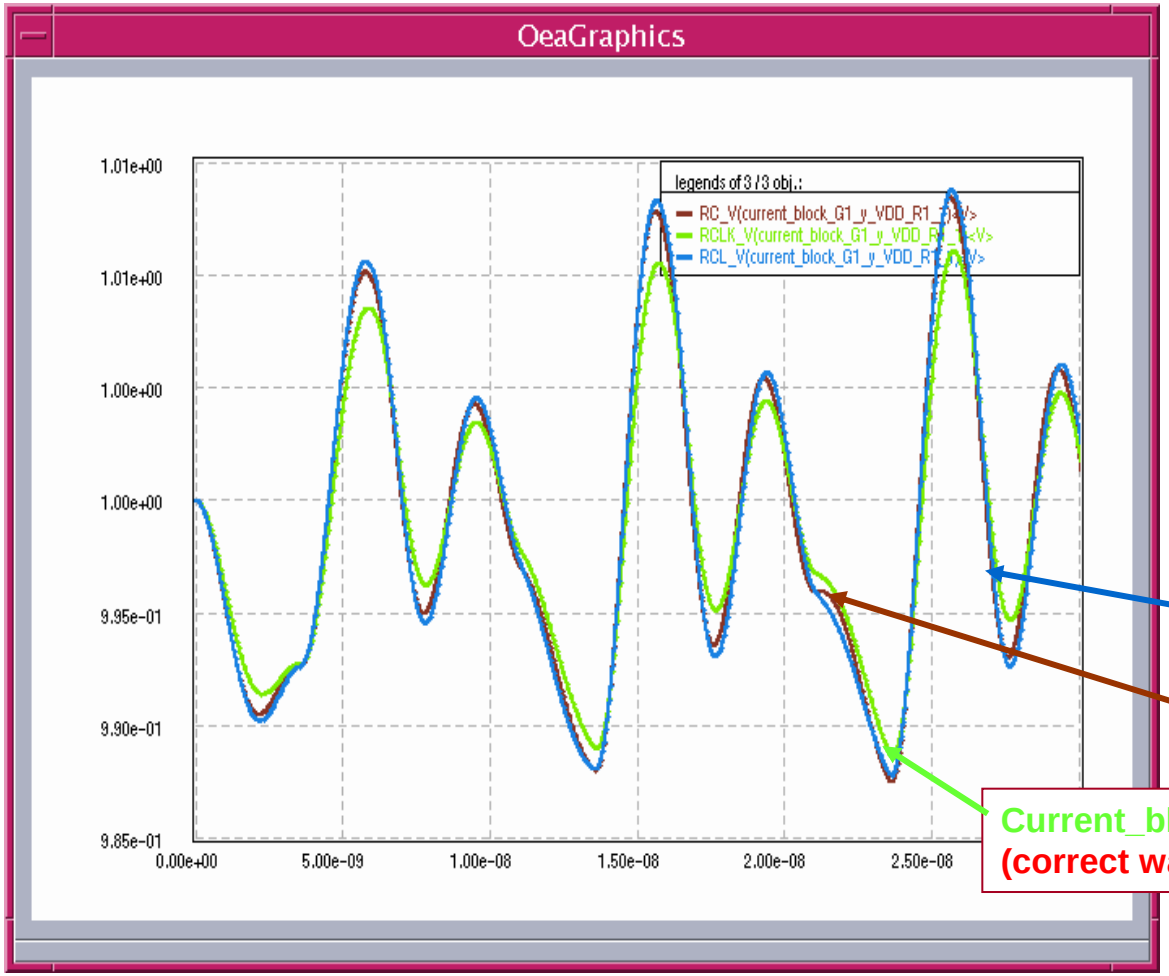
Current_block_G1_y_VDD_R293_4_RCL

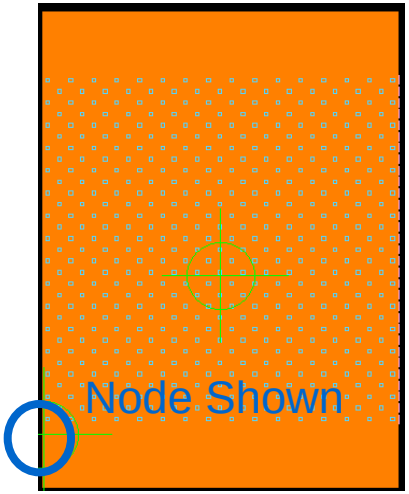
Current_block_G1_y_VDD_R293_4_RC

Current_block_G1_y_VDD_R293_4_RCLK
(correct waveform)

Transient Simulation Plot for VDD nodes

Supplying 30.30 nF Bypass Capacitance





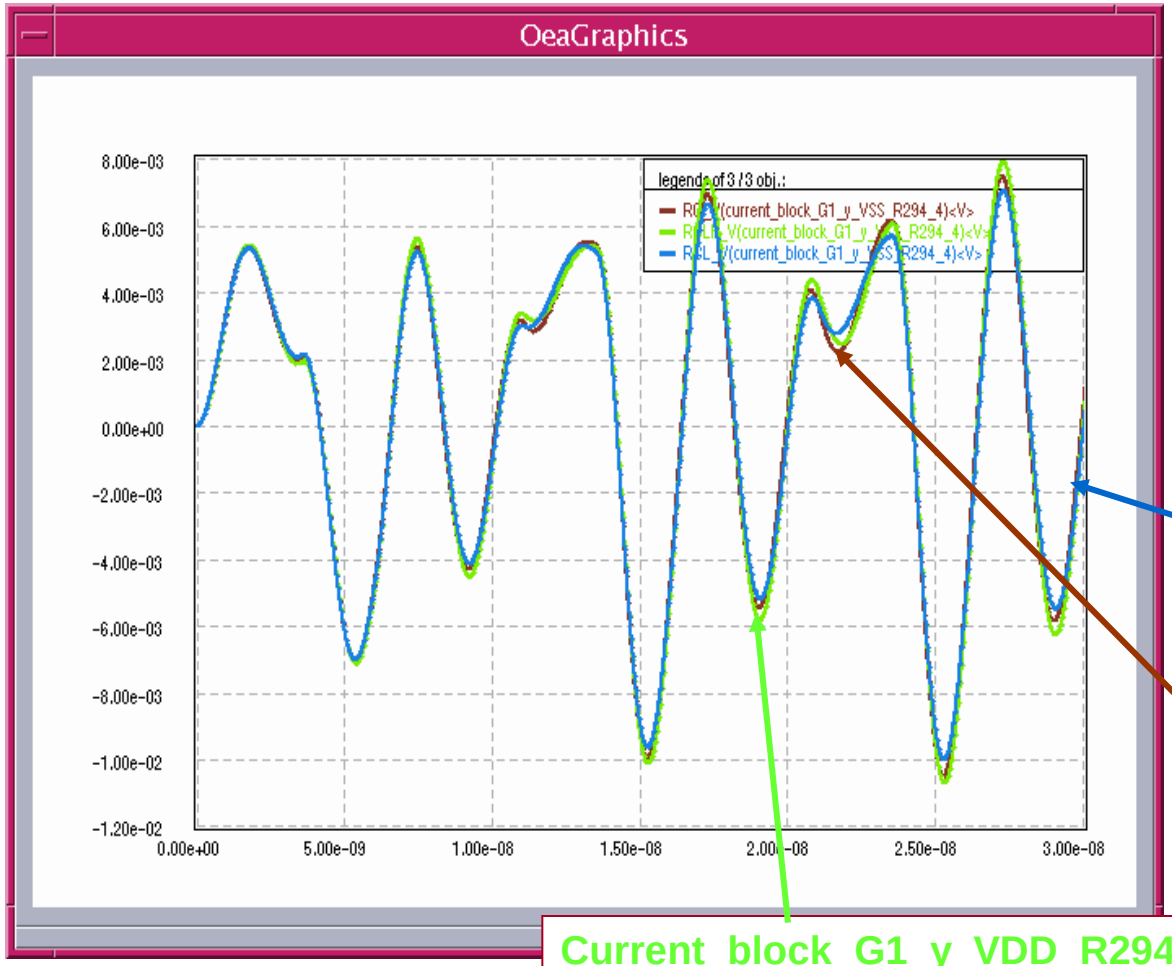
Current_block_G1_y_VDD_R1_1_RCL

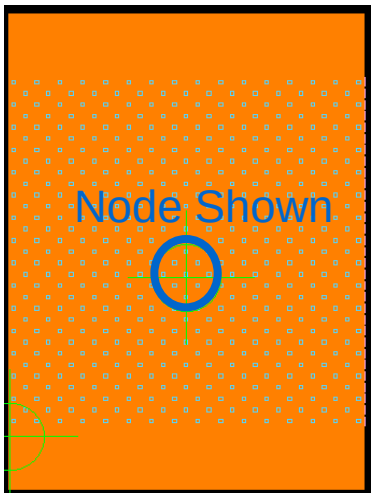
Current_block_G1_y_VDD_R1_1_RC

Current_block_G1_y_VDD_R1_1_RCLK
(correct waveform)

Transient Simulation Plot for VSS nodes

Supplying 30.30 nF Bypass Capacitance





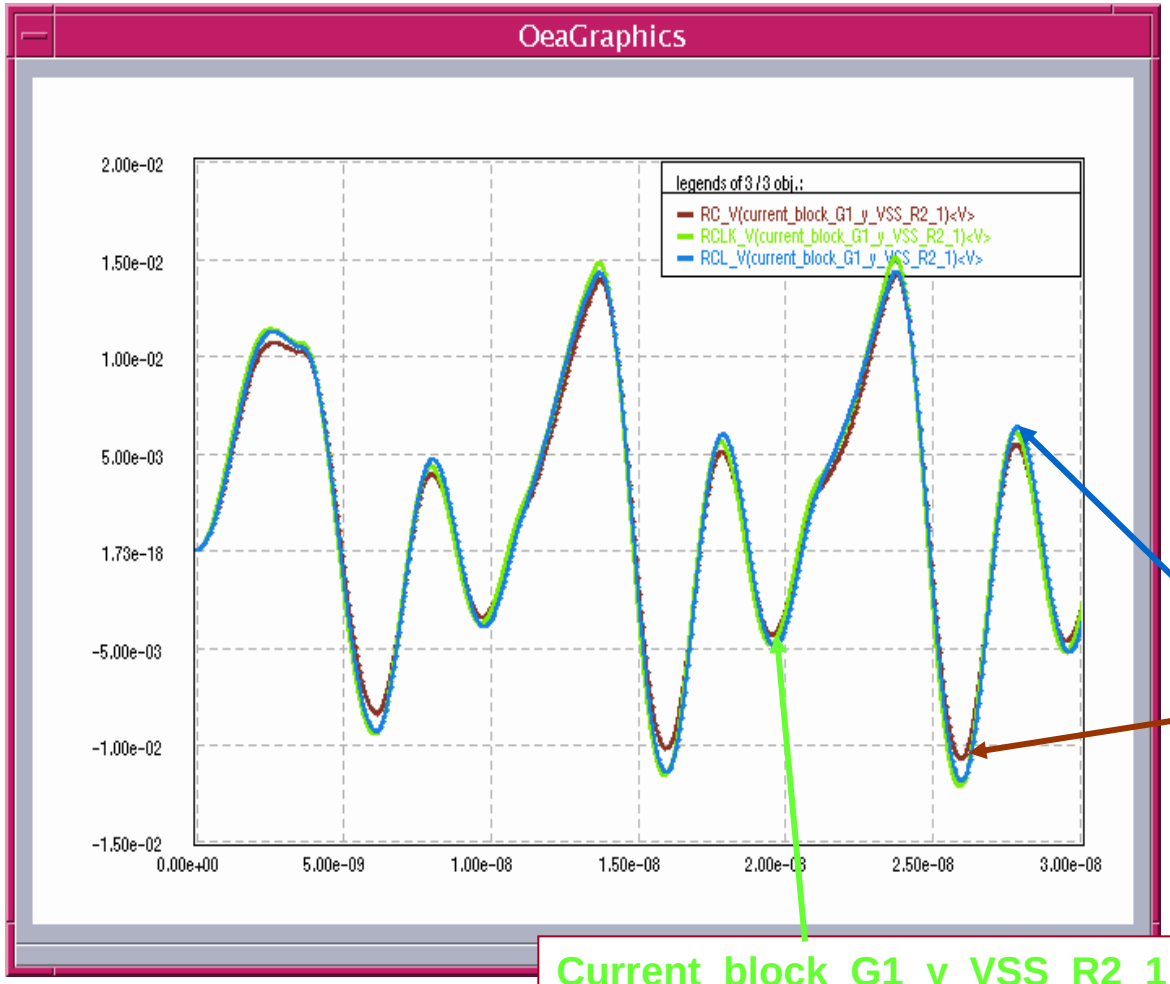
Current_block_G1_y_VDD_R294_4_RCL

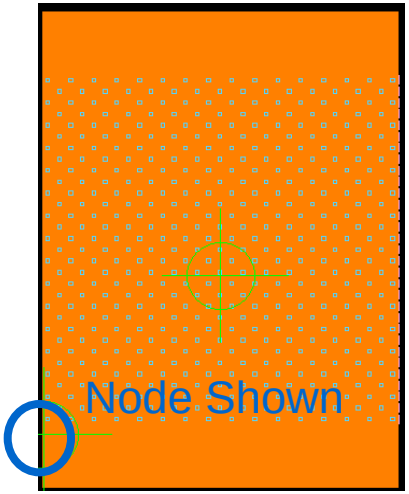
Current_block_G1_y_VDD_R294_4_RC

Current_block_G1_y_VDD_R294_4_RCLK
(correct waveform)

Transient Simulation Plot for VSS nodes

Supplying 30.30 nF Bypass Capacitance





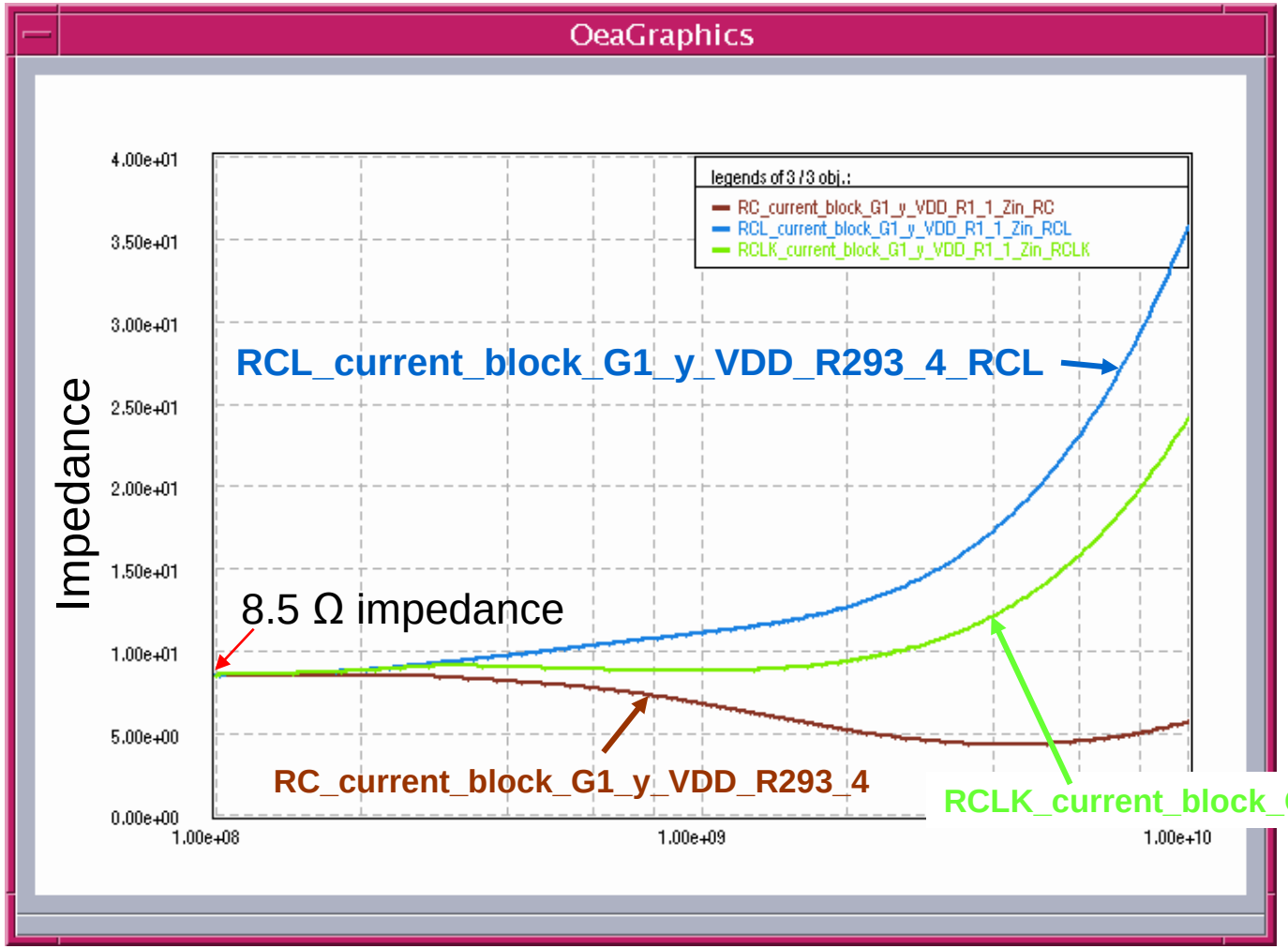
Current_block_G1_y_VSS_R2_1_RCL

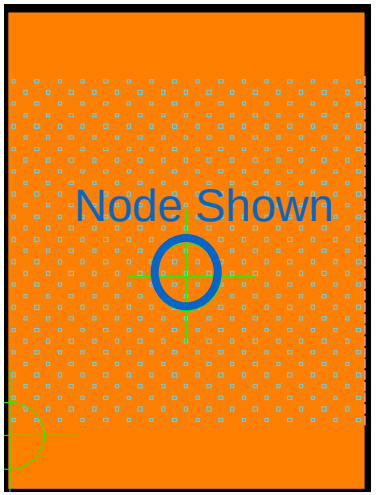
Current_block_G1_y_VSS_R2_1_RC

Current_block_G1_y_VSS_R2_1_RCLK
(correct waveform)

AC Simulation Plot for VDD nodes

Supplying 30.30 nF Bypass Capacitance

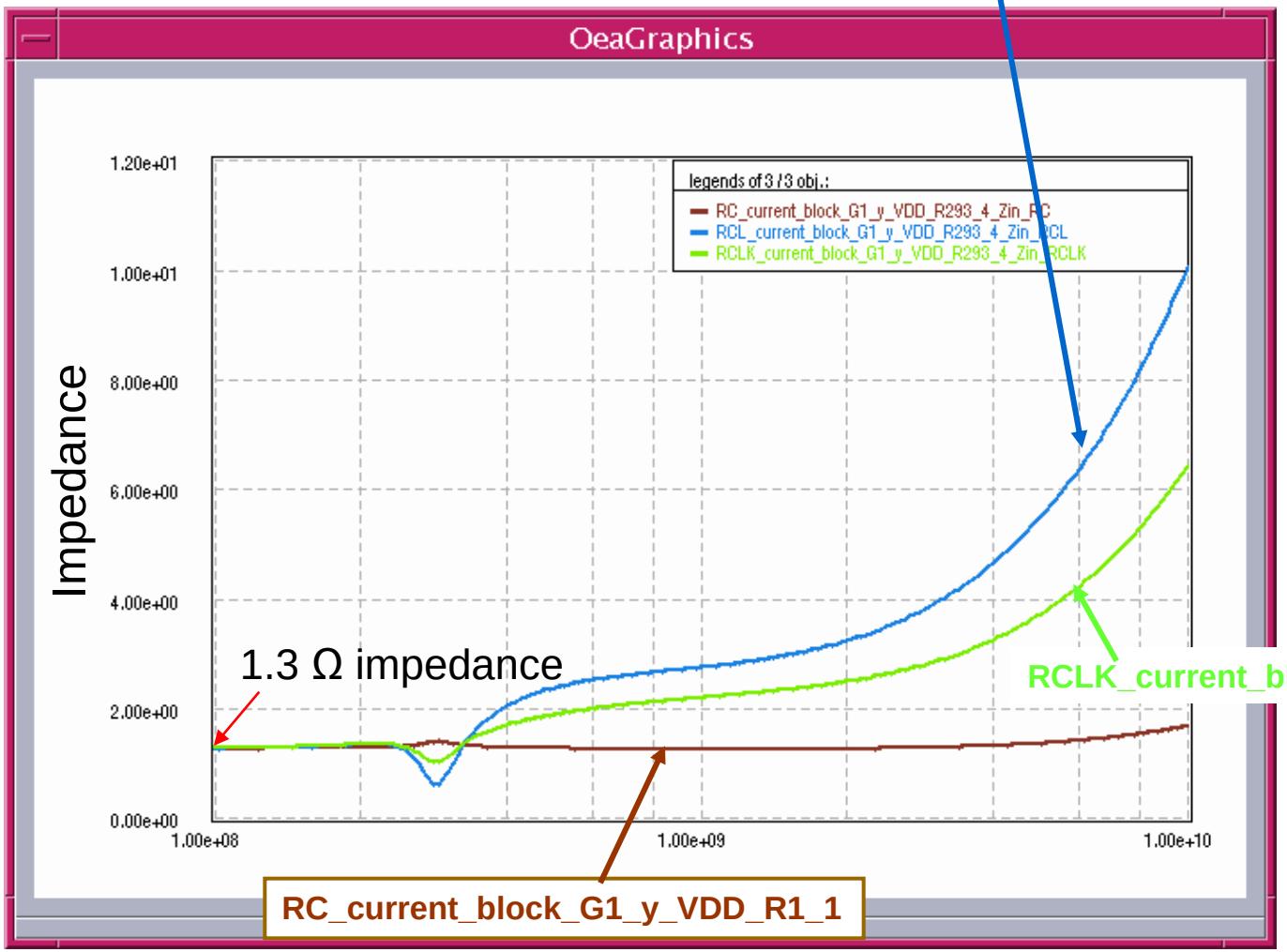


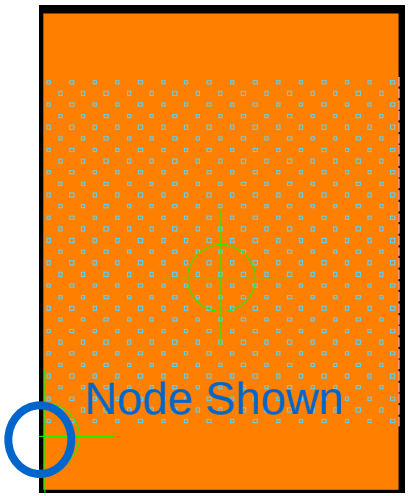


AC Simulation Plot for VDD nodes

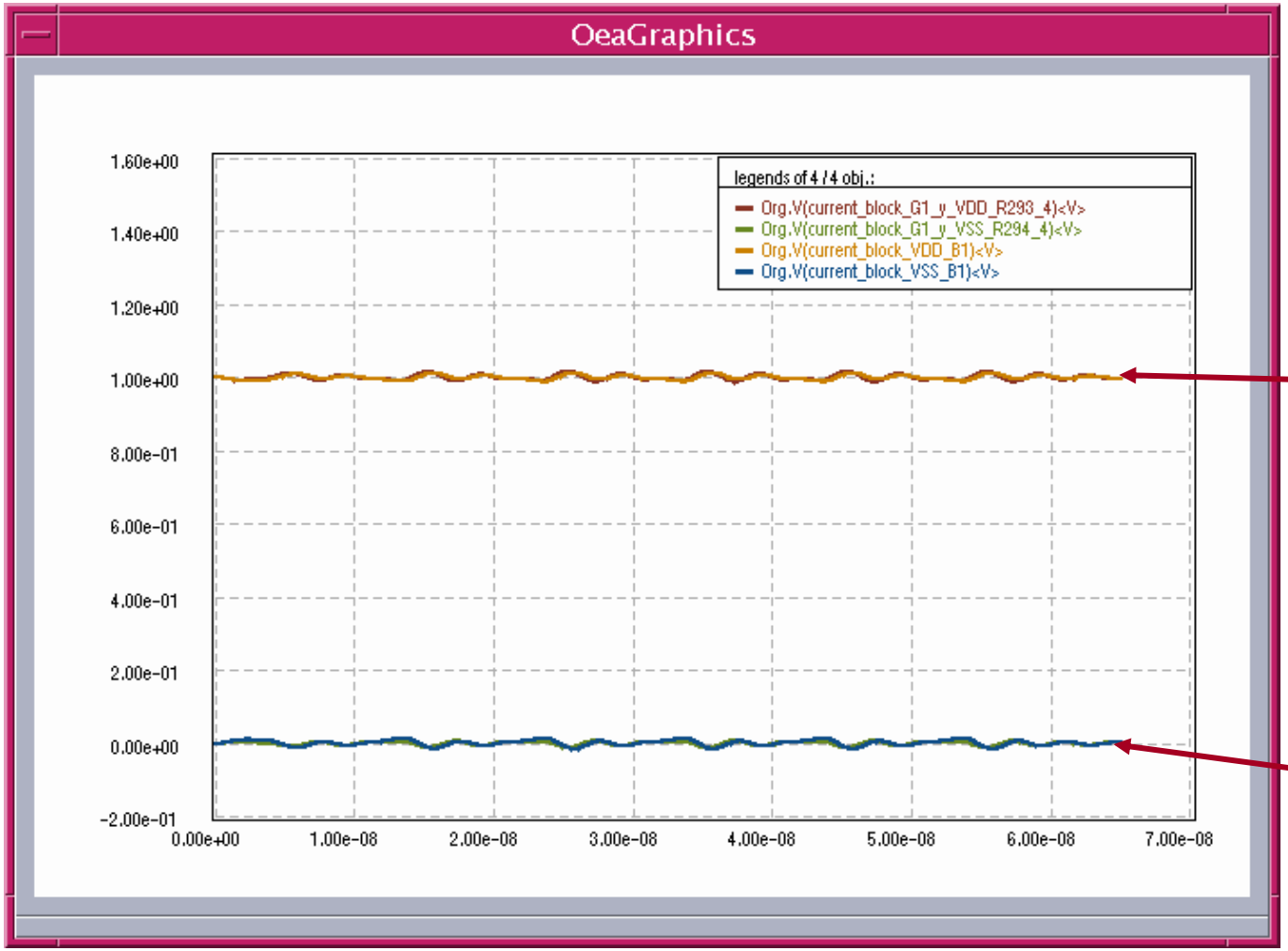
Supplying 30.30 nF Bypass Capacitance

RCL_current_block_G1_y_VDD_R1_1





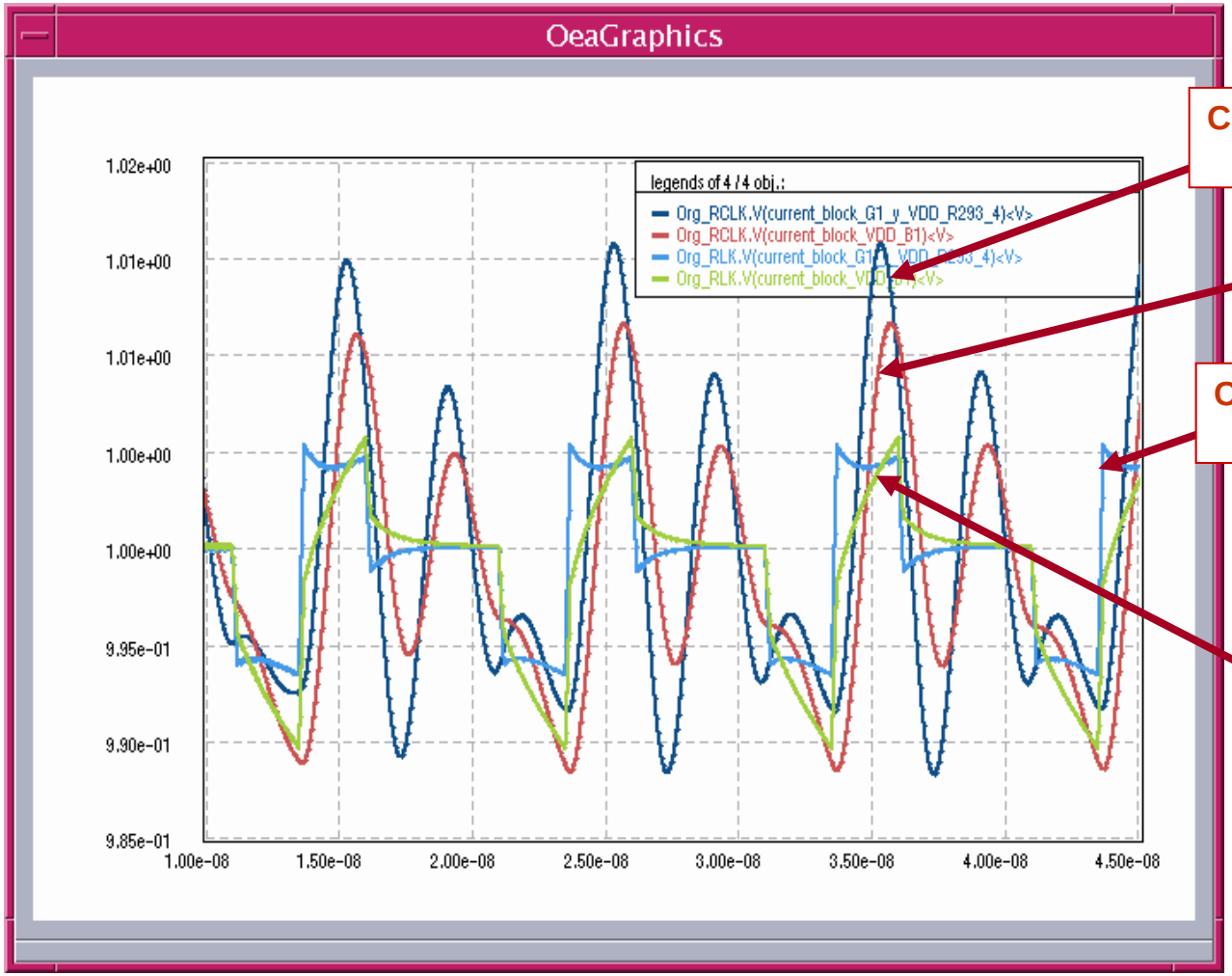
Transient Simulation Plot



VDD Nodes

VSS nodes

Transient Simulation Plot



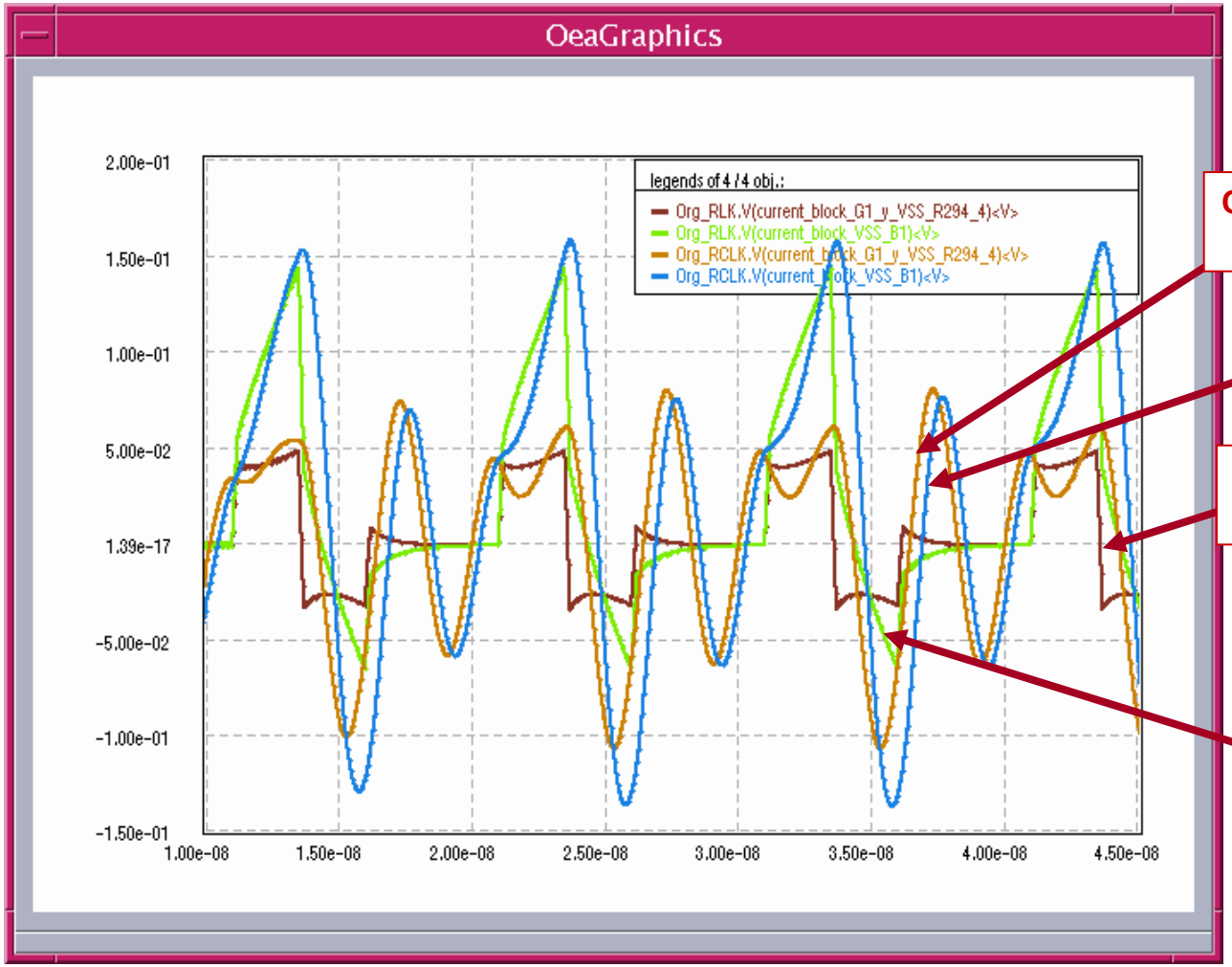
Current_block_G1_y_VDD_R293_4 (RCLK simulation)

Current_block_VDD_B1 (RCLK simulation)

Current_block_G1_y_VDD_R293_4 (RLK simulation)

Current_block_VDD_B1 (RLK simulation)

Transient Simulation Plot



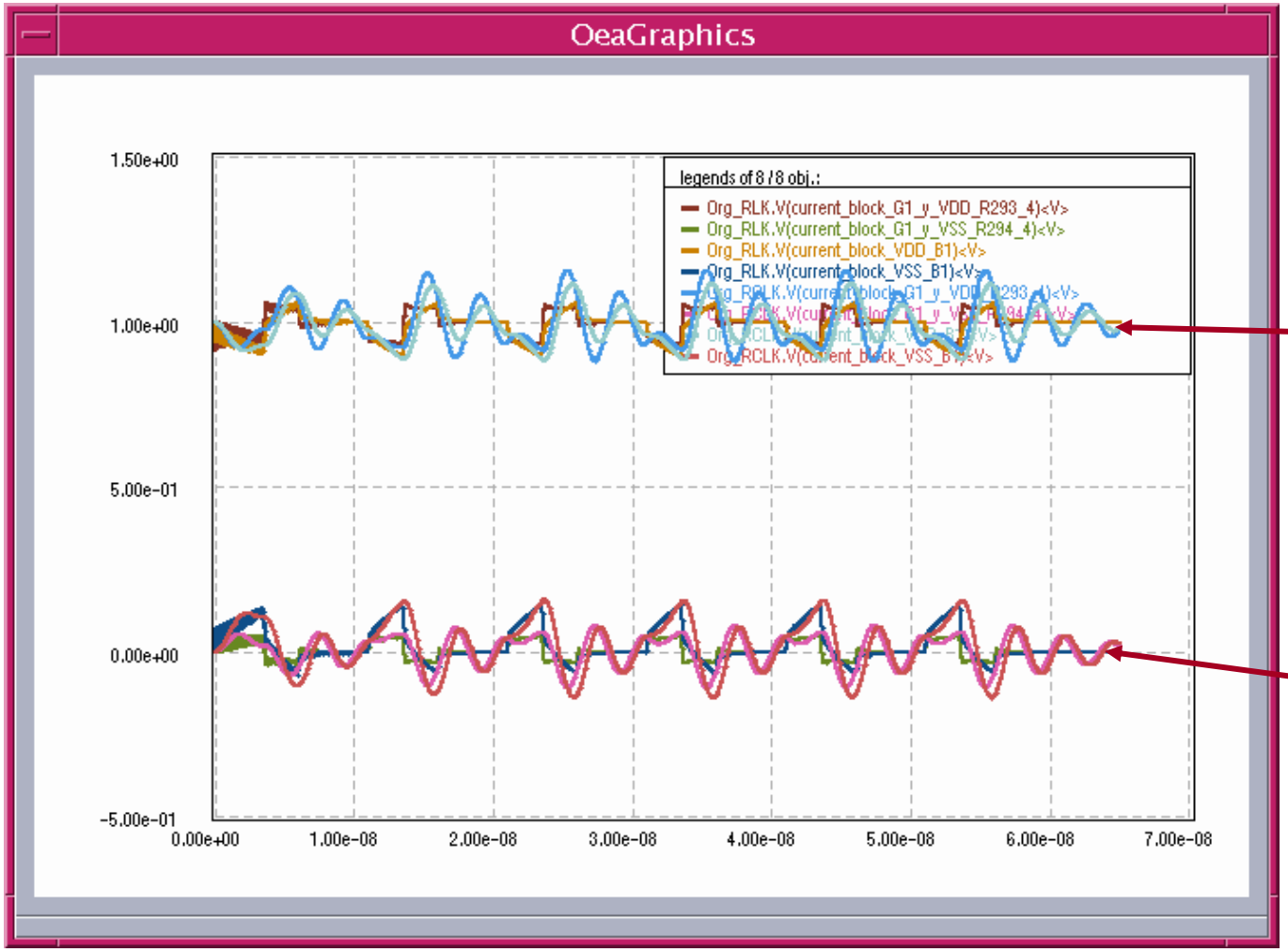
Current_block_G1_y_VSS_R293_4 (RCLK simulation)

Current_block_VSS_B1 (RCLK simulation)

Current_block_G1_y_VSS_R293_4 (RLK simulation)

Current_block_VSS_B1 (RLK simulation)

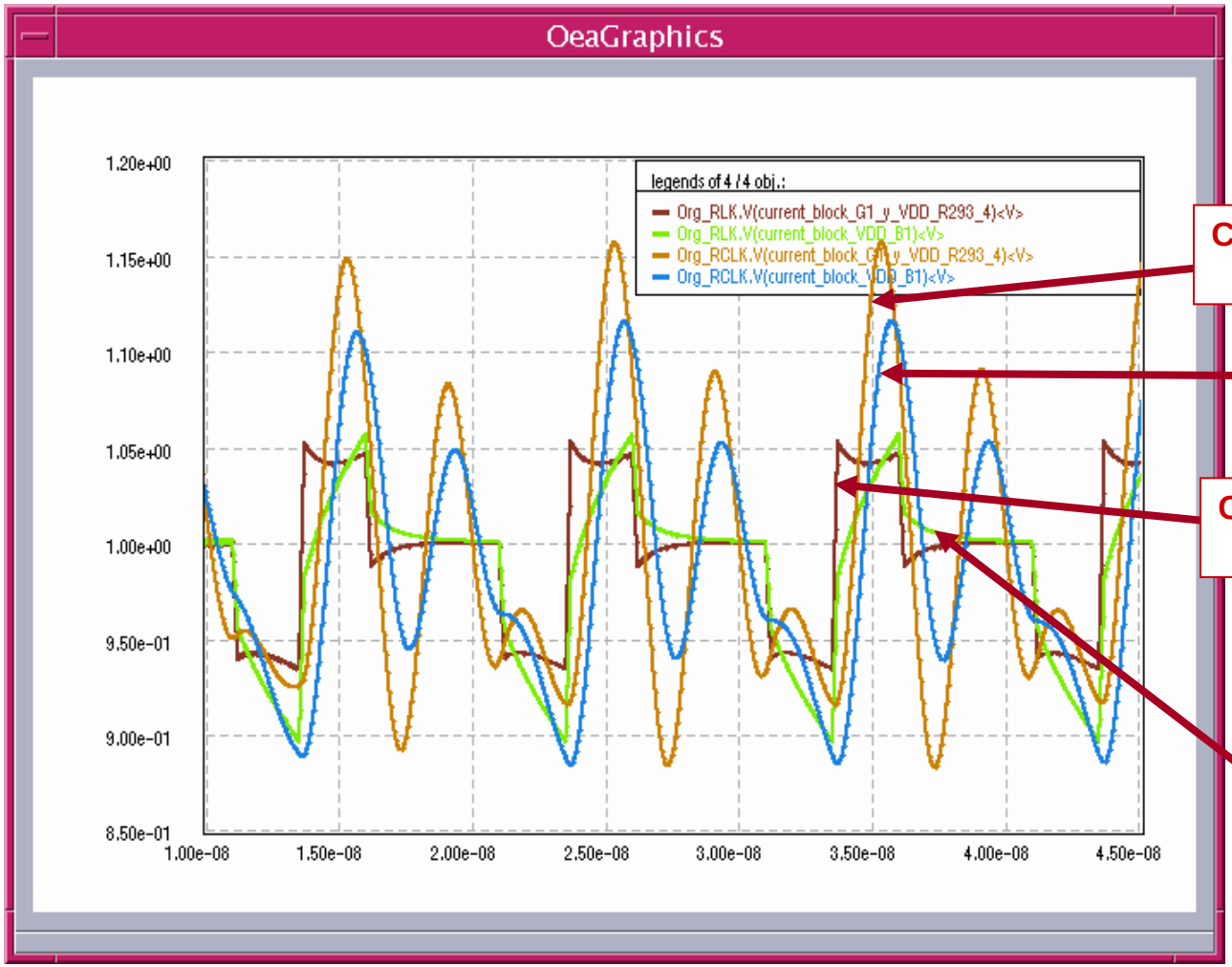
Transient Simulation Plot



VDD Nodes

VSS nodes

Transient Simulation Plot



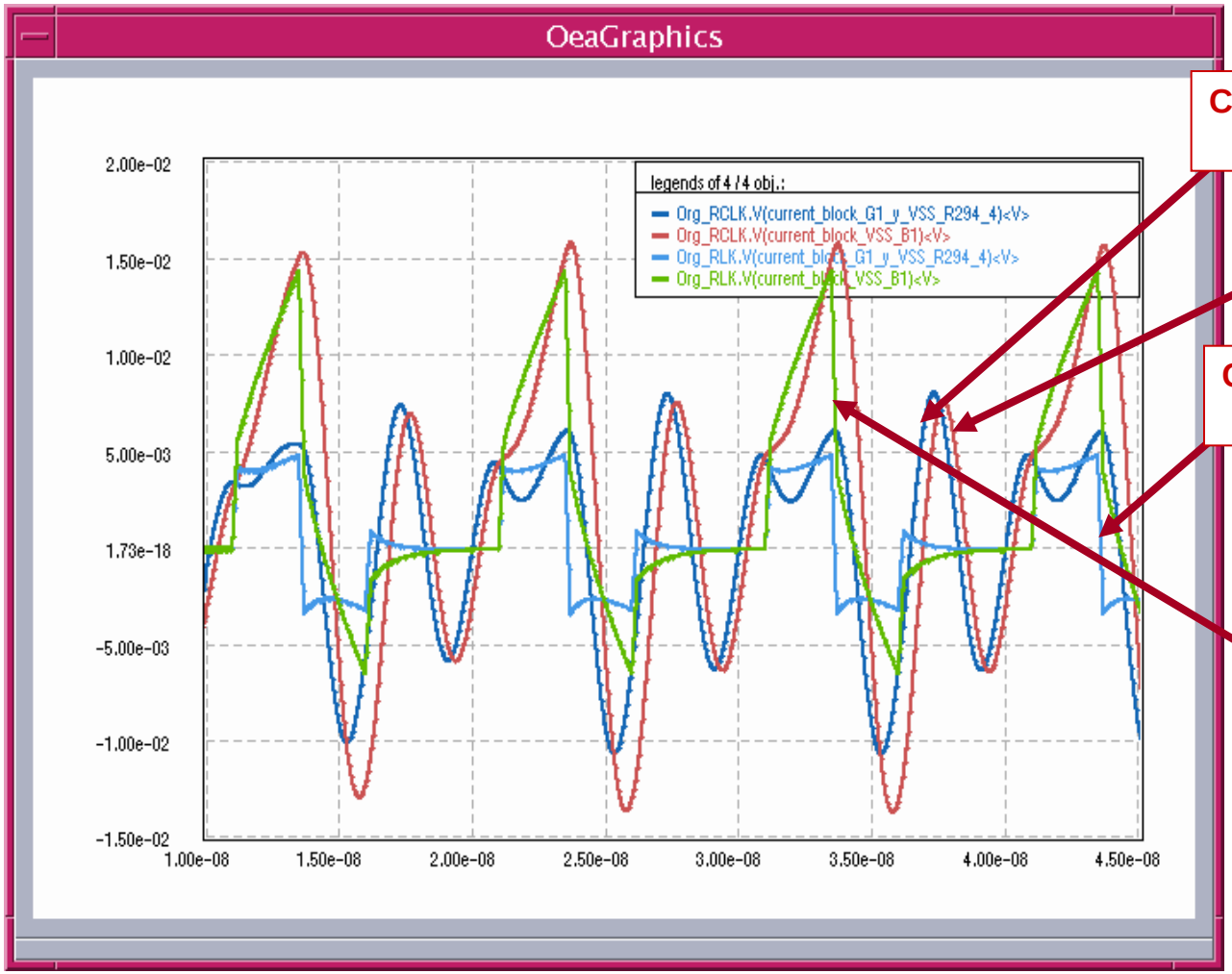
Current_block_G1_y_VDD_R293_4 (RCLK simulation)

Current_block_VDD_B1 (RCLK simulation)

Current_block_G1_y_VDD_R293_4 (RLK simulation)

Current_block_VDD_B1 (RLK simulation)

Transient Simulation Plot



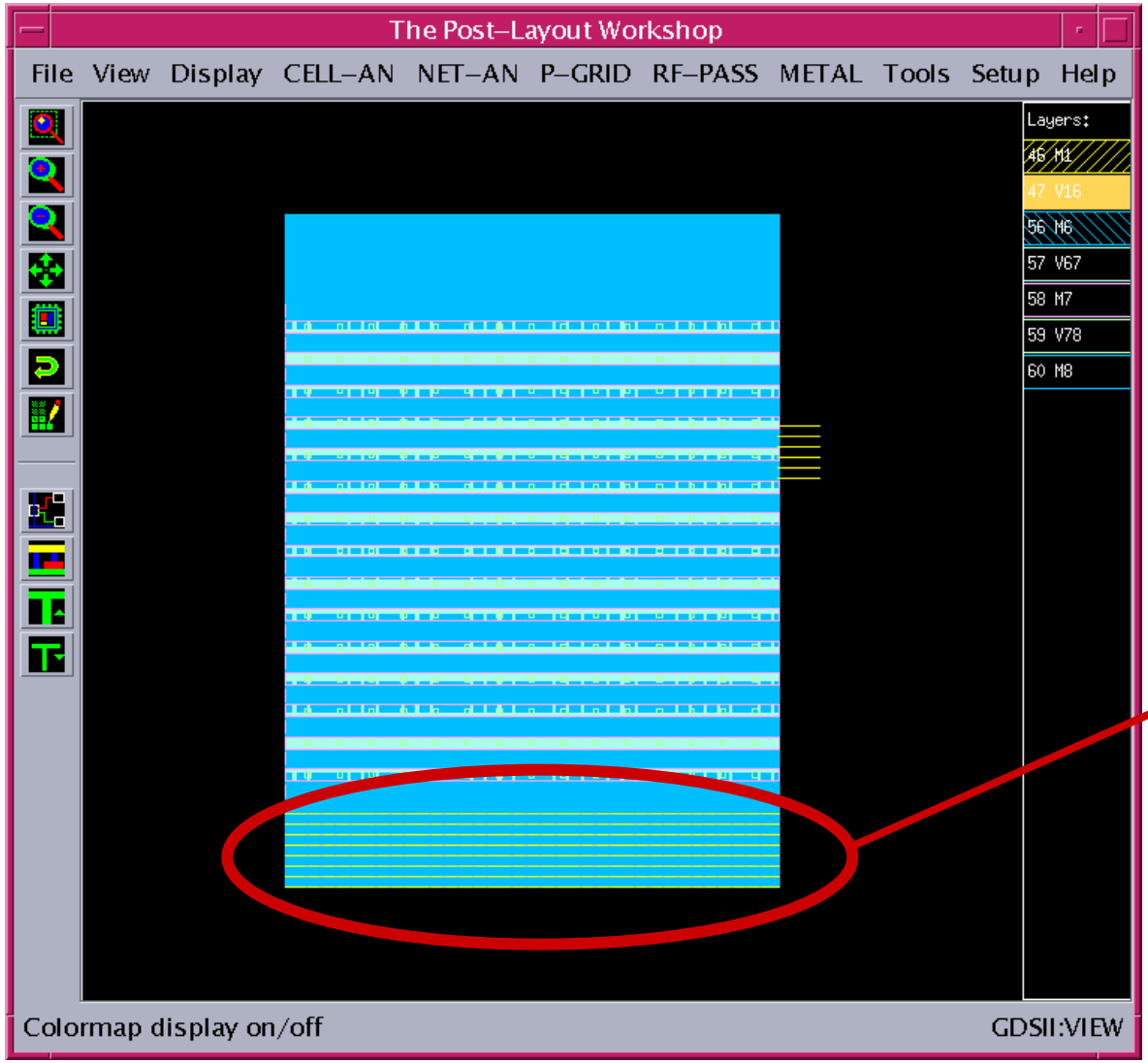
Current_block_G1_y_VSS_R293_4 (RCLK simulation)

Current_block_VSS_B1 (RCLK simulation)

Current_block_G1_y_VSS_R293_4 (RLK simulation)

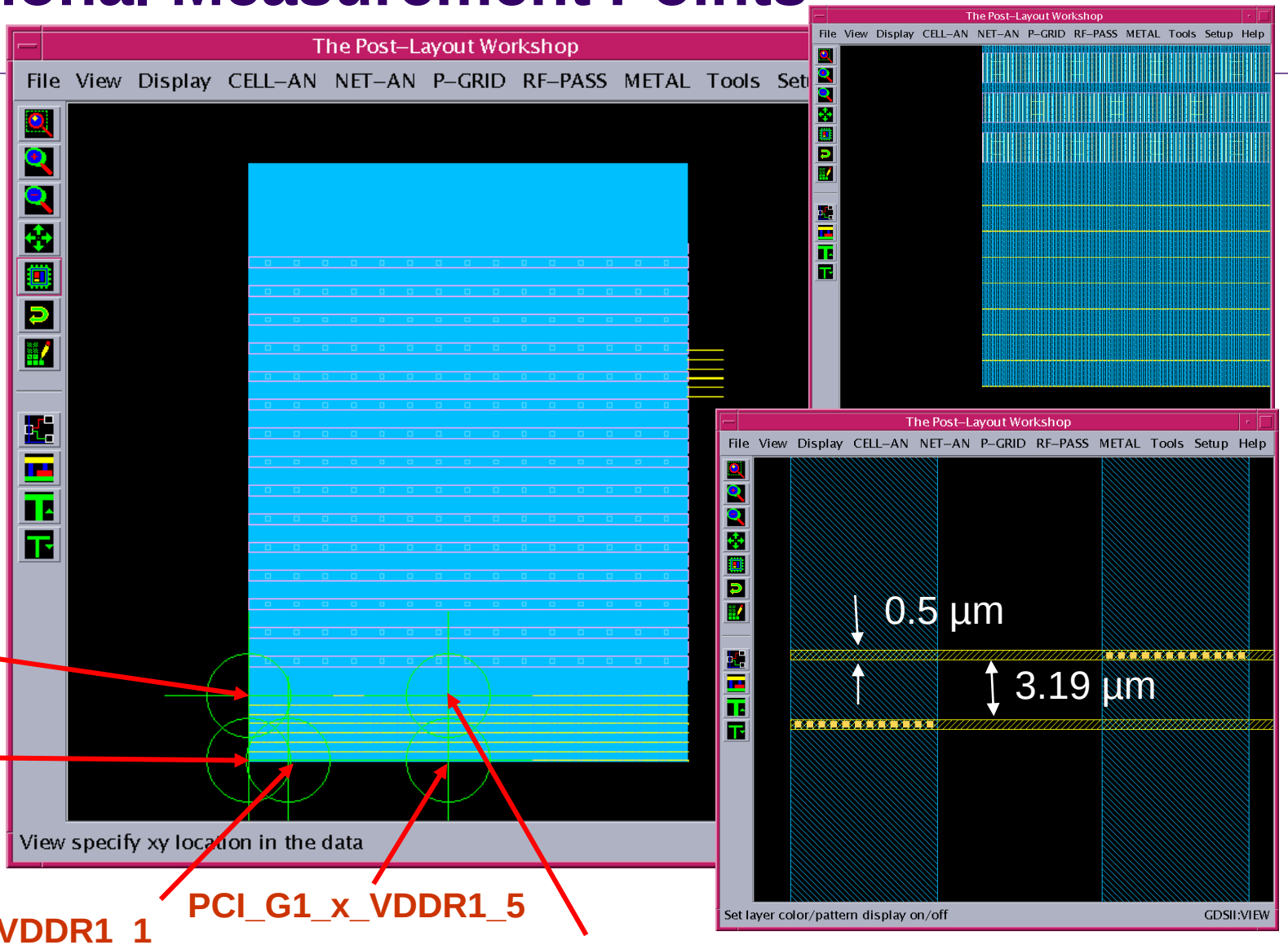
Current_block_VSS_B1 (RLK simulation)

Additional Analysis Including Layer M1

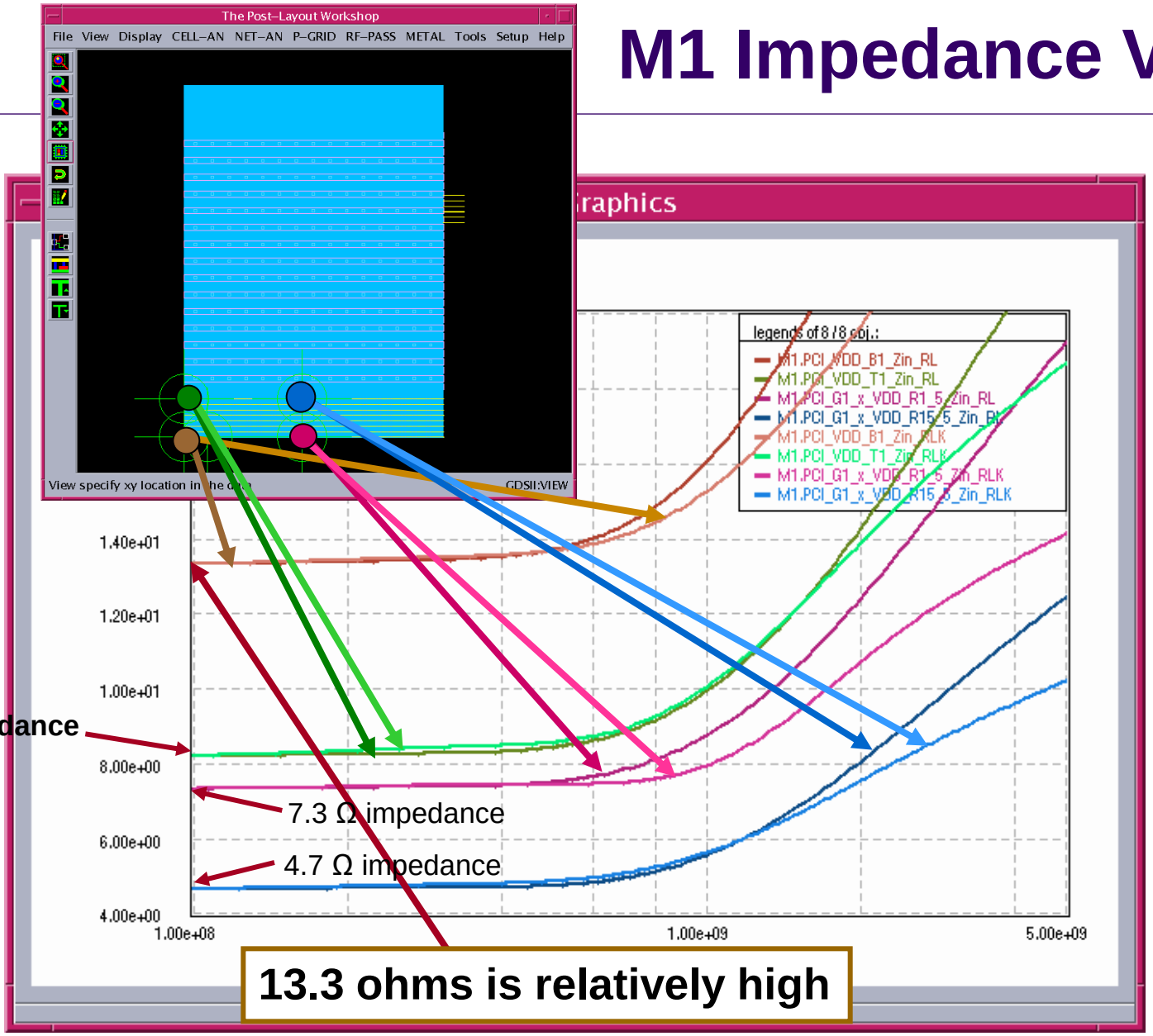


Unsure of Actual M1 in This Area

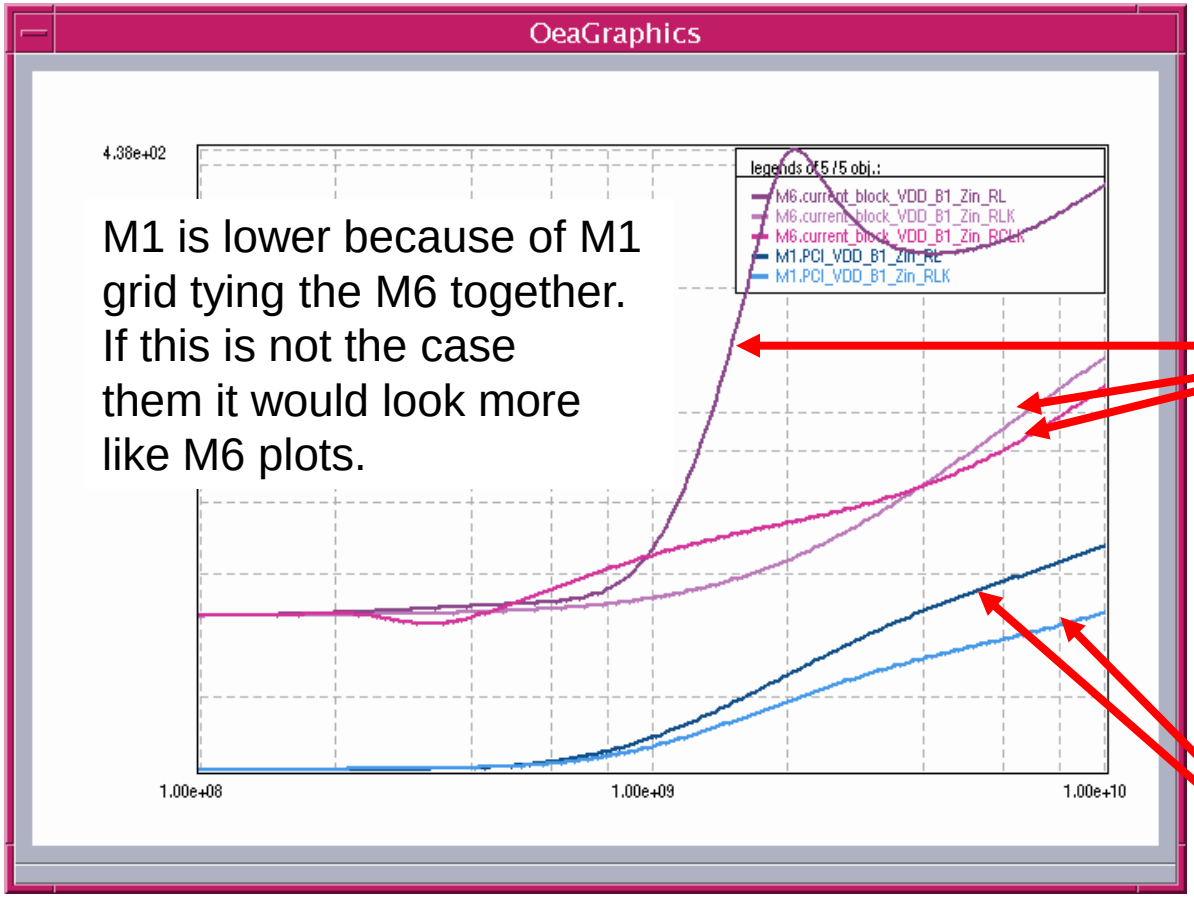
Additional Measurement Points



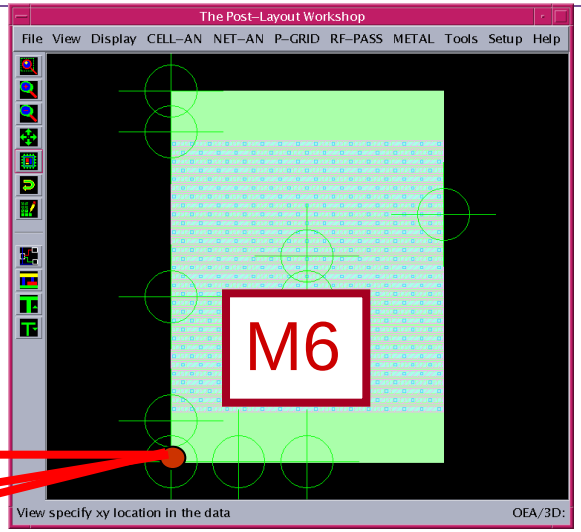
M1 Impedance Values

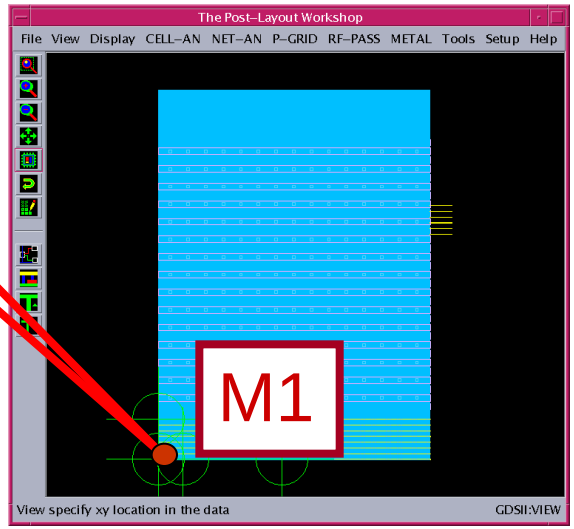


Comparison of Values at Same Locations
but Different GDS Layers - M6 and M1



M1 is lower because of M1 grid tying the M6 together. If this is not the case them it would look more like M6 plots.





Conclusions

- Dummy Metal and Slotting Required in DSM is Very Important in Analog and RFIC's
- In Digital IC's With High Metal Density, Dummy Metal and Slotting is Not That Significant
- In High Performance IC's, Simulation of VDD/VSS Requires the Modeling of Inductance and Mutual Inductance to Determine Proper Rail Placements and Sizing of On-Chip Decoupling Capacitors