A Practical Approach to Preventing Simultaneous Switching Noise and Ground Bounce Problems in IO Rings

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Proper planning and early Spice level simulation is required to detect possible simultaneous switching noise and ground bounce failures. A fast iterative what-if method to find solutions for these problems is presented below and is based on actual design experience resulting in the development of a software tool called RING Designer for automating the methodology. A real example is shown where a problem was detected and fixed early in the design planning stage.

A complete Spice simulation of the IO ring for simultaneous switching noise and ground bounce problems requires the inclusion of the IO ring RCLM parasitics, a model of the IC package, and all IO buffers. This simulation should be done at the earliest point in the design process when pin placements, package selection, and chip size are still flexible. This is the point at which early IO ring simulation can yield a potential savings in chip size by minimization of the power and ground IO pins or with selection of the most cost-effective package with acceptable pin inductances. Cost trade-offs are made easily because the PCB, package and chip rings are modeled together. It is also the point at which it is easiest to perform pin swapping, IO buffer sizing, and the insertion of power and ground pins to reduce noise and ground bounce. Thus the proposed methodology is optimally inserted in a planning flow, rather than in a post-layout verification flow.

By understanding the causes of IO ring simultaneous switching noise and ground bounce failures, it is easier to make engineering decisions which will correct problems found by the simulations. The main switching condition where noise problems are evident is when too many output buffers switch together to cause large inductive voltage spikes in the IO power rail. If there are an insufficient number of power and ground pins or if power and ground pins are poorly spaced, unstable voltages can occur at some of the IO buffers. Also, if the bond wire or package lead inductance is too high, and a delay on-chip decoupling is insufficient a delay in getting the required switching current to the IO buffers can occur causing a collapse of the power rails and group launch delays or switching failures. Another problem introduced by package parasitics can be inductive crosstalk induced delay or speedup between IO signals with closely spaced package traces or bond wires.

To avoid creating a simulation file that will take too long to simulate or which fails due to memory limitations, care must be taken to simplify the ring and package input files. The Spice files need to be reduced down to only significant RCLM parasitics. For instance, traditional extraction and modeling of the IO rings with all the relief cutouts and via arrays will create an extremely complex Spice file that will take days to run, if at all. Also, most traditional extraction tools do not include the most critical element, inductance. It is also difficult to separate out the parasitics provided for in the IO Spice sub-circuit models and extracted parasitics. By reducing the Spice to just an effective inductance and a resistance between pins and then attaching the full IO buffer Spice models to points on the ring. Spice will run in minutes allowing much iteration to optimize and fix problems (Figure1). To build the RLM model of the rings, a simplified ring geometry must be generated, connection nodes on the ring geometry identified for each IO pin and the Spice model extracted using a tool such as OEA's NET-AN which extracts the inductance and mutual inductance with the resistance model. An example of such an IO ring is shown in Figure 1.
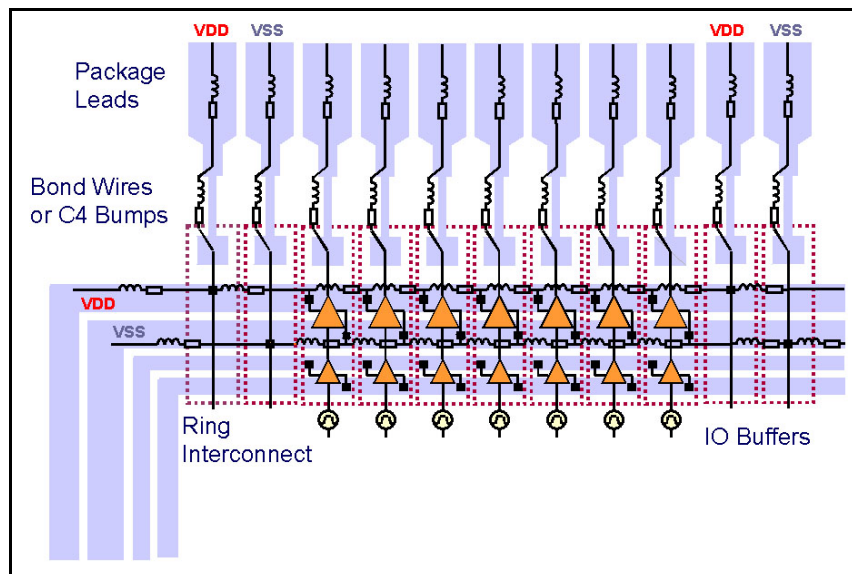
Figure 1. The Basic IO Ring Circuit

Since all Spice simulators are significantly slowed by mutual inductances, using reduction methods to deal with insignificant inductance couplings will reduce Spice run times. A tool such as OEA's CircuitSmart can be used to filter these values and optimize the package and ring Spice sub-circuits for simulation speed. The next step is to create a master Spice circuit deck containing the ring sub-circuit, the package sub-circuit, and the IO cell sub-circuits. This master sub-circuit must also include drivers and loads attached to the package and chip ends of the IO pins and hundreds of measure statements to obtain current and voltage levels at each IO pin connection, at the external package pins, and at the power and ground pin input and ring nodes (Figure 2). The resultant Spice run should be able to detect and help in understanding the causes of simultaneous switching noise and ground bounce problems. Nominal operating conditions for temperature and normal spice model speeds should be used for the initial simulation. Variations in Spice for the best case and worst case (i.e. fast models at lowest operating temperature and slowest models at the highest operating temperatures) should be done after the initial IO pin placement is verified.
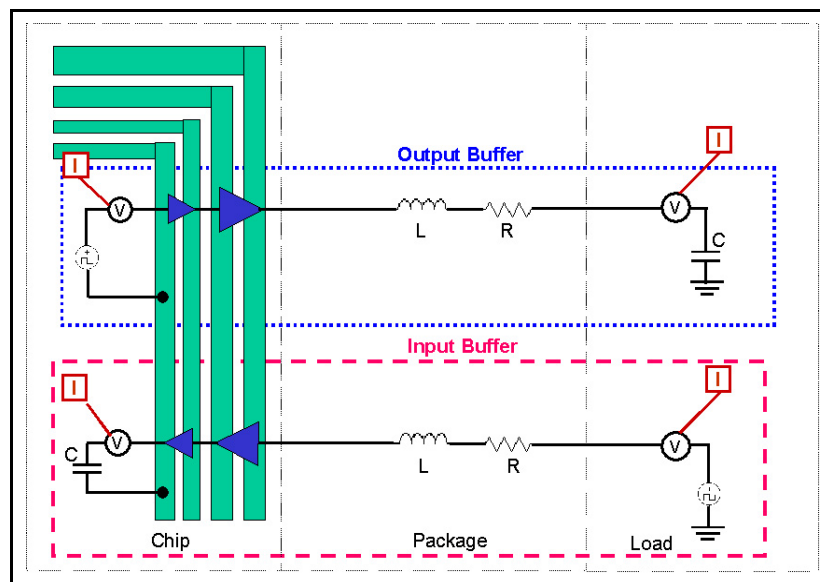

Figure 2. Voltage and Current Measurement Points for IO Buffers

An example of how this methodology was used to prevent a failure is presented in the 512-pin communications chip example in Figure 3. The OEA RING Designer, OEA NET-AN, and Silvaco SmartSpice tools were used for the task. In this case a detailed package model was unavailable from the package vendor, but worst case assumptions were made for the package parasitics based on previous similar packages. All of the power input pins were assigned 2nH of package inductance and a package resistance of 0.01 ohms. All of the IO buffers were assigned a package inductance of 5nH and a package resistance of 0.01 ohms. The output buffers were assigned a PCB load of 10pf and the input buffers were assigned an on-chip load of 0.5pF. The active IO pins were driven with a pulse of 1 ps rise and fall time. The main IO buffer rings were 60 microns wide and had a voltage of 3.3V and 0.0V. The pre-driver rails that were connected to core power were 20 microns wide and were supplied with 1.8V and 0.0V.
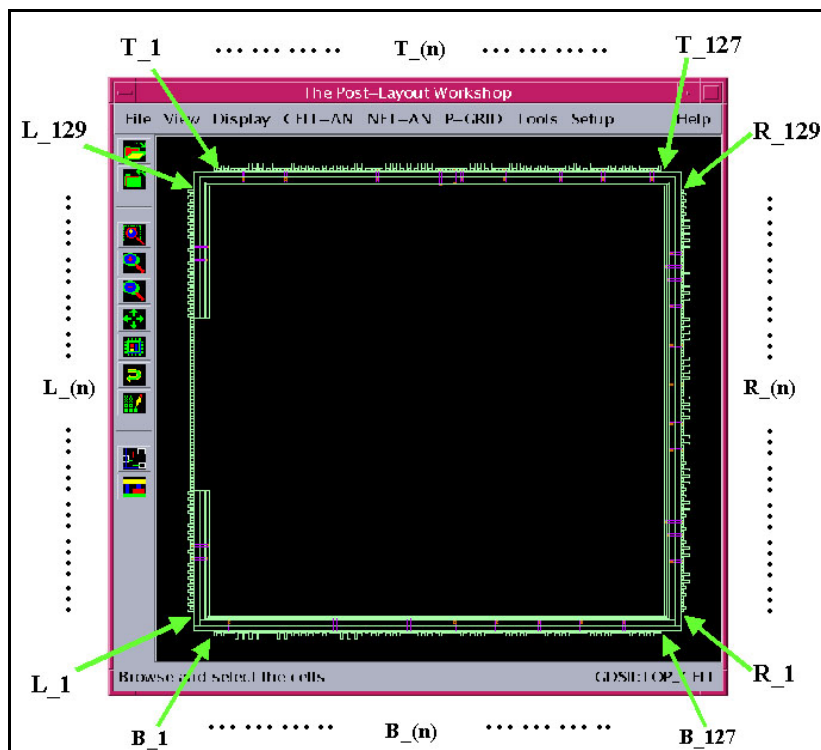

Figure 3. Example Ring Structure

The ring was split on the left side and had an isolated rail section dedicated to an IP block. This was ignored in the example below since it was isolated from the main rail structure. Since the buffers forming each IO bus were clustered together a decision was made to run each of the four IO buses in separate simulations (Figure 4).   This would further reduce simulation times, since each of the simulations involved only one-fourth of the active devices. A final more time-consuming simulation combining the low buses could be run once each bus was shown to operate properly on an independent basis.
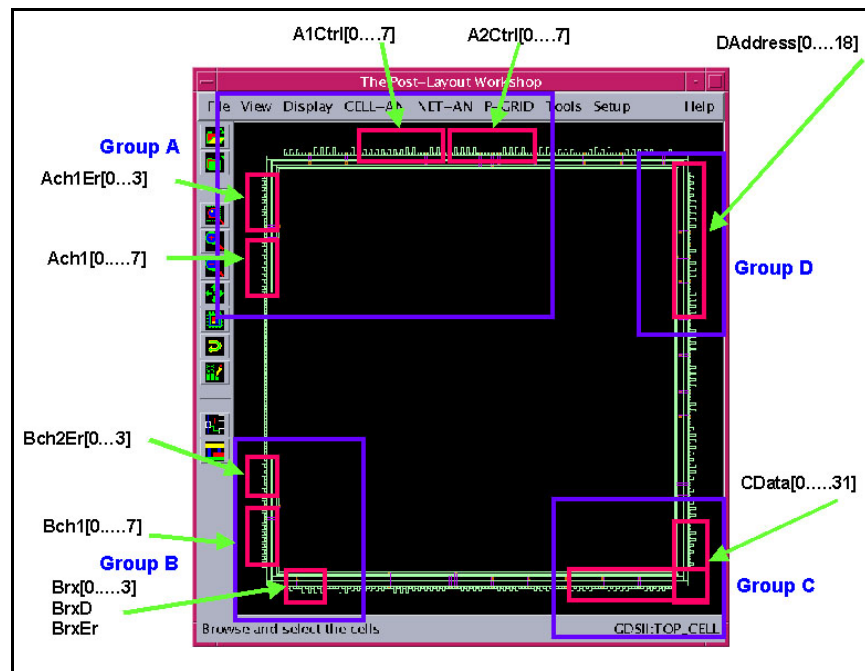
Figure 4. Grouping Simultaneous Switching Buffers

As shown in Figure 4 the first cluster in the upper left quadrant, Group A, had three (3) eight-bit IO buses and a single four-bit bus, which were all switched simultaneously. The number of power and ground pins supplying the rails in the area was VDD_IO 5, VSS_IO 4, VDD_CORE 2, and VSS_CORE 2. All of the VDD_IO and VSS_IO pins in the area were on the topside of the ring. The remaining pins in the vicinity were control logic IOs that were treated as inactive or 'quiet' victim IOs and core power IOs. The other groups (B, C, and D) were simulated later. The result of the Group A simulation revealed a complete collapse of two of the buses which were on the left ring as can be seen in the Spice waveforms shown in Figure 5.
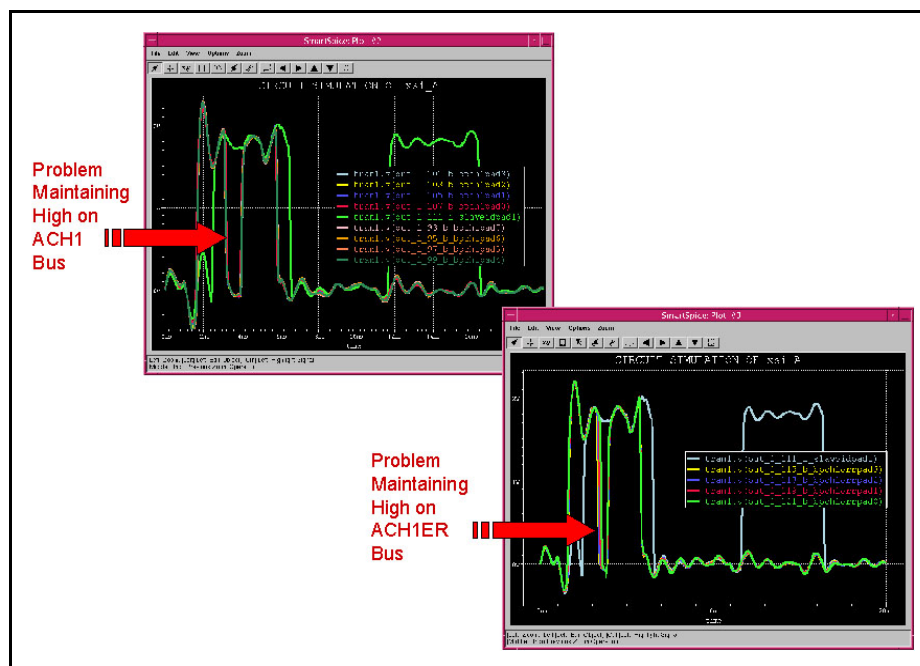

Figure 5. Group A Spice Simulation Transient Output

In examining the reasons for the failure, all of the measure statements implemented in the master Spice deck become crucial. Looking at the IO VDD_IO and VSS_IO pins on the bus IOs indicate a high current draw on the rail for each pin (Figure 6). If switched individually, or a few at a time, the rail probably would have supplied sufficient current to hold the signals high during the on time of the pulse. Because of the large inductive path in getting power to buses, the rail experienced a collapse. The next step was to review how many VDD_IO and VSS_IO pins were in the vicinity of the buses. It was easy to see that only a few pins were assigned near this bus on the hanging split end of the rail on the left side. Where in other areas there were VDD_IO and VSS_IO pins for every 15 pins, in this cluster of 104 pins there were only 5 VDD_IO pins and 4 VSS_IO pins or one for every 20 IO pins and these were poorly placed all on the top and no pins on the left side.
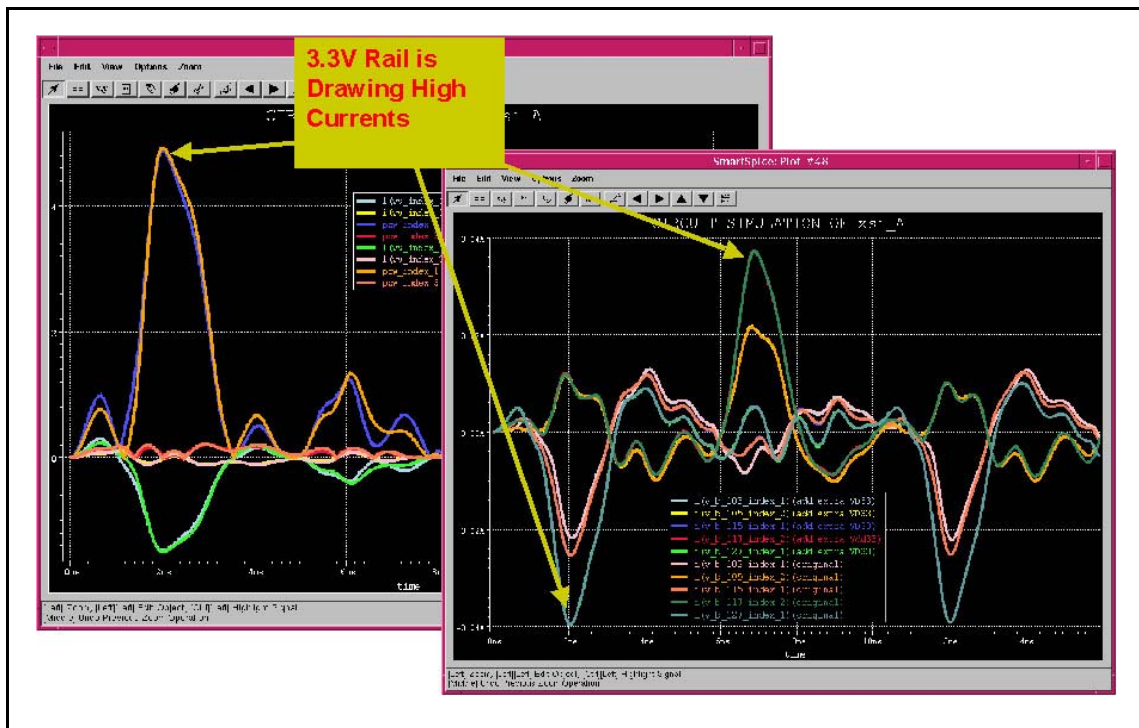

Figure 6. Group A Spice Simulation Current Plots

When fixing these problems and similar simultaneous switching and ground bounce problems, there are always alternatives. For instance, this problem can be solved by lowering the inductance on package power pins in the area, adding or moving power pins closer to the bus, moving one or more buses to a different area on the chip with better power connections, spreading out simultaneously switching pins over a wider area of the chip, or adding decoupling caps which will store current on the chip close to the bus or in the package creating a lower effective inductive path to the area. Choosing the correct solution almost always involves an engineering decision that may require a trade-off between performance and cost. For instance, adding pins or reducing the inductance of the package pins may require a more expensive package. In this case, several control logic pins near the buses of Group A were moved to another area of the chip IO ring and VDD_IO and VSS_IO pins added in their place (Figure 7). The repaired IO ring configuration was re-simulated and the resultant waveforms shown in Figure 8 confirmed that the problem was solved.
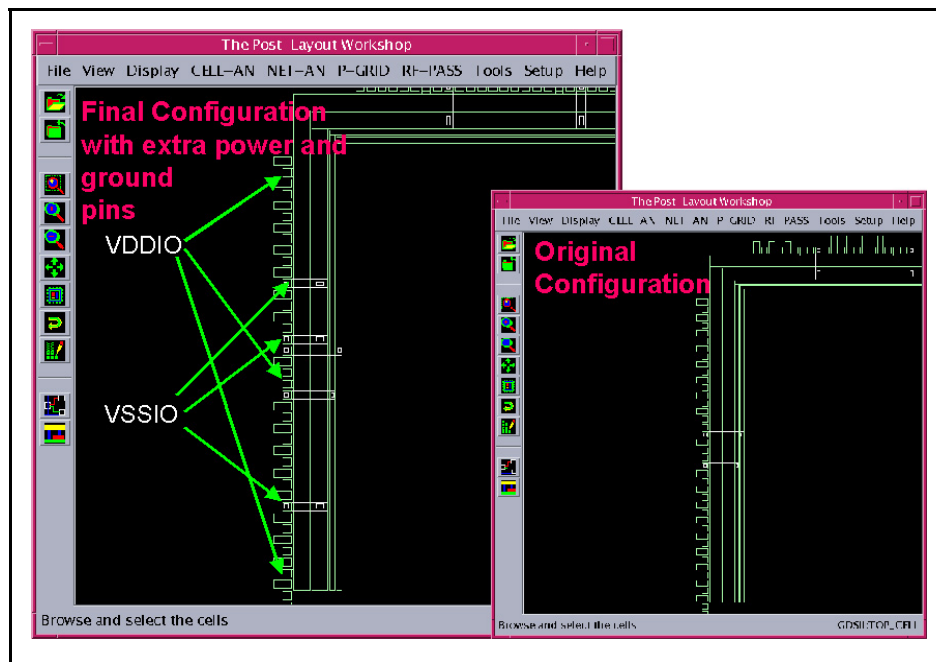
Figure 7. Group A Power Pins Before and After the Fix

Simulation of the other Groups (B, C, and D) of buses in this case confirmed no other problems existed. Since the methodology above is fast many what-if scenarios can be quickly examined once the final con-figuration is determined to further verify the IO placement in extreme conditions. Some examples are:

a.) Examining different possible loading conditions and integrity of signals under different switching conditions
b.) Evaluating process corners and temperatures
c.) Examining signal integrity of active and quiet IO buffer output pins
d.) Looking for IO buffer output pin noise errors
e.) Examining package inductance effects on the buffer IO supply pins
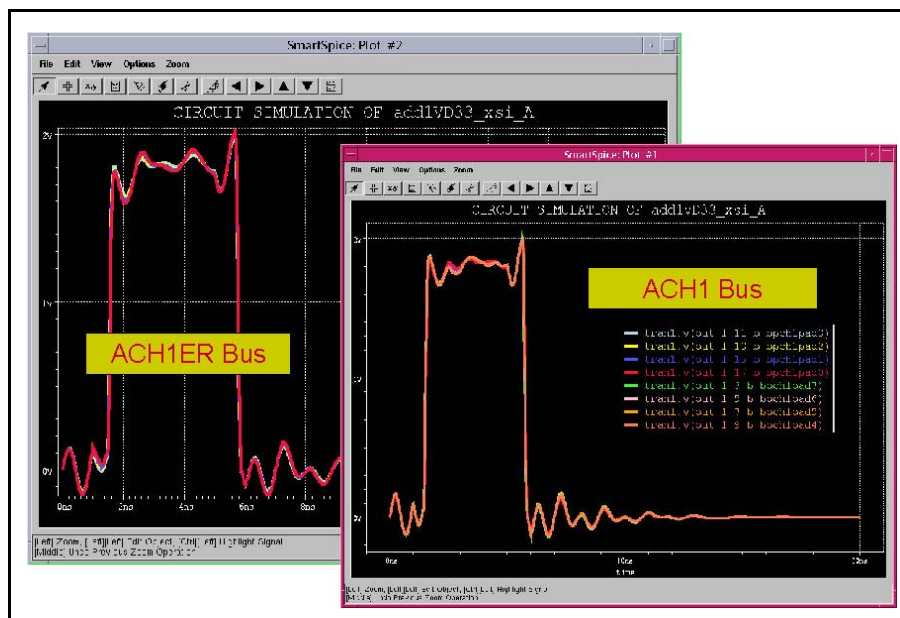f.) Examining package inductance effects on quiet lines

Figure 8. Group A Spice Re-simulation After Power Pins

Conclusion
The pre-planning methodology of building a simple model of the IO ring with all significant IO ring and package parasitics, using actual Spice IO sub-circuits, and simulating in Spice is a fast and practical method of avoiding simultaneous switching noise and ground bounce issues caused by poorly designed IO ring placements. Since the methodology requires no integration, it can be implemented in any design flow and is easily automated as proven by the OEA RING Designer tool. The same pre-planning methodology can be applied in other critical nets in the chip design, such as core power and clocks, to avoid problems and give a more correct-by-construction design.

References
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