Optimization of Metal-Metal Comb-Capacitors for RF Applications

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Abstract

This paper describes the design and modeling of metal-metal comb-capacitors (MMCC) for RF and analog applications. An optimum MMCC topology is found for a 0.25µ process that results in capacitance per unit area of 0.61 fF/µ^2, parasitic capacitance to ground of 8%, as well as a very high Q (>200). Due to the large number of possible structural variations, rapid modeling of these structures is necessary for optimization. The commercially available RF-PASS™ [1] software is validated against silicon measurements on a 0.25µ 5-metal process. Future trends for MMCCs are explored and found to be very promising.

Introduction

Capacitors are used in a variety of ways within RF circuits. These include their use in resonant circuits and filters, voltage-controlled oscillators, coupling between stages and bypassing. The characteristics by which such capacitors are judged include capacitance density; parasitic capacitance to ground; quality factor; voltage, temperature and frequency coefficients; and the maximum allowable peak repetitive voltage.

Building and optimizing a metal-metal comb-capacitor involves a number of complex tradeoffs. There are a large number of possible topologies and each topology has several tunable parameters. Furthermore, the optimum tradeoffs derived for a 0.25µ process may not be optimum for a 0.18µ or smaller process. It becomes impractical to fabricate and measure all the possible variations. Thus, extraction software was utilized to simulate numerous variations of which only a small subset were fabricated and measured to validate the software and methodology.

The simulation software used is RF-PASS™; it is specifically designed to model large distributed passive structures for RF applications using full 3-D field solvers. It extracts a fully distributed and coupled resistance, capacitance and inductance (self and mutual) model of all conductors. In addition, the software includes effects important to RF applications such as skin effect and induced currents in the substrate. A detailed frequency dependent spice model is created and this model is used to generate S and Z parameters. Inductance modeling of capacitors can also be included to predict the self-resonance frequency.

Capacitor Types

In commercial CMOS or BiCMOS processes the following capacitors are generally available:

- Capacitors that use the MOSFET gate oxide [2]
- Metal–insulator-metal (MIM) capacitors [3,4]
- Poly–insulator-gate poly (Double Poly) capacitors [2]
- MMCC [5,6,7,8,9]

Currently, the highest capacitance densities are obtained with capacitors that utilize MOSFET gate oxides. Capacitance density of 6 fF/µ^2 has been reported [2]. However, there is a trade-off between the gate oxide thickness and the breakdown voltage. A 50-Angstrom gate oxide capacitor in a 0.25µ processes can typically withstand a maximum peak repetitive voltage of 2.75V. Depending on the topology and circuit design this may be a limitation. The CV characteristic varies with the particular process technology and is non-linear. This non-linearity may cause distortion in the circuit.

To minimize parasitic capacitance to ground MIM capacitors are typically built near the top of the metal stack; for example, a bottom-plate using METAL4 and a top-plate using METAL5 separated by a thin insulator layer a few hundred Angstroms thick. The large separation between the bottom plate and substrate (≅ 6µ) helps in reducing the parasitic capacitance to ground to about 2% of the useful inter-metal capacitance (trans-capacitance). MIM capacitors have very good voltage and temperature-coefficient characteristics and a capacitance density of approximately 0.8fF/µ^2. MIM capacitors are available in many RF CMOS and BiCMOS processes, however, they require extra masking steps to implement and increase the cost of the IC. Furthermore, these devices do not scale with process technology.

Double-poly and MOS capacitors also have parasitic capacitance associated with them. Double-poly capacitors have about 18% parasitic capacitance to ground while MOS capacitors can have 2~20% parasitic capacitance to ground depending upon their design. Both MOS and double-poly capacitors have the problem of very high series resistance to one of the two nodes.

Metal-Metal Comb-Capacitors

Metal-metal comb-capacitors hold much promise in providing capacitors that continue to improve with

succeeding process technologies. Capacitance density increases significantly as the number of metal layers increase and the feature size decreases. Such capacitors can be optimized to minimize parasitic capacitance and to make the parasitic capacitance symmetric, thus reducing noise pickup from the substrate or nearby structures.

Various MMCC topologies of capacitors have been reported in literature [5,6,7,8,9]. In this work, the topology shown in Fig. 1 is used [6]. In general the topologies can affect the capacitance density by trading off capacitance from three sources: 1) Parallel plate capacitance between conductors on two different metal layers (vertical fields). 2) Parallel plate capacitance between two conductors on the same metal layer (horizontal fields). 3) Fringe capacitance that cannot be attributed to either of the two preceding sources (fringing fields). While useful as a conceptual model, for feature sizes below 1.0μ, this simple model must be replaced with a full 3D field solver to get accurate results.

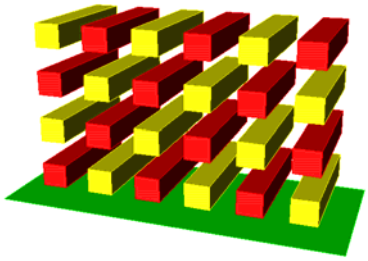

Figure 1: A cross section of the MMCC device described in this paper. Colors represent the two different nodes of the capacitor. The bottom plane represents the substrate ground.

Each topology also has many tunable parameters. Only after optimizing these parameters for each topology can one properly compare the various topologies. One must choose which metal layers to use, how long and wide the fingers should be and how to connect the fingers together. These choices will affect capacitance density, parasitic capacitance and quality factor. Choosing to omit metal layers near the substrate reduces parasitic capacitance to ground but also decreases the capacitance density. Narrow fingers and spacing have larger capacitance density but increased resistance that reduces the quality factor. The optimum length of a finger is dependent on the resistivity and width of the finger. To model the capacitor near self-resonance the inductance and mutual inductance of the fingers and leads must also be included. The location and number of vias used to connect metal layers that form part of the same node are also important parameters. One can greatly increase the series resistance by an improper placement of vias.

Prior work has shown MMCC devices with a capacitance density of 0.53 fF/μ^2 [5] in a 0.25μ process technology. The capacitance density depends on the topology of the finger structure used. In this paper MMCCs are shown to produce a capacitance density of $0.61fF/\mu^2$ on a 0.25μ technology. Much higher capacitance densities are predicted for finer lithography processes, please see Table 3.

The MMCCs in this paper have a parasitic capacitance of 4% from each node of the capacitor to ground. As both nodes are almost equally coupled to ground, substrate noise is not readily picked up by the capacitor. Capacitors based on finer lithography processes can achieve a parasitic capacitance of less than 0.5% per node.

The Q-factor is a measure of the useful energy stored in the capacitor versus all other energy loss mechanisms. The energy loss mechanisms include energy dissipated through resistive losses in the conductors and substrates and the energy siphoned into the parasitic capacitances. Care needs to be exercised in comparing Q factors as they are a function of the value of the capacitance and frequency. MIMs and MMCCs of 500fF have a $Q > 80$ at 2.4GHz.

Modeling of Metal-Metal Comb Capacitors

MMCCs of various physical dimensions were laid out. The inputs required to RF-PASS are the GDSII layout and a process technology file. The process technology file contains information on thickness and resistivity of substrate layers; thickness and resistivity of conductive layers; and thickness and permittivity of dielectrics. The inputs are read into RF-PASS after which the nets and nodes can be identified using the graphical user interface. The output of RF-PASS consists of a spice file containing thousands of distributed resistance, capacitance, inductance and mutual inductance elements. Many of these elements are frequency dependent. This spice deck is then solved for Z, Y and S parameters over a user selected frequency range. The user may also select to have the software find a lumped element model that best fits the Y parameter data.

One example layout is an MMCC with the following characteristics: 35 fingers (18 for Net1 and 17 for Net2), the length of each finger is 26μ, the width of each finger is 0.4μ, and the spacing between fingers is 0.4μ. The capacitor structure was constructed using Metal layers 1 through 5 in a 0.25μ 5 metal layer process. The summarized report for this device is shown in Table 1:

The tool provides information on the Q of the structure, the contribution of each metal layer to overall useful capacitance as well as the parasitic capacitance. Note that in the first part of Table 1 capacitance from a net to itself is listed. This capacitance is due to the distributed nature

of the extraction allowing one segment of the net to couple to another segment of the same net.

Table 1: Simulation results. Net1 and Net2 refer to the two nodes of the capacitor. All capacitance values are in Farads.

Net to Net Coupling Capacitance:

Net 1 → Net 1:	3.1429e-14
Net 1 → Net 2:	4.60008-13
Net 2 → Net 2:	3.1368e-14

Net to Substrate Capacitance:

Net 1 → Substrate:	1.7490e-14
Net 2 → Substrate:	1.8724e-14

Layer by Layer breakdown for Net1

All Layers	5.0900e-13	100.00%
Metal 1	1.0103e-13	19.85%
Metal 2	1.0505e-13	20.64%
Metal 3	1.0025e-13	19.70%
Metal 4	1.0219e-13	20.08%
Metal 5	1.0047e-13	19.74%

Layer by Layer breakdown for Net2

All Layers	5.1017e-13	100.00%
Metal 1	1.0376e-13	20.34%
Metal 2	1.0017e-13	19.63%
Metal 3	1.0518e-13	20.62%
Metal 4	9.7283e-14	19.07%
Metal 5	1.0378e-13	20.34%

Quality Factor and Capacitance Density

Q @ 1.58GHz = 257 (initial result)
Q @ 1.58GHz = 37 (including contact vias)
Cap. Density = 460fF/27.5μ^2 = 0.6fF/μ^2
Parasitic Capacitance = 7.8%

Measurements

The test structures were fabricated in a 0.25μ 5-metal layer process. Measured results from one structure are shown in Table 2. The measured values of trans-capacitance and parasitic capacitance matched the RF-PASS simulation results very well. However, there was initially a big difference in the measured vs. modeled Q. This discrepancy was due to an omission of the contact structure for each terminal from the RF-PASS simulation while not concomitantly adding it to the de-embedding structure for measurement. Thus these contacts became part of the measured results and not part of the simulated results. The contacts consist of 6 parallel via stacks from METAL5 to METAL1. The resistance of 6 parallel vias stacks in each terminal was about 2.5 Ohms – for a total series resistance of 5.0 Ohms. This is significantly greater than the intrinsic finger resistance. Adding the contact structure to the RF-PASS simulation easily compensated for this oversight. The new RF-PASS Q value was predicted to be 37. This matches closely with measured data. Alternatively, de-embedding via resistances in the measurement yielded a Q of 212. This also matches closely with a Q of 257 computed by RF-PASS.

Table 2: Measurement results.

Parameter @ 2GHz	Measures Value
Trans-capacitance – C_{12}	4.67e-13 F
Port 1 Cap. To ground	2.00e-14 F
Port 2 Cap. To ground	2.00e-14 F
Series resistance – R_{12}	5.57 Ω
Q factor at port 1 – Q_{11}	34.5
Q factor at port 2 – Q_{22}	52.0
Q factor after via-R de-embedding	212

Scaling with Process Technology

The layout simulated earlier was scaled to create the additional layouts given in Table 3. The width, length and spacing of fingers were all scaled. Metal and dielectric thicknesses were not changed. As the width and length of the fingers were scaled by the same value, the resistance of each finger will remain approximately constant. The area shrinks very rapidly – with the square of the scaling factor. The smallest finger width and spacing used is 0.08μ which corresponds to a finger length of 5.2μ and an area of 31μ^2. The largest finger width and spacing used is ten times larger at 0.80μ, ten times longer 52.0μ, and one hundred times more area 3091μ^2.

Table 3: Several scaled layouts of the thirty-five-finger comb capacitor were built. Metal and dielectric thicknesses were not scaled with horizontal dimensions.

Finger W/S(μ)	Finger L (μ)	Capactiance (fF)	Density (fF/μ^2)	Parasitic Cap (%)
0.080	5.2	300	9.70	1%
0.100	6.5	321	6.64	1%
0.120	7.8	326	4.69	1%
0.150	9.8	340	3.13	2%
0.200	13.0	362	1.87	3%
0.250	16.3	383	1.27	4%
0.300	19.5	411	0.95	5%
0.400	26.0	473	0.61	8%
0.800	52.0	857	0.28	14%

We see in Figure 2 that parasitic capacitance varies strongly with area. However, the capacitance between the two nodes (trans-capacitance) tends to flatten out as we decrease the area. For narrow finger width and spacing (< 0.3μ) one can get very high capacitance densities– approaching that of gate oxide capacitors while simultaneously getting parasitic capacitance rivaling MIM capacitors. Reliability and voltage withstand capabilities of capacitors with such reduced dimensions could be affected, but have not been analyzed in this paper.

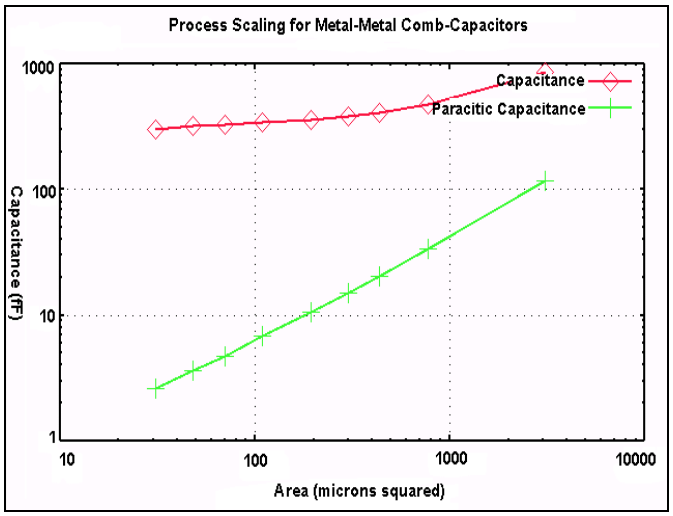

Figure 2: Effect of scaling on capacitance and parasitic capacitance.

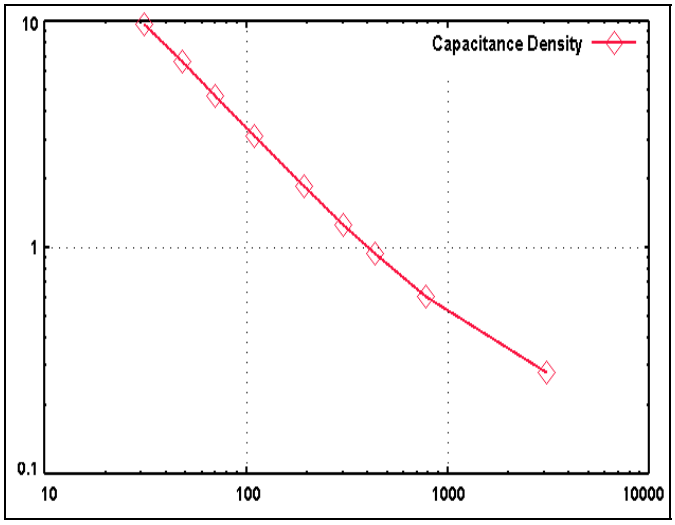

Figure 3: Effect of scaling on capacitance density.

Conclusions

Metal-metal comb-capacitors offer good capacitance density, Q, parasitic capacitance and voltage withstand abilities. The topology chosen here has a capacitqance density of $0.61fF/\mu^2$, a Q of 200 and 8% parasitic capacitance to ground. A simulator capable of quickly modeling all relavent effects including substrate currents, skin and eddy current losses must be used to find an optimum device. A good correlation between simulation and measurement is seen. Given the intrinsically low resistance of the MMCC structure, care needs to be taken to minimize via and contact resistance in the circuit. Future process technologies with the concomitant decrease in metal finger spacing and metal finger width will enable the capacitance density, parasitic capacitance and quality factor values to rival the best on-chip capacitors available.

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