Tools for On-Chip Interconnect Inductance Extraction

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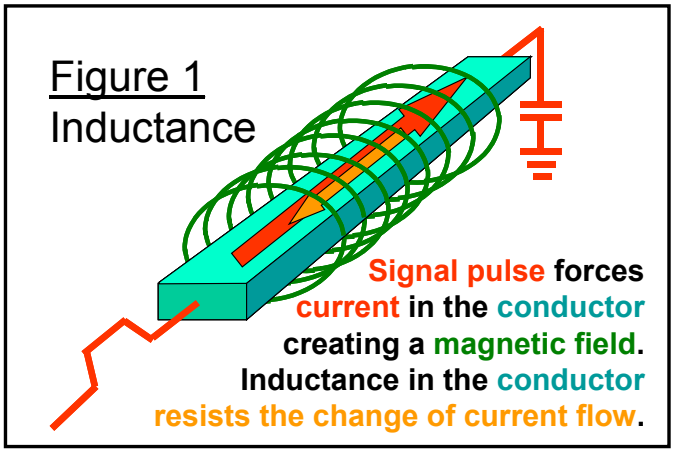
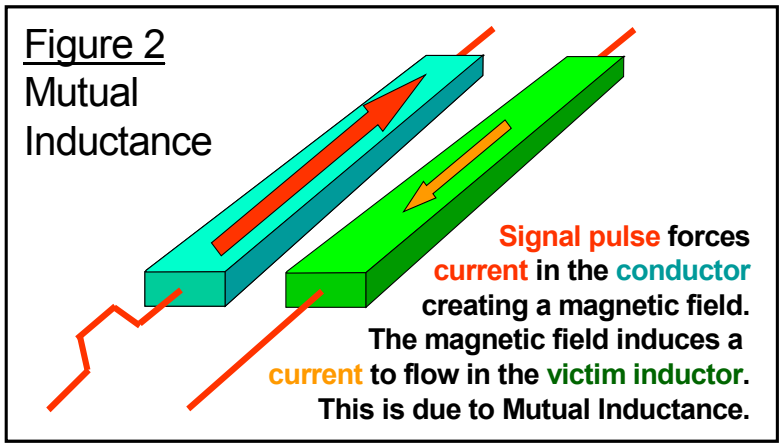
Introduction

For years the focus of analyzing interconnect has been in getting accurate capacitance and resistance parasitics. But what about this parasitic called inductance? Where did it come from and why is there so much interest in it today. Inductance has always been a parasitic in interconnects but it is just starting to become significant in today's DSM high speed SOCs and RFIC designs. OEA International delivers tools which help you understand if un-intentional inductance effects are important in your digital or RF/analog designs and help predict accurate inductances in designs where inductance is designed into circuit components.

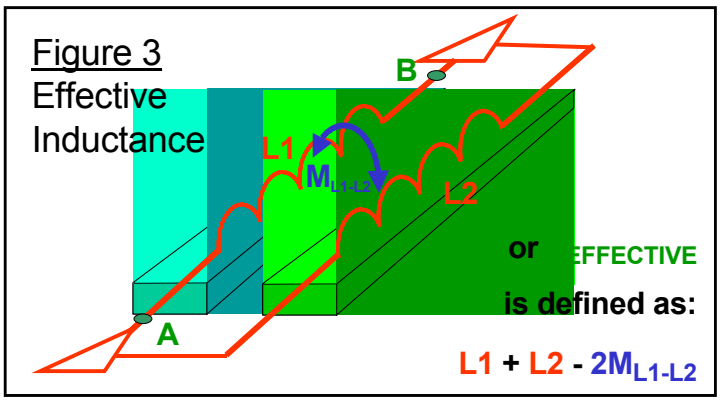
Early research and papers on inductance were published in the book, "Inductance Calculations" by Fredrick Grover (1) and by A.E. Ruehli, from IBM Research (2). Since then many papers and presentations have been written and presented including many by OEA International (3), (4), (5). OEA realized early the importance of inductance for package leads, bonding wires and power planes in 1991 and developed the first commercial 3D inductance solver called **HENRY**. In 1995, OEA also discovered the first chip timing failure due to inductance on a microprocessor chip (5).

When a current is passed through a conductor it creates a magnetic field around that conductor. That magnetic field in turn resists any change in current flow in the conductor. The measure of this property is called inductance. (Fig.1) When the magnetic field influences the current flow on another signal, that effect is measured by mutual inductance. (Fig.2) The impact of the inductance on the circuit performance is primarily dependent on the conductor geometry, which affects the resistance, and the frequency of operation. If the conductor is narrow as in today's DSM technologies, the resistance will be high in comparison to the inductance value. Then, the frequency at which inductance will show a significant effect will be very high, many giga-hertz in some cases. As the conductor width gets wider, the resistance drops rapidly and the frequency at which inductance shows a significant effect can be lowered to the operating frequencies of today's





high performance circuits. Inductance effects on a net cannot be accurately simulated without simulating the inductance return path. A complication of getting accurate signal integrity is that the 'effective' inductance of a net may need to be determined from the self-inductance of the net, the self-inductance of the return-path and the mutual coupling between the two. (Fig.3) Another complexity at very high frequencies is that skin effect and proximity effects must be considered to get an accurate simulation. OEA tools accurately solve for inductance including skin and proximity effects when necessary for RF/analog.



With this stated, the question is when should one be concerned about inductance in their design? The response is not a simple one and for each process and set of design rules there must be an investigation with tools that extract accurate inductance. This paper details the tools and methodologies required for accurate induc-tance modeling.

Tools for On-Chip Inductance Rules Generation

When inductance is to be considered in analyzing a circuit, one can define four useful categories of tools. In the first category are tools that simply guide the designer in how to avoid or control inductance effects in a general way. These tools provide electrical design rules on the permitted combinations of widths, lengths, metal layers, buffers and loads. These electrical design rules are then incorporated into the design flow so that inductive effects can be largely avoided or understood. These tools can be quick and dirty or do a detailed and very accurate analysis. OEA has developed a toolset built around **BUS-AN** and **NET-AN** that can quickly characterize a process technology and provide interconnect guidelines that are specific to available cell libraries and the metal and dielectric stack. This toolset can be used for many interconnect optimization and exploration tasks including, buffer sizing experiments, drive capability studies, buffer repeater determination, signal line and shield width optimization, RC vs. RCLM delay and skew comparisons, frequency sweeps, bus crosstalk studies, same layer and layer-to-layer bus inductance crosstalk, clock-tree and critical path prototypes. **BUS-AN** and **NET-AN** can also be used for design rule generation for place and route tools. Unfortunately, current ASIC flows have no automated way of incorporating these rules into the place and route flow. However, post-layout filters are not difficult to implement for most flows.

Some on chip structures require specialized design planning tools to prevent catastrophic failures of the design due to 'forgotten' or 'ignored' inductance effects. Gridded and shielded clocks are especially difficult to model and optimize without several iterations on the design concept. The consideration of the inductive return path of the clock net is critical to obtain an accurately predicted skew value. One has to consider the inductance of the clock signal, the VDD and VSS shields and the mutual inductance coupling between them. Also, differences in termination of the shields can change the skew values obtained. For this task, OEA has developed the **CLOCK Designer** clock grid-planning tool. This tool allows fast optimization of a clock grid topology to obtain the lowest skew value. Another example of a highly inductive structure requiring preplanning is the IO ring. Ignoring inductance on the IO ring can lead to IO pin signal integrity failures due to simultaneous switching noise and ground bounce. In addition to the need to model inductance on the IO ring, the package inductance must also be included in any IO ring simulation. OEA offers the **RING Designer**

planning tool to bring all of the necessary components together and accurately insure the planned IO ring design will not have simultaneous switching noise and ground bounce problems.

Tools for On-Chip Inductance in Digital Circuits

The second category of tools can be thought of as applying primarily to digital applications. As can be seen in Fig. 4 skew for a digital circuit can vary greatly based on the interconnect model used. Tools in this category are required to be very fast, handle enormous input data sets, and should generate a distributed resistance, capacitance, inductance and mutual inductance spice model. One should be able to adjust how finely the distribution is done by specifying the frequency of the highest input signals – this ensures that the interconnect representation is not excessively large while still accurately representing the signal performance. OEA's **NETAN** pro-duct is currently used to accurately characterize the highest frequency critical nets and to obtain a higher accuracy on critical signal paths for numerous large digital ICs. This includes microprocessors, digital signal processors, graphics processors and network processors. **NETAN** is the only true seamless 3D critical multi-net field simulator, which takes into account the full 3D nature of the problem providing accurate simulation of even the largest and most complex nets. Other formula-based or cut & paste extraction methods do not accurately account for all of the 3D fringing parasitics or inductances, which are significant in deep sub-micron technologies. Thus, parasitics derived from these tools can be off by 50% due to boundary cut errors and extraction rule sets which cannot possibly account for complex 3D effects accurately. **NETAN** employs a fully seamless 3D Laplace/Poisson field solution using the fast proprietary "Cheetah II" solver to extract distributed RCLM models for specified nets. Multi-net simulations produce fully capacitively coupled and inductively coupled distributed RCLM SPICE sub-circuit models. Using these fully coupled models accurate crosstalk and signal integrity simulations can be easily accomplished.

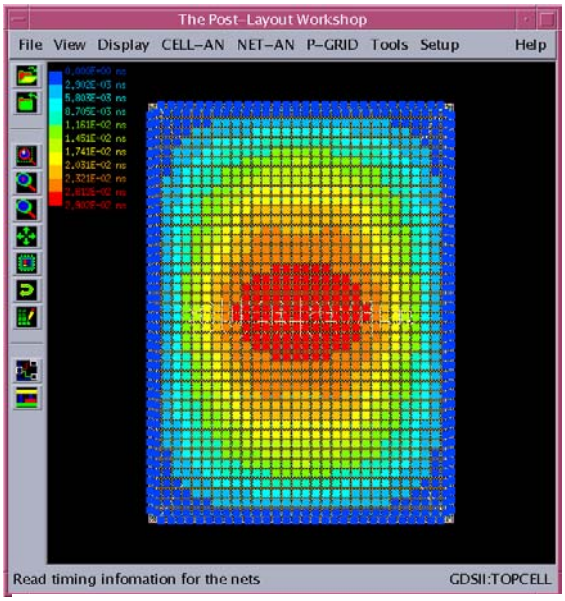


Figure 4. Skew for Clock Grid

RC skew 17.9 ps
RCL skew 48.1 ps
RCLK skew 29.0 ps

Extracting the accurate parasitics including inductance is only the first step. The existence of inductance and mutual inductance breaks most delay calculators, while SPICE type simulators can be slowed by the large size of the extracted parasitic file – some nets might be represented by millions of components. Furthermore, a very large number of mutual inductors can bring SPICE type simulations to a standstill. Therefore, it is important that there be a capability to reduce the size of the netlist or solve it without reliance on traditional SPICE solvers. OEA tools include advanced netlist reduction algorithms built into the **CircuitSmart** product. In addition, OEA has extensive efforts with research universities in developing an advanced simulation engine specific to interconnects that early tests show is many orders of magnitude faster than SPICE while retaining good accuracy.

Tools for RF/Analog Inductive Component Analysis

The third category of tools is for the analysis of passive components. A variety of inductive components is shown in Fig. 5. OEA has two tools in this category: **RF-PASS** and **SPIRAL**. As shown in Fig. 6 these tools must extend the accuracy of the above digital tools in five ways: 1) AC resistance effects due to skin effect and proximity effect must be included. 2) Interaction with conducting substrates (such as silicon) must be modeled. 3) Output formats should include scattering, admittance and impedance parameters as well as spice decks. 4) The capability to find (through automated fitting techniques) small lumped models that faithfully reproduce the detailed behavior of the large distributed spice models. 5) No hard assumptions about the availability of ground reference on the IC may be assumed. Fortunately, these tools are applied to far smaller datasets than are used with digital extractions. Nevertheless, large extraction files can be generated. The size of these files is largely determined by the detail required in the modeling of conducting substrates. Designers in III-V semiconductors and other insulating substrates benefit greatly by having a non-conducting substrate that does not require a complex substrate model. Since they contain a large number of mutual inductors and accuracy is a high priority one must be careful in how the spice decks of such tools are used; typical SPICE solvers based on the Berkeley SPICE sparse matrix solver will often generate inaccurate results. OEA provides a spice-like solver, called **COUGAR** that is highly fast and accurate when solving spice decks that include numerous mutual inductors. Cougar is used to generate scattering, admittance and impedance parameters from the detailed distributed spice deck.

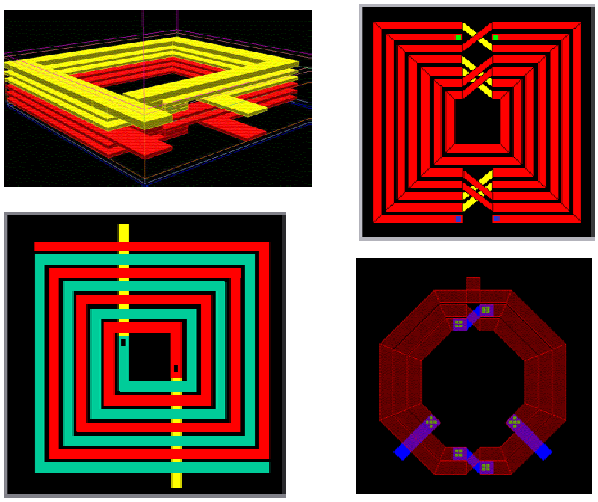


Figure 5. Inductive Components

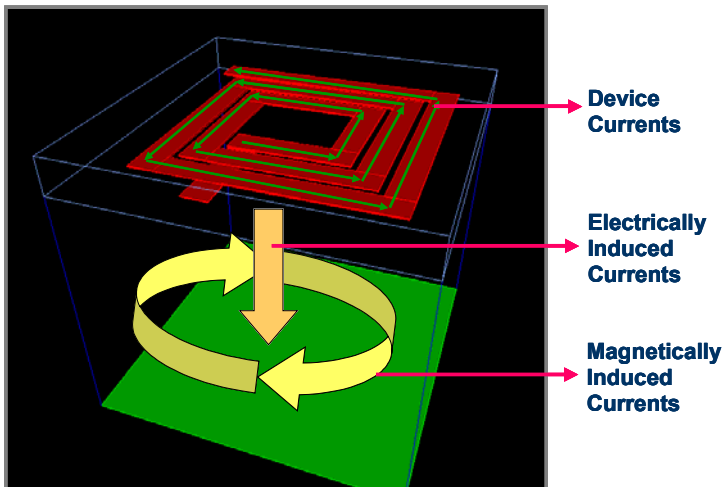


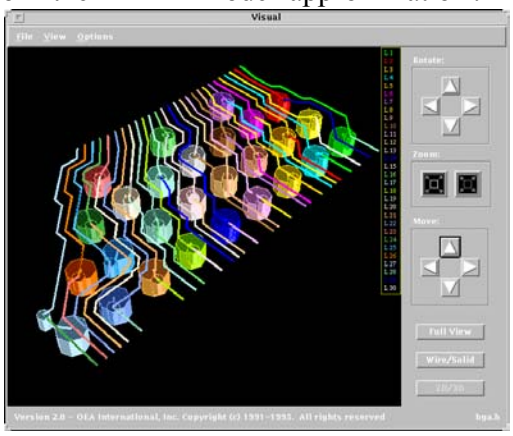
Figure 6.
Passive Components must include Self Capacitance, Capacitance to Substrate, High Frequency Skin Effect etc.

Tools for Package Inductance

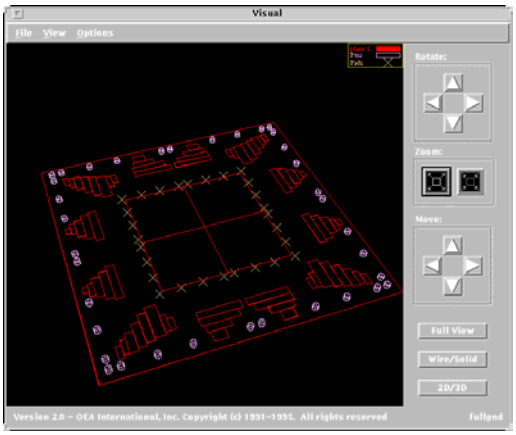
Since the early 1990s, accurate package modeling has been a very important issue in high-speed analog, mixed signal, and digital IC and system designs. Electrical parasitic interactions between the chip and the packaging, and the limiting constraints of the package itself affect the overall internal chip performance in the system design. The inductance of package leads, bond-wires, package ground planes, and even the on-chip IO ring have an

effect on the ability of the package to supply power to the chip at a rate that will prevent ground-bounce and simultaneous switching noise and thus chip failure. Questions such as, 'How many ground and supply pins are required to keep the ground-bounce below a desired level?', 'What is the cross-talk due to the bond-wires?', 'How can one isolate the analog and digital grounds effectively?', 'What can be done to reduce cross-talk and simultaneous switching noise in the case of 'n' simultaneously switching outputs?' or 'How should one design a package to have a given number of simultaneously switching outputs, or if this is not possible, how should the output buffers be designed and where should they be placed?' are becoming common in the design and even in the concept phase of the design of complex high speed ICs.

To answer any of the above questions one needs to have the capability to calculate self and mutual inductance and capacitances of a complex group of three-dimensional structures. In most published literature to date, self and mutual inductance calculations are mainly based on the 'TEM mode approximation'. This approximation is acceptable only for two-dimensional structures that have perfect ground planes. It cannot be used for structures without ground planes where the 'TEM mode' does not exist. The OEA program, HENRY, uses the partial equivalent element calculation method for extracting inductance. **HENRY** calculates very accurate frequency-dependent inductance models of a full package in just minutes.



The complexity of structures that need to be simulated for the packaging application is broad. **HENRY** handles the three-dimensional shapes of curved bond-wires, varying width and angled leads, shaped power and ground planes, and traces with or without ground planes on either side, and complex vias. **HENRY** is a complete solution to calculate self and mutual inductances in a matrix representation, and also supplies an accurate Spice sub-circuit deck of the entire package. Leads can be represented as individual elements for each structure, or as composite lead elements extending from the bonding pad on the IC all the way to where the lead enters the printed circuit board. With this accurate spice model, the package and the I/O portions of the chip could be easily exercised to ensure a successful design.



With **HENRY**, each current path or inductor is defined by giving the centerline and cross-section of the path. Very complex paths can be defined through interface programs or easily entered manually. **HENRY** provides several programs to ease the burden of typing coordinates for complex shapes such as coils, spirals and bond wires. Once the path geometry is defined, **HENRY** then uses the 'energy formulation' definition of self and mutual inductance for calculations. That is, the magnetic energy stored in a conductor, given by the well-known simple relation W=L*I2/2. **HENRY** forces a terminal current 'I' into the conductor and calculates the magnetic energy stored in the conductor under investigation from the current distribution. Since the terminal current 'I' is a known forced current and 'W' is the resulting magnetic energy stored in the conductor, 'L' can be easily obtained. The integral for calculating the energy is quite complex and singular, and has to be performed very carefully for accurate results. A very similar approach is taken

for mutual inductance calculations. The accuracy of **HENRY** has been confirmed both by measurements and by formulas where analytical solutions are available. Computed results for all analytical cases were within 1% of the analytical results published in Frederick Grover's Inductance Calculations book (1). Simulated versus measured lead-frame and PLCC cases were within 10-15%. From these confirmations, it can be deduced that the methods are valid and can be applied to all similar cases with relative confidence. The overall goal of package designers is to reduce the effective inductance for the power and ground supply pins to prevent ground bounce and simultaneous switching noise. Since a plane gives the minimum inductance between two points, introducing power and ground planes between the output driver terminals and the system power supply is a common design methodology used in demanding package applications. Since the effective inductance between the output drivers and the supply is the function of the three-dimensional current distribution, it is affected by the number of planes, their physical geometry and their geometrical configuration in addition to the number of pins and their arrangement within planes that connects them to the system power supply. Therefore, the problem is complex and cannot be reduced by only calculating effective inductance between two or more points on a single plane or analyzing the structure one plane at a time basis. In **HENRY** a program called **PG-PLANE** solves all planes, vias and pins as a unified problem and generates a gridded inductive (n+1) port Spice sub-circuit network which represents the power and ground configuration where all the inductive elements are coupled and lossy. This is then reduced by another **HENRY** program, **simplify**, to an effective inductance between PCB pins and the chip bond-wire contacts. This makes it possible for spice to be run in a reasonable amount of time for a full package.

Conclusion

Inductance does not have to be such a mystery when you utilize OEA tools. The effects of inductance can be accurately simulated and understood for any set of process technology and design rules. Prediction of inductance effects through pre-simulation is possible and strongly advised to avoid problems. Power and ground networks cannot be assumed perfect when calculating signal delays.

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