# A General and Comparative Study of RC$^{(0)}$ , RC, RCL and RCLK Modeling of Interconnects and their Impact on the Design of Multi-Giga Hertz Processors


**by**

**O. Ersed Akcasu, Onur Uslu, Nagaraj NS*, Tufan Colak, Stephen Hale** and Edmund Soo**

**OEA International, Inc.**
**155 East Main Avenue, Suite 110**
**Morgan Hill, CA95037**
**Tel. (408)-778-6747, Fax. (408)-778-6748**
***email:ersed@oea.com***

**Texas Instruments, Inc.***
**12500 TI Boulevard, MS 8635**
**Dallas, TX 75243**
**Tel. (214)-480-2843, Fax. (214)-480-2752**
***email:nsnr@ti.com***

**Advanced Micro Devices****
**One AMD Place**
**Sunnyvale, CA94088**
**Tel. (408)-774-7769, Fax. (408)-774-7701**
***email:stephen.hale@amd.com***

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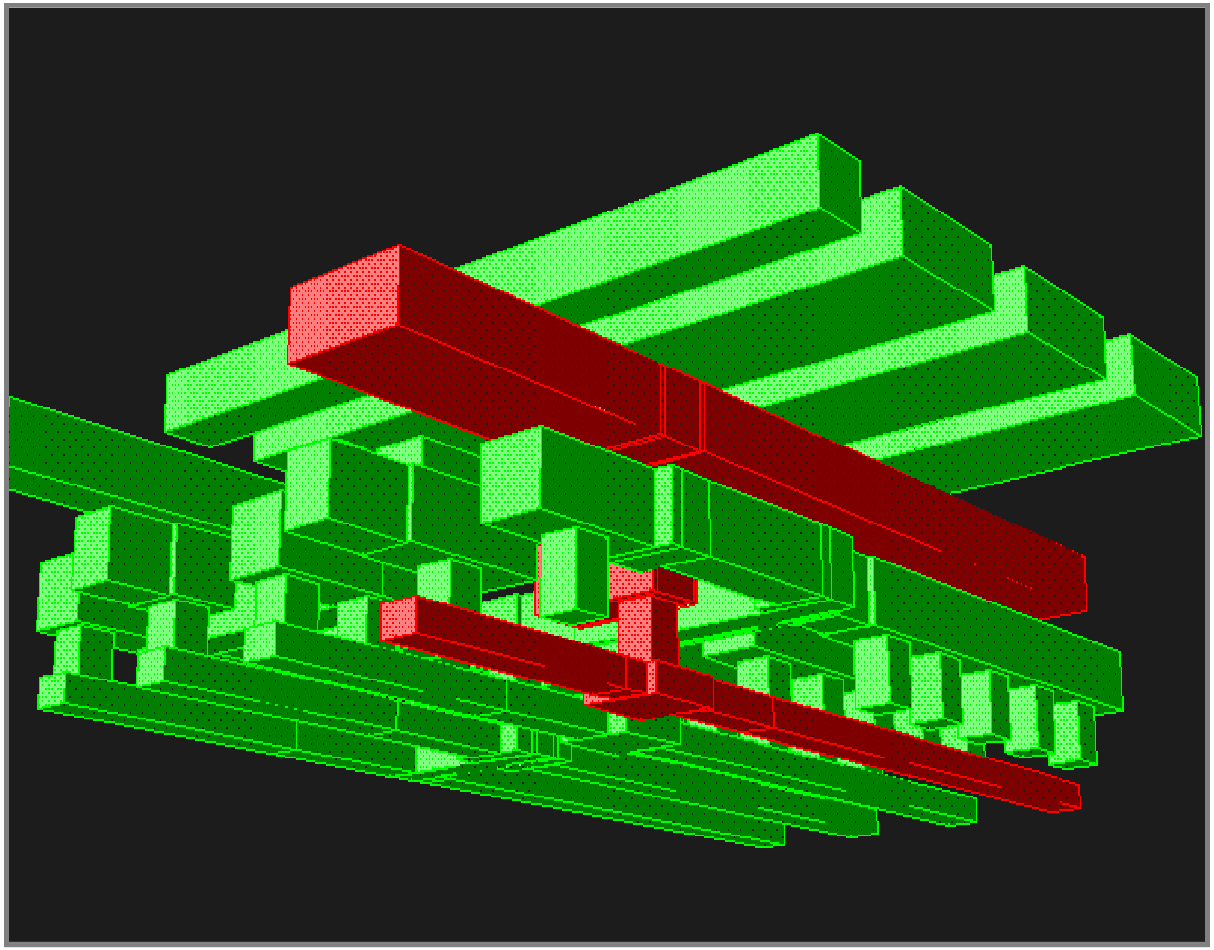
**Alla Toy, OEA International, Inc.**

# AGENDA

1. Interconnect Parasitic Extraction Complexity in Historical Perspective.
2. The Simplest and Most Used Extraction: $C^{(0)}$ and $RC^{(0)}$ Signal Parasitic Extraction Under the Assumption of "All" Proximity Interconnect Geometry and Substrate Ideal Ground.
3. General Inductance Overview.
4. On-Chip Inductance Effects, which Nets Displays Inductive Effects more than others, and Needs to be Modeled Including Inductance.
5. RC, RCL and RCLK with and without Ideal Ground.
6. Inductive effects on Multi-Level Clock-Grids with Shields.
7. Inductive Effects on Cross-Talk for Complex Buses with Shields.
8. Simulation of On-Chip Decoupling for Buses for Different Packaging Schemes.
9. Over-all Methodology of Designing Interconnect Networks for High Performance IC's with "Needed" Complexity.
10. Conclusions.

# Capacitance Calculation



$$C = Q / V$$

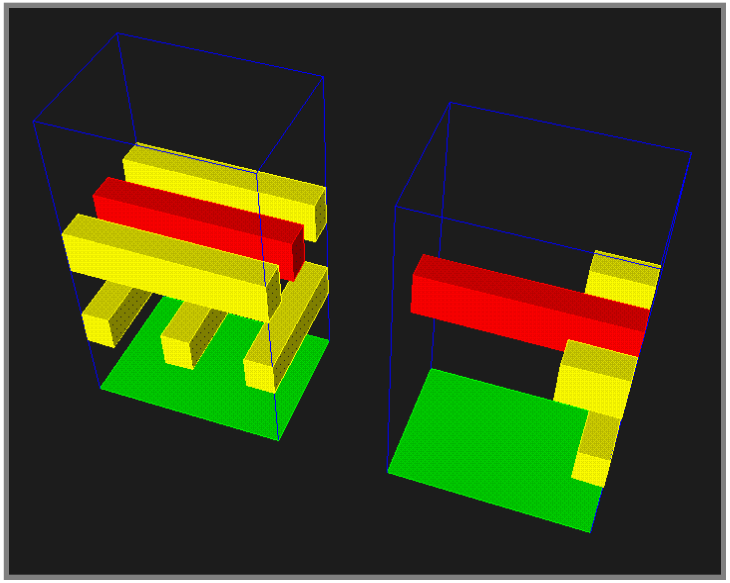
$$\nabla(\varepsilon \nabla V) = \rho$$

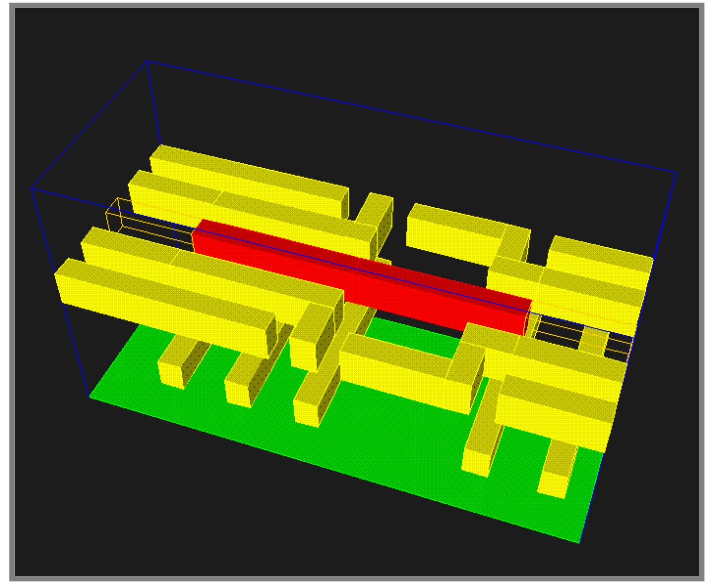
$$\vec{E} = -\nabla V$$

$$\vec{D} = \varepsilon \vec{E}$$

$$Q = \iiint_{\Omega} \rho \, d\nu = \oint\!\!\oint_{\Gamma} \vec{D} \cdot d\vec{s}$$

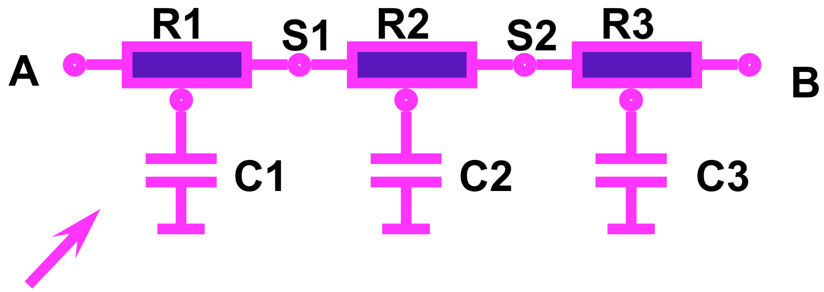
# Comparison of Full 3D Versus 3D Cut & Paste Extraction

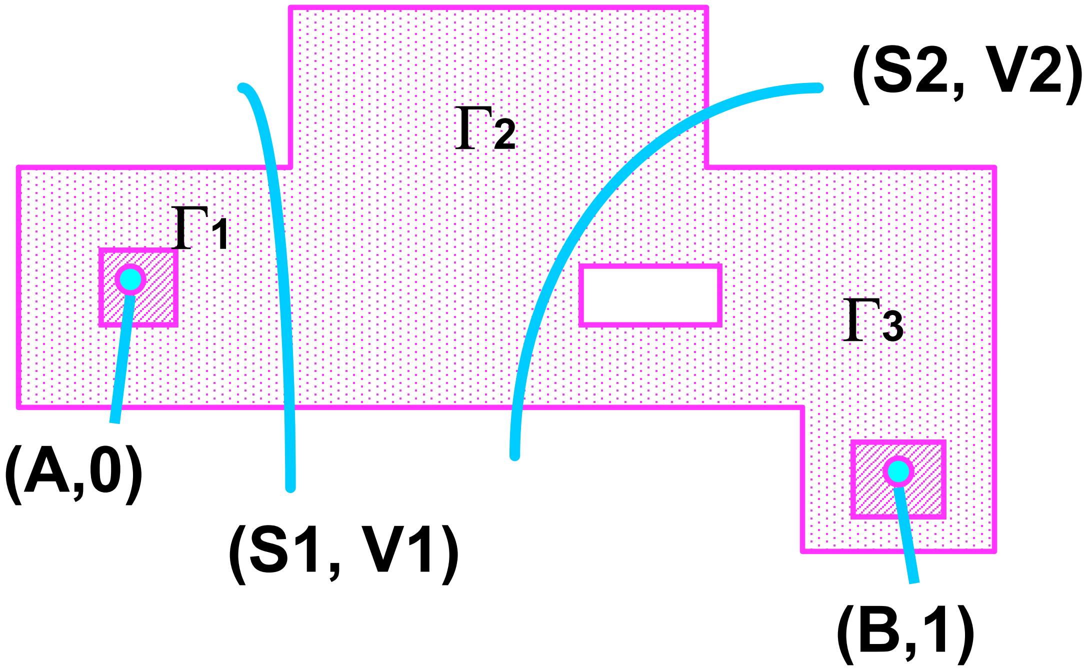




| Cap (fF) | Cut & | Paste Method | | Full 3D | Cut & Paste | Full 3D | Cut & Paste |
|---|---|---|---|---|---|---|---|
| | Sect 1 | Sect 2 | Both | Method | Method | Method | Method |
| Window | 1 μ | 1 μ | 1 μ | 1 μ | Error | 2 μ | Error |
| C11 full | 0.847 | 0.443 | 1.290 | 1.624 | 21% | 1.725 | 25% |
| C12 | 0.847 | 0.400 | 1.247 | 1.603 | 22% | 1.705 | 27% |
| C11 gnd | 0.001 | 0.043 | 0.044 | 0.021 | 109% | 0.020 | 118% |

# Resistance Calculation




$$R = V / I$$

$$\nabla \vec{J} = 0$$

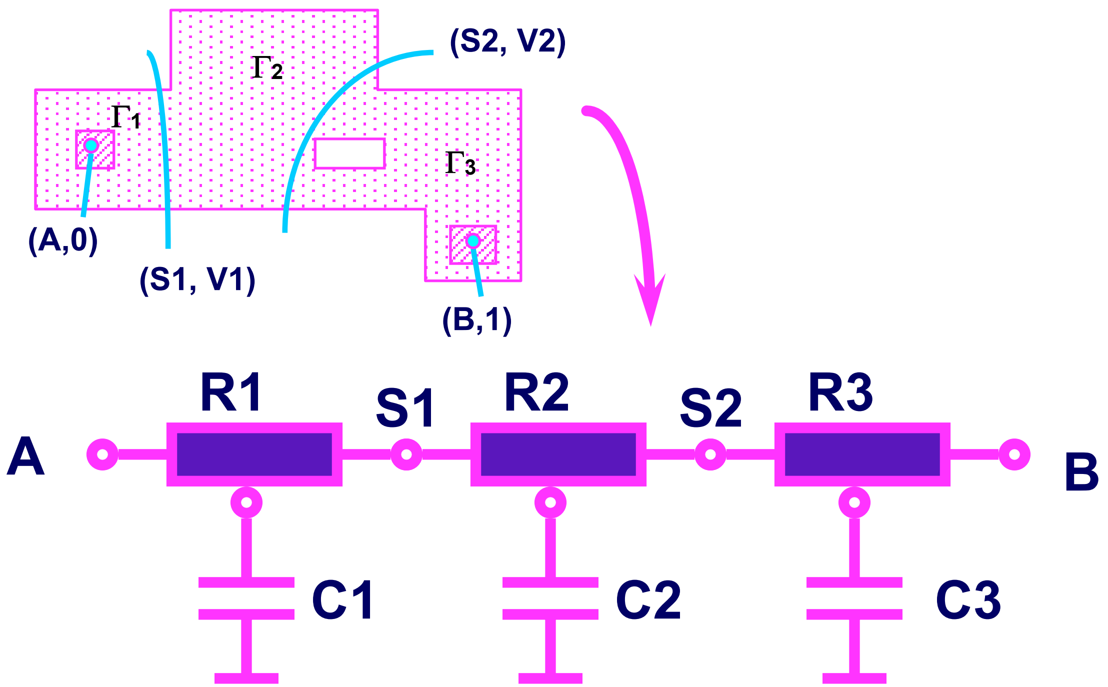
$$\vec{J} = \sigma \vec{E}$$

$$\vec{E} = -\nabla V$$

$$\nabla (\sigma \nabla V) = 0$$

$$I = \iint_S \vec{J} \cdot d\vec{s}$$

# Calculating Capacitance of the Resistance Regions

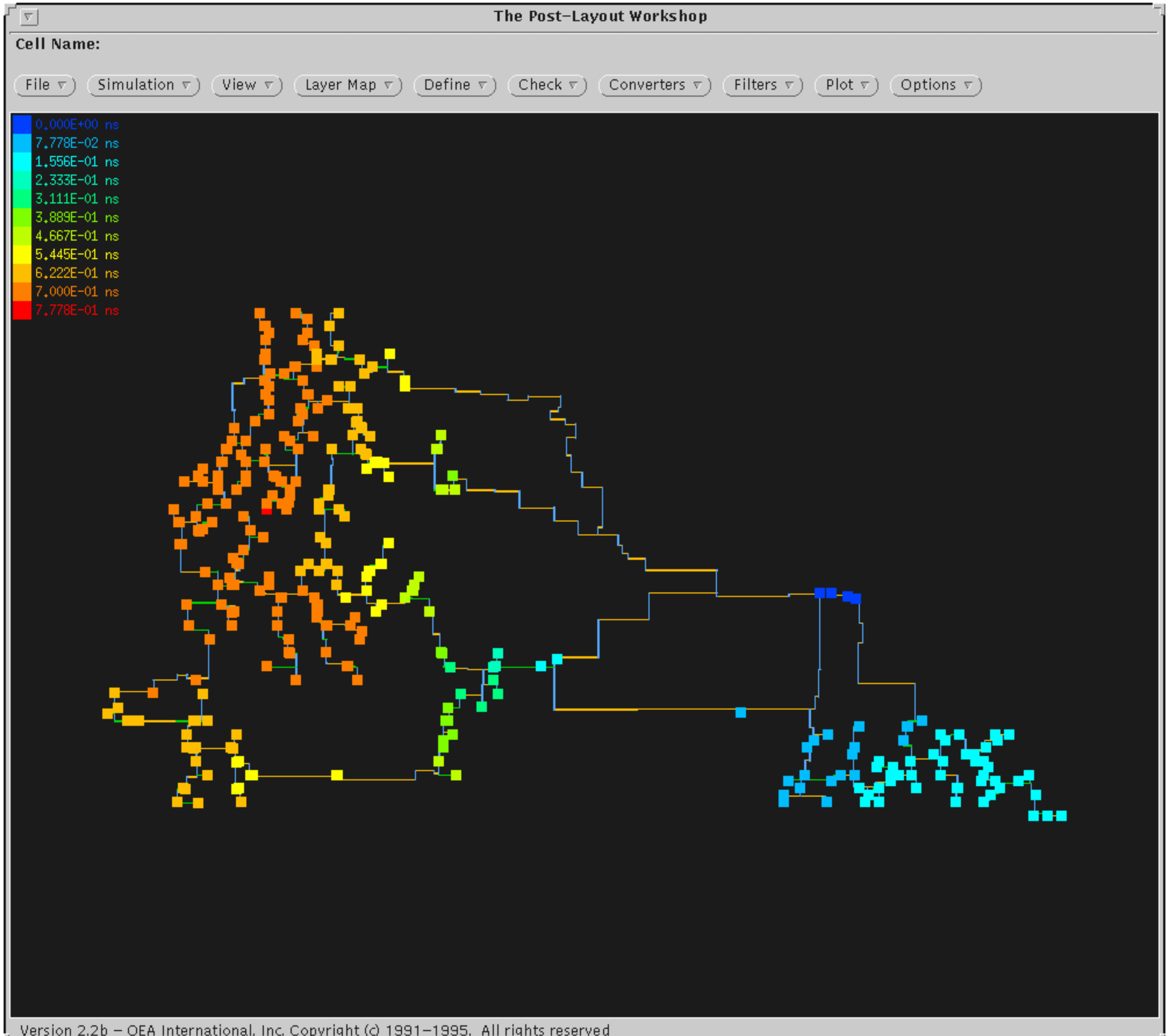



from

$$\nabla(\varepsilon\nabla V) = \rho$$

$$Q_1 = \oint\!\!\oint_{\Gamma_1} \vec{D}\cdot d\vec{s}, \qquad Q_2 = \oint\!\!\oint_{\Gamma_2} \vec{D}\cdot d\vec{s}, \qquad Q_3 = \oint\!\!\oint_{\Gamma_3} \vec{D}\cdot d\vec{s}$$

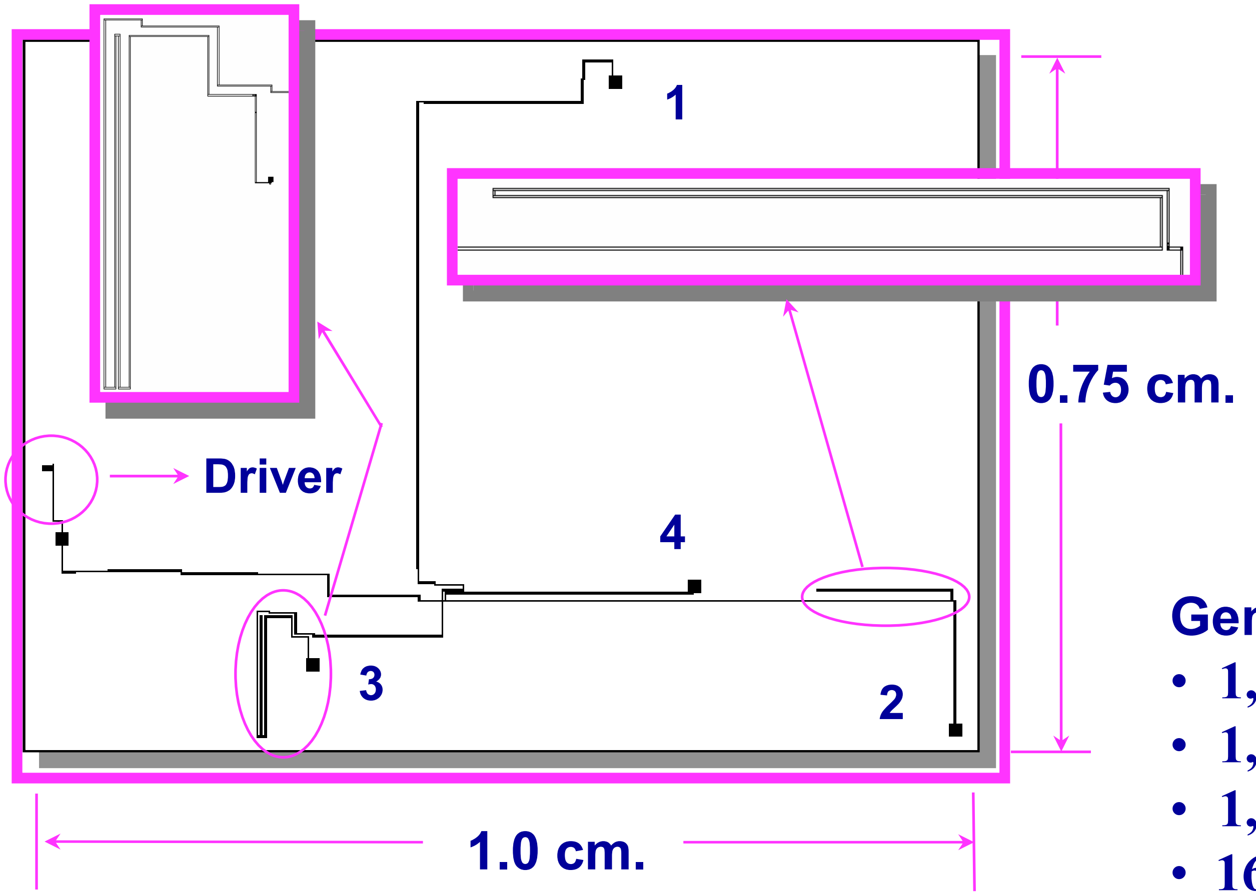
# Delay Distribution on the Net: TFUN_MRXC_BUFF




## Net Statistics

**Drivers = 2**
**Loads = 275**
**Net Cap = 5.1 pF**

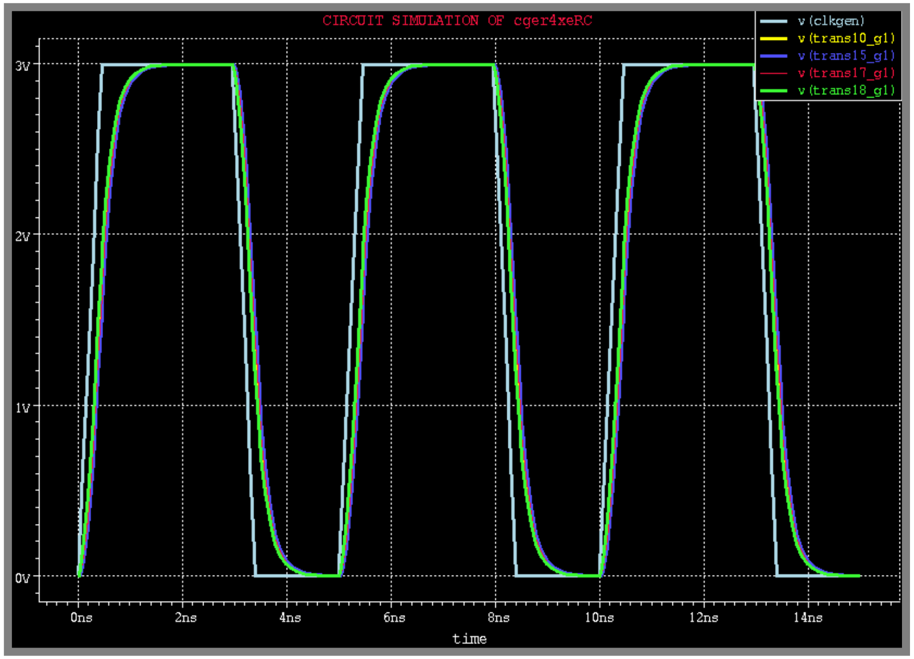
# Level 1 Clock Net for a Major Microprocessor Chip

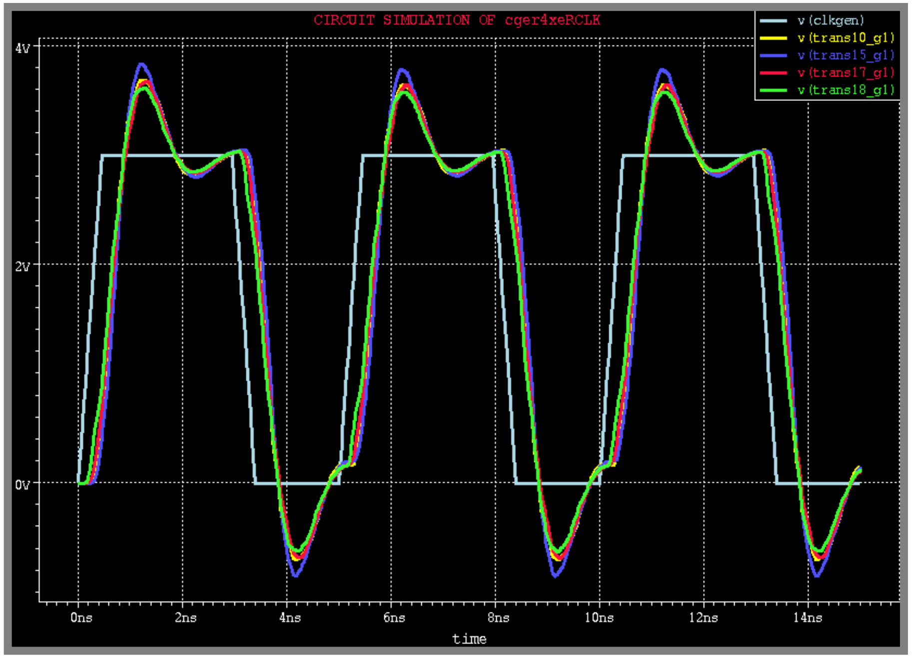



**Generated spice deck**

- 1,401 resistors
- 1,001 inductors
- 1,084 capacitors
- 16 gate capacitance loads

# Comparison of Wave Forms with & without Inductance

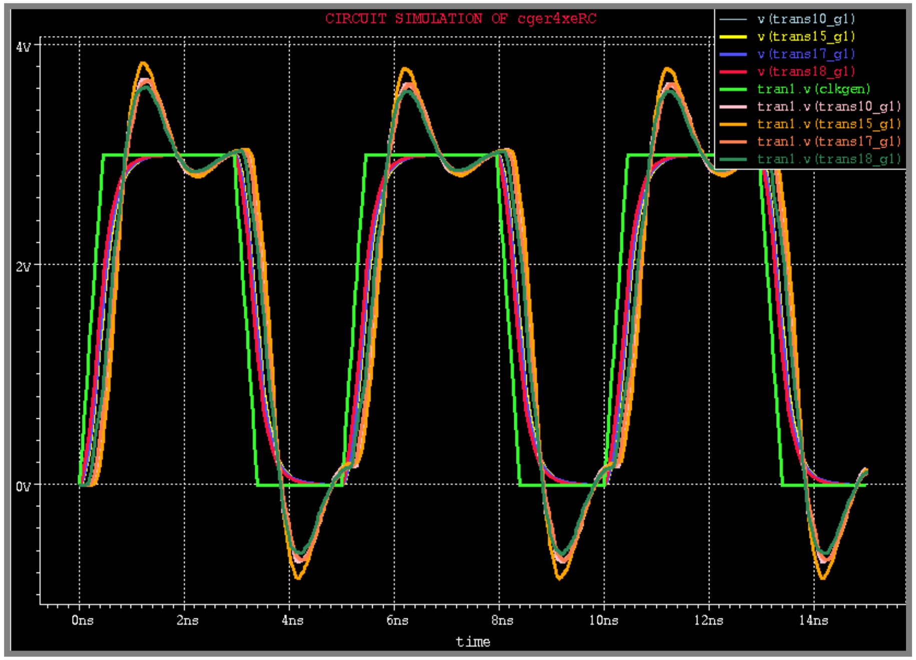


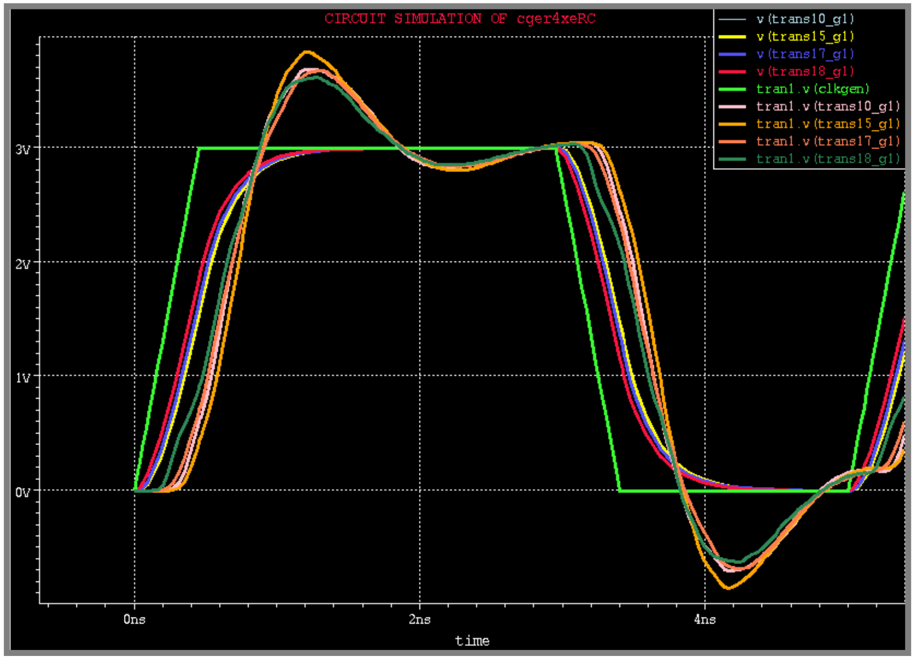




0.45 nS rise and fall times (0 - 3 Volt Transition)

Four, 50fF Loads, 200 MHz Clock

# Comparison of Wave Forms with & without Inductance (Superimposed)




0.45 nS rise and fall times (0 - 3 Volt Transition)

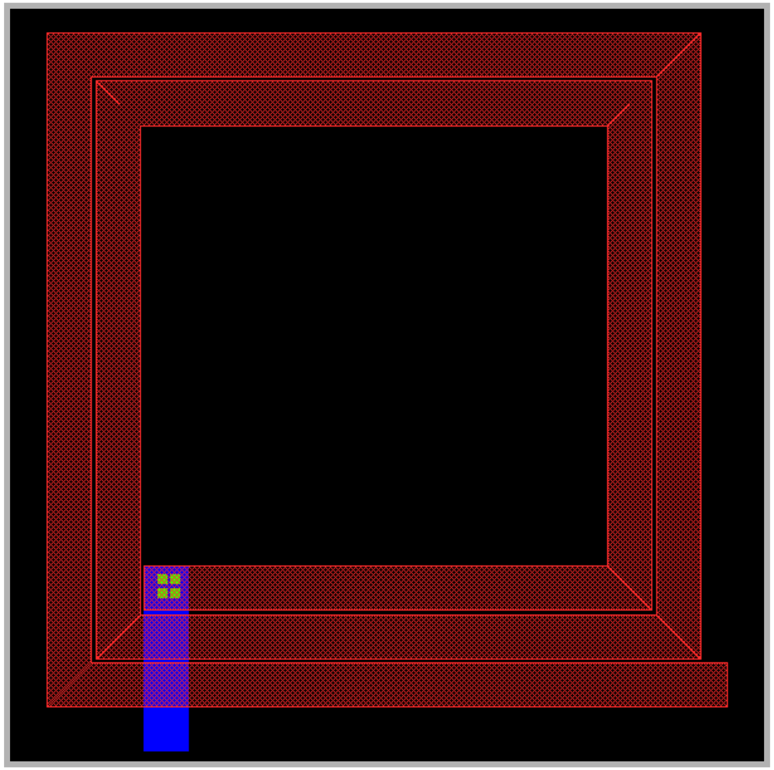
Four, 50fF Loads, 200 MHz Clock

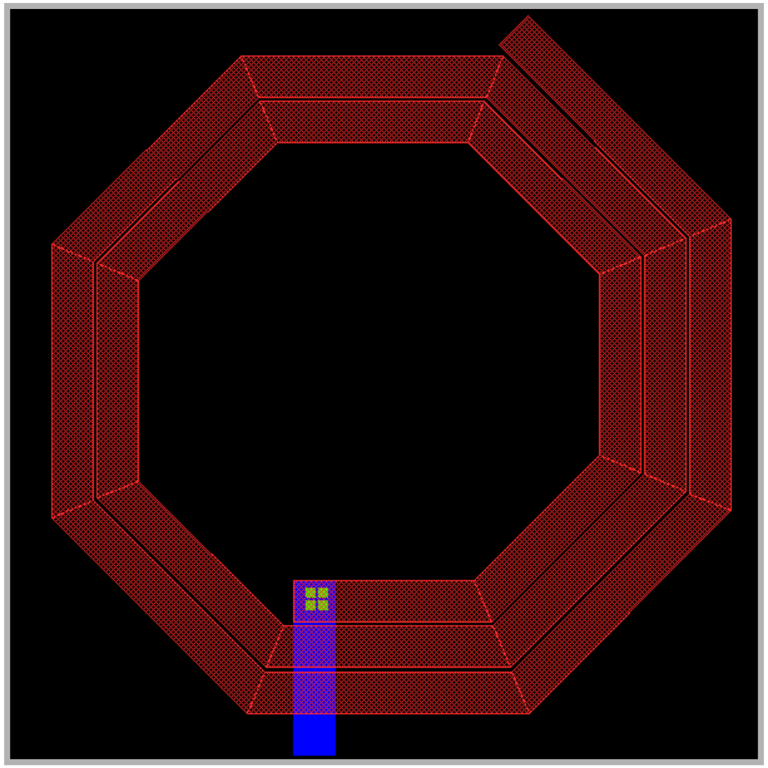
# Delay and Skew Comparison

| | $T_{d1}$ (ps) | $T_{d2}$ (ps) | $T_{d3}$ (ps) | $T_{d4}$ (ps) | Skew(ps) |
|---|---|---|---|---|---|
| RLC | 422 | 479 | 410 | 360 | 119 |
| RL(2*C) | 640 | 732 | 619 | 539 | 193 |
| RL(0.5*C) | 278 | 315 | 270 | 248 | 67 |
| RC | 275 | 295 | 276 | 228 | 67 |
| R(2*C) | 499 | 543 | 500 | 404 | 139 |
| R(0.5*C) | 162 | 171 | 162 | 138 | 33 |
| C | 0 | 0 | 0 | 0 | 0 |

Delay and Skew Comparison for the Level 1 Clock Net for different model complexities and effects of under and over estimating the distributed capacitances.

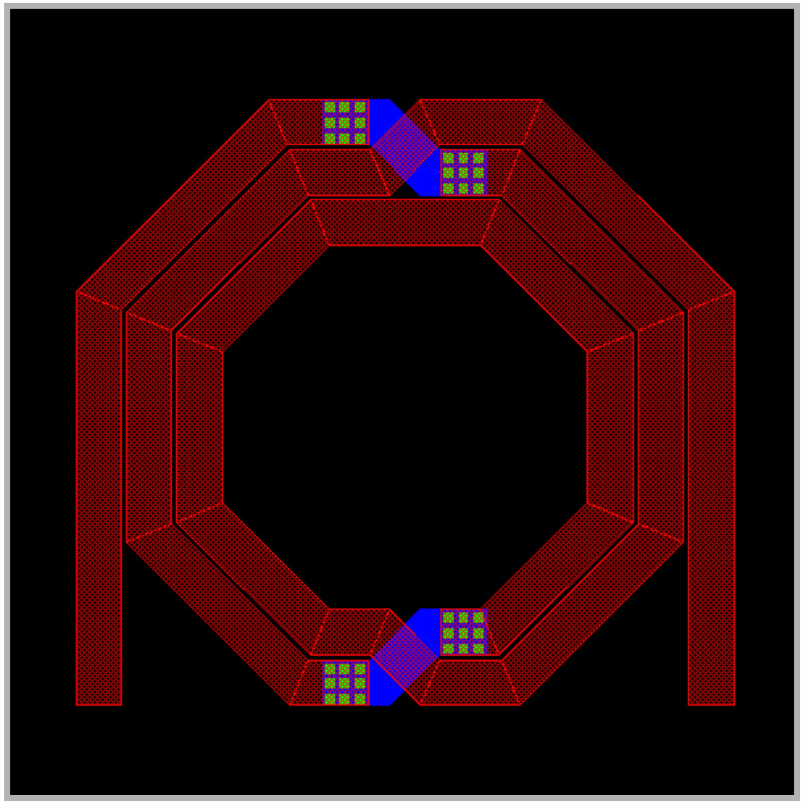
# Standard Inductors: 4 sided / 8 sided

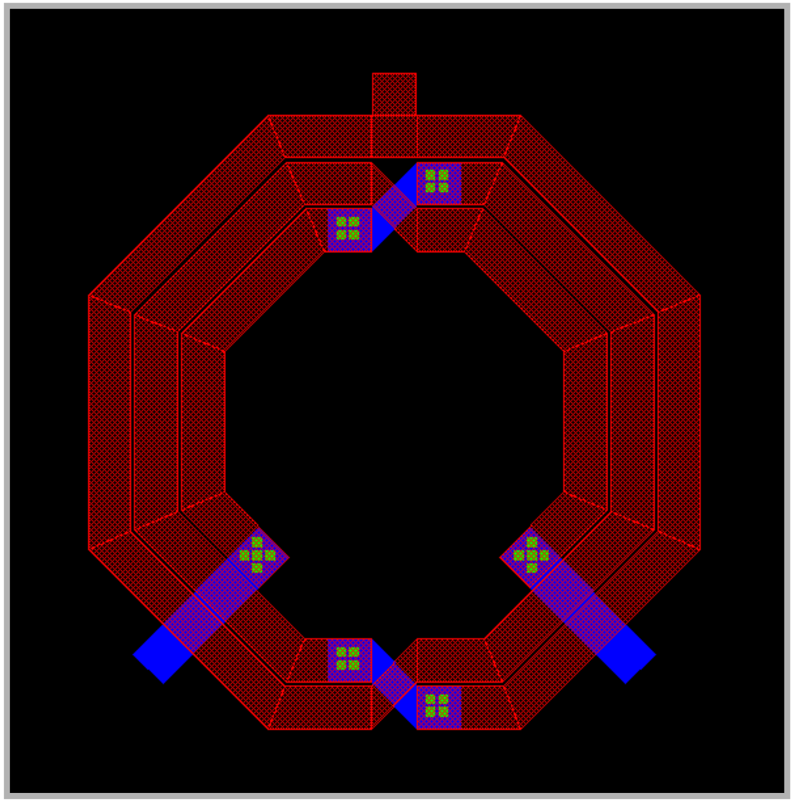




- **Usually uses top metal layer for winding**
- **Can use multiple metal layers in parallel**
  - Lowers series resistance
  - Increases capacitance
- **Can use multiple metal layers in series (coil)**

# Symmetric Differential Inductors





- **Symmetric Center Tapped Inductors instead of 2 'uncoupled' inductors:**
  - Easily defined center tap
  - Reduced chip area
  - Higher Q (reduced substrate losses)
  - No need to model parasitic coupling

# Inductance Issues

IEDM95

## IEDM 1995

**"NET-AN" a FULL THREE-DIMENSIONAL PARASITIC INTERCONNECT DISTRIBUTED RLC EXTRACTOR for LARGE FULL CHIP APPLICATIONS**

- Osman Ersed Akcasu - OEA International, Inc.
- Jesse Lu - OEA International, Inc.
- Alexander Dalal - Sun Microsystems, Inc.
- Sundari Mitra - Sun Microsystems, Inc.
- Lavi Lev - Sun Microsystems, Inc.
- Nader Vasseghi - Silicon Graphics, Inc.
- Aleksandar Pance - Sun Microsystems, Inc.
- Hem Hingarh - Sun Microsystems, Inc.
- Haris Basit - Rockwell International Corp

**Case Study of On-Chip Inductance Effects (extraction and analysis)**

SEMATECH FSA Modeling Workshop May 24, 1999

by
Osman Ersed Akcasu

OEA International, Inc.
3235 Kifer Road, Suite 300
Santa Clara, CA 95051
Phone: 408-738-5972
Fax: 408-738-2017
*ersed@oea.com*

OEA International, Inc. 1

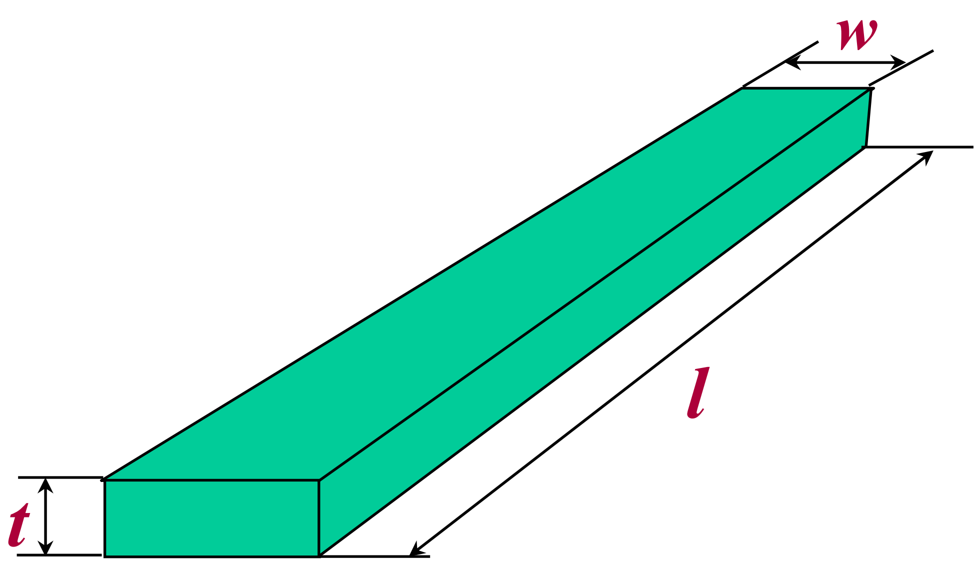
**Impact of the On-Chip Inductive Effects on the Power Distribution Networks for Simultaneous Switching Noise and Ground Bounce Analysis for High Speed Processor Design**

IMAPS Advanced Technology Workshop
on Next Generation IC and Package Design
July 15-17, 1999

by
Osman Ersed Akcasu, Mehmet Tepedelenlioglu
and Kerem Akcasu

OEA International, Inc.
3235 Kifer Road, Suite 300
Santa Clara, CA 95051
Phone: 408-738-5972
Fax: 408-738-2017
*ersed@oea.com*

# Inductance of a Rectangular Conductor




$$L(\mu H) = 0.002l \left\{ \ln\left[\frac{2l}{(w+t)}\right] + 0.5 - k \right\}$$

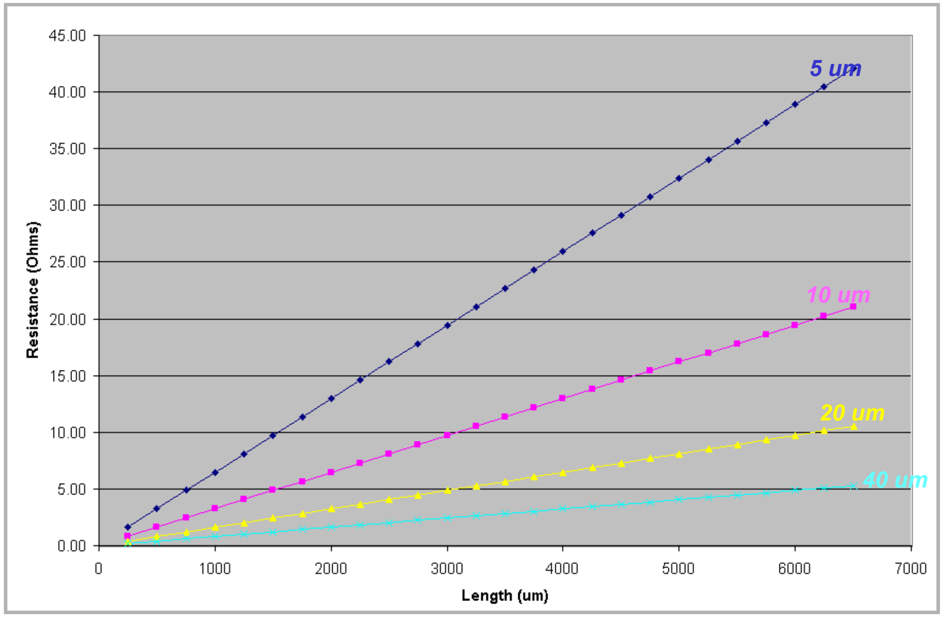
Where $k = f(w,t)$

$0 < k < 0.0025$

$l, t, w$ in cm

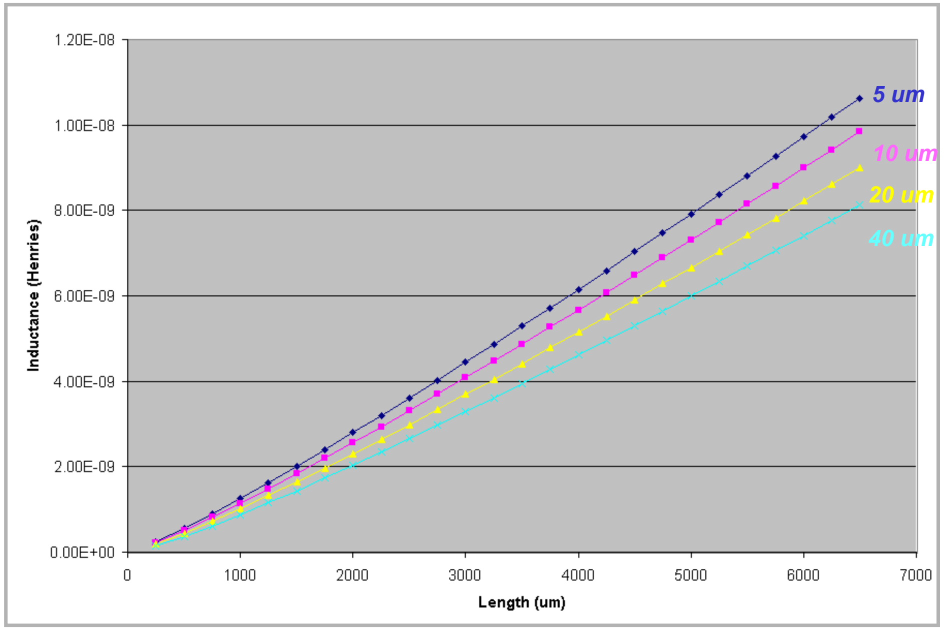
$$R(\Omega) = \frac{\delta l}{(w\ t)}$$

$$Z(j\omega) = R + j\omega L$$ Where $\omega = 2\pi f$




## DC Resistance vs. Length at Various Widths (1 $\mu$m Thick Aluminum)

## Inductance vs. Length at Various Widths

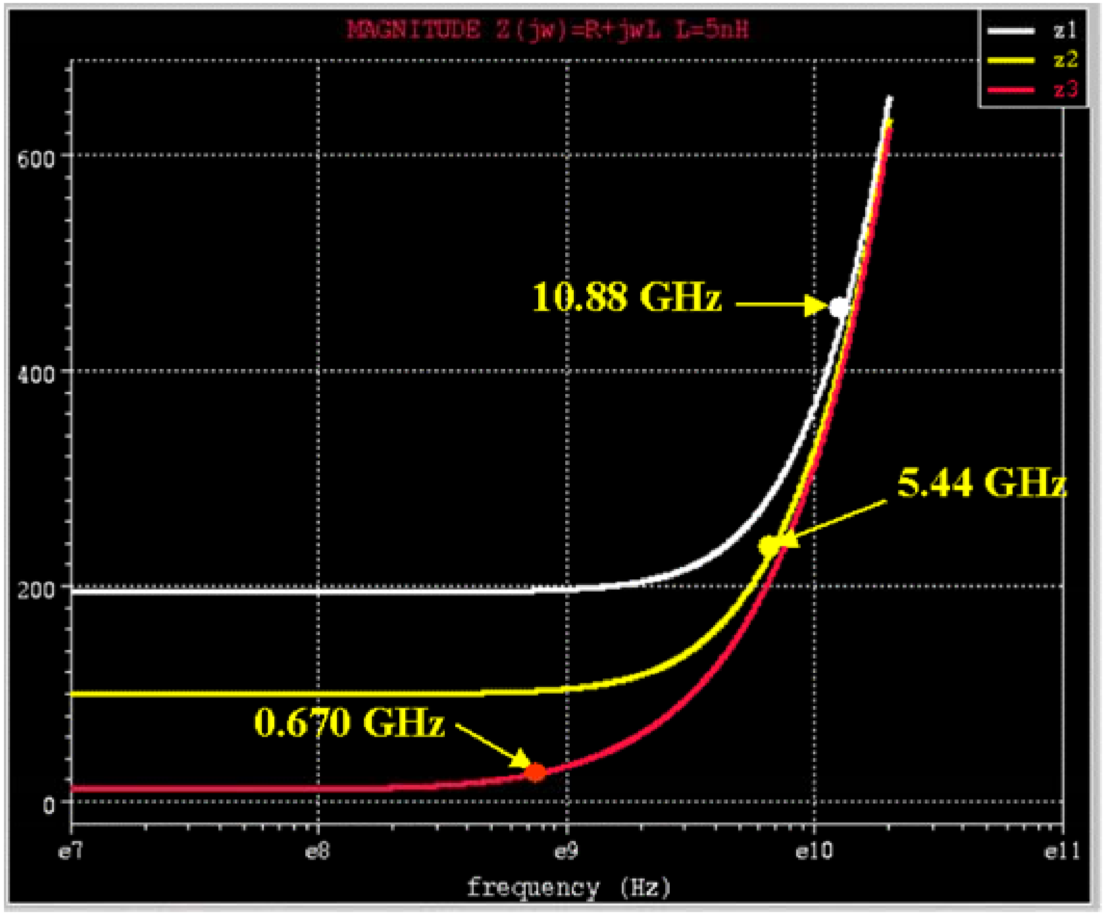


# Inductive Behavior of 5nH Line as a Function of Width

$$\delta = 3.24 \cdot 10^{-6} \Omega \ cm$$

$$t = 1 \ \mu \ , \quad L = 5 \ nH$$

| | | |
|---|---|---|
| $w = 0.5\mu$ | $l = 3013\mu$ | $R = 195.2\Omega$ |
| $w = 1\mu$ | $l = 3109\mu$ | $R = 100.7\Omega$ |
| $w = 10\mu$ | $l = 3821\mu$ | $R = 12.38\Omega$ |




$$f_{pass} = \frac{R}{2\pi L} = \frac{\delta}{0.002 w \, t \, [\, ln \left( \frac{2l}{w+t} \right) + 0.5 - k \,] \, 2\pi}$$

# Q and $f_{pass}$ of a Rectangular Wire

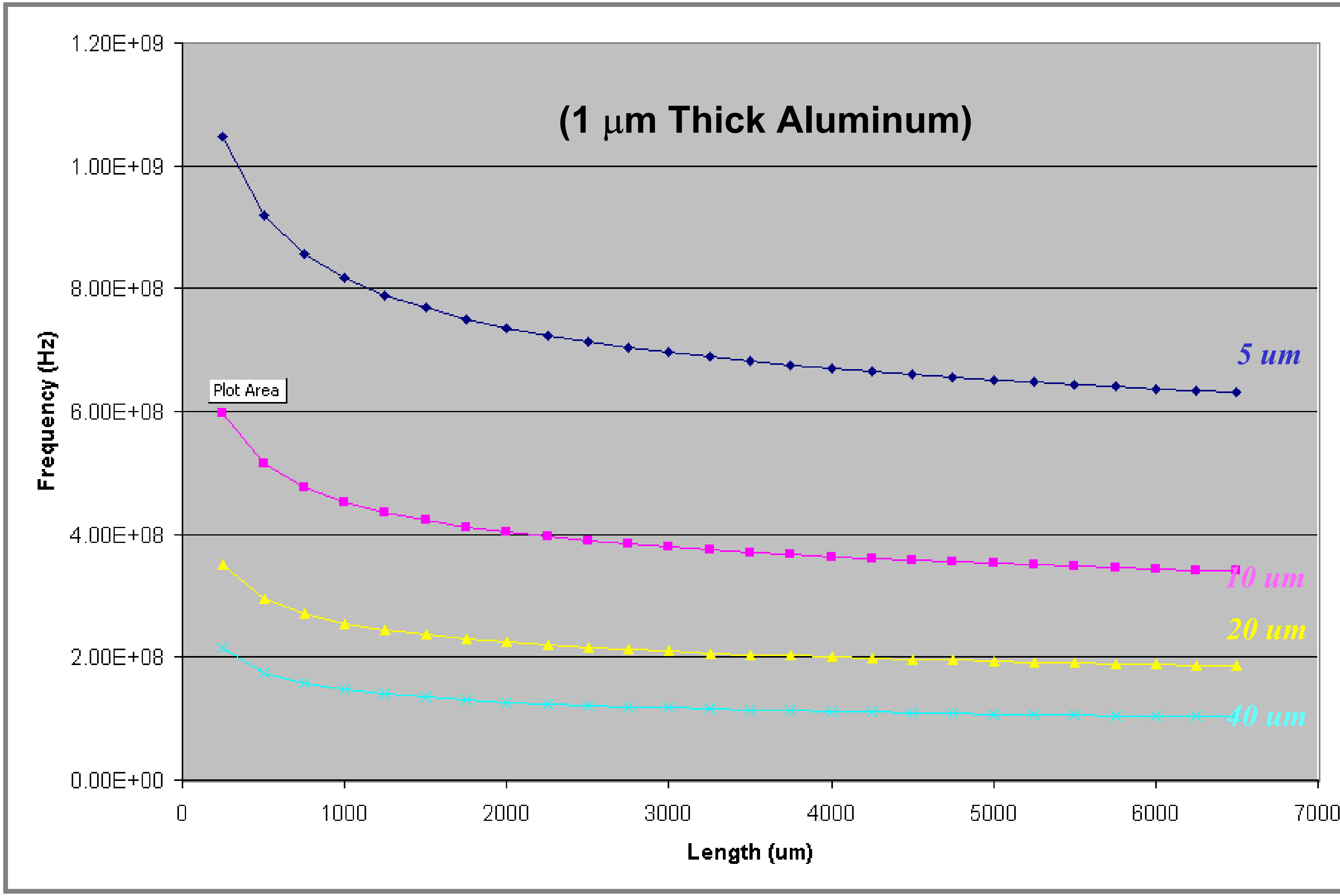
$$Q = \frac{I_m[Z(j\omega)]}{Re[Z(j\omega)]} = \frac{L\omega}{R}$$

$$Q = \frac{0.002wt\left[\ln\left(\frac{2l}{w+t}\right) + 0.5 - k\right] 2\pi f}{\delta}$$

[Reactance = Resistance] when $Q = 1 \Rightarrow f_{pass}$

$$f_{pass} = \frac{R}{2\pi L} = \frac{\delta}{0.002wt\left[\ln\left(\frac{2l}{w+t}\right) + 0.5 - k\right] 2\pi}$$

# Maximum Frequency at Which One Can Ignore Inductive Effects in a Wire



# Partial Inductance Concept

**Six Self Inductances:** $L_1, L_2, L_3, L_4, L_5, L_6$

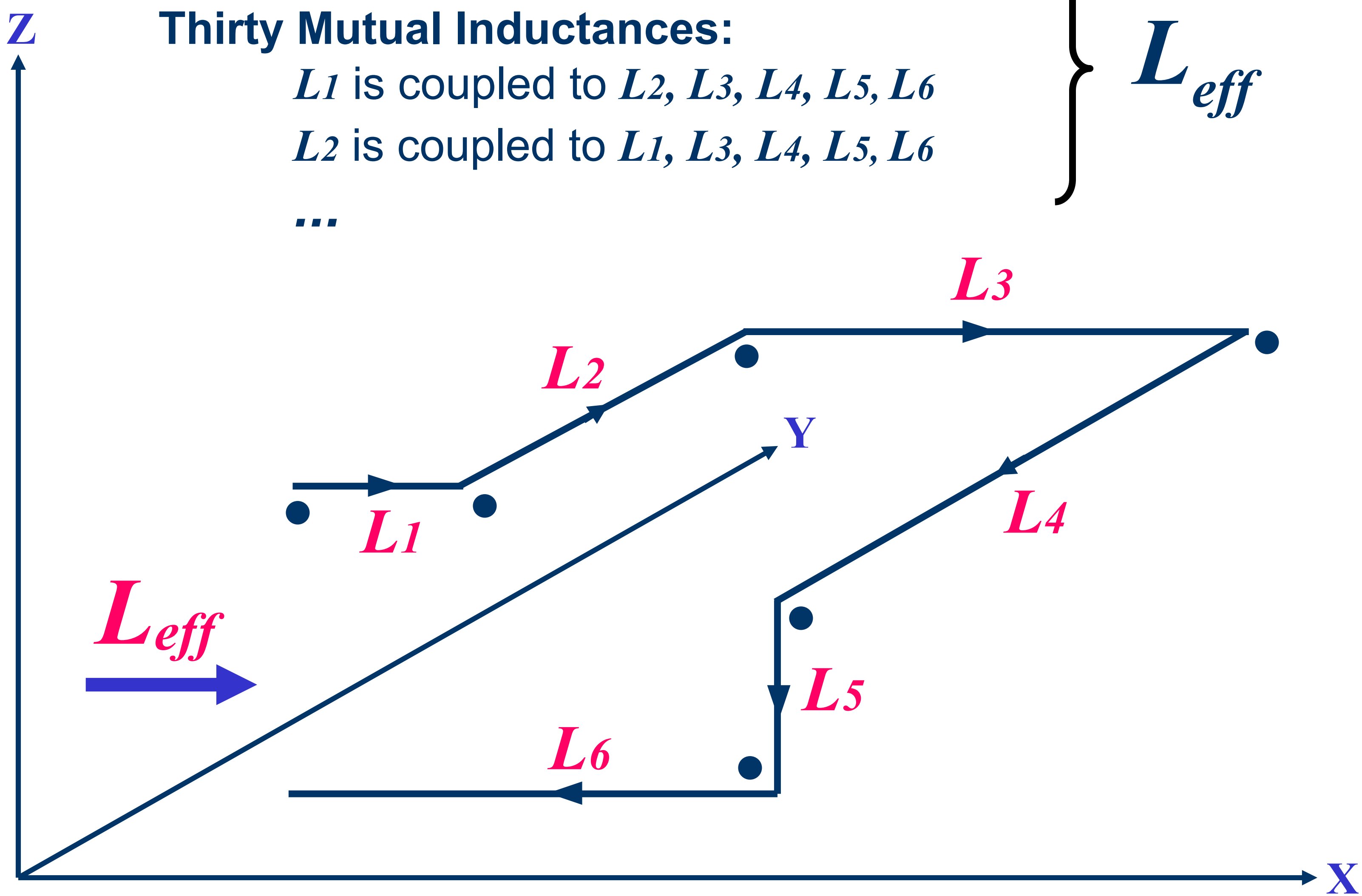
**Thirty Mutual Inductances:**

$L_1$ is coupled to $L_2, L_3, L_4, L_5, L_6$

$L_2$ is coupled to $L_1, L_3, L_4, L_5, L_6$

...

} $L_{eff}$



# Inductance Matrix Representation

$$\begin{bmatrix} L11 & L12 & \ldots\ldots\ldots\ldots & L16 \\ L21 & L22 & \ldots\ldots\ldots\ldots & L26 \\ \vdots & & & \\ L61 & L62 & \ldots\ldots\ldots\ldots & L66 \end{bmatrix}$$

$$L_{eff} = \sum_{i=1}^{n} \sum_{j=1}^{n} L_{i,j}$$

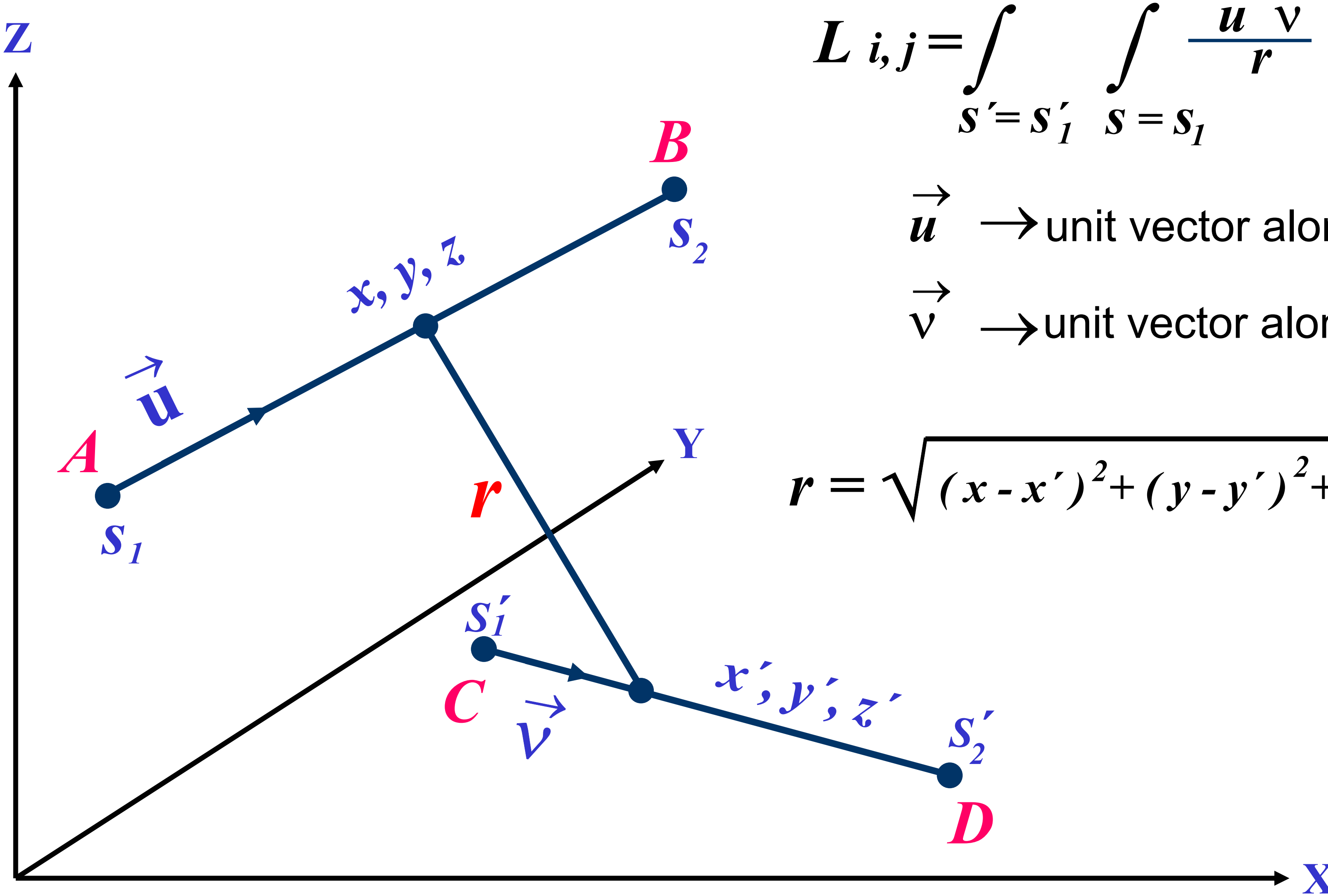
$$L_{i,j} = L_{j,i}$$

→ Self Inductance
Diagonals > 0

Off Diagonals
Mutual Inductance

Can have < 0, > 0, or 0 value in Henry

# Neumann Formulation of Mutual Inductance



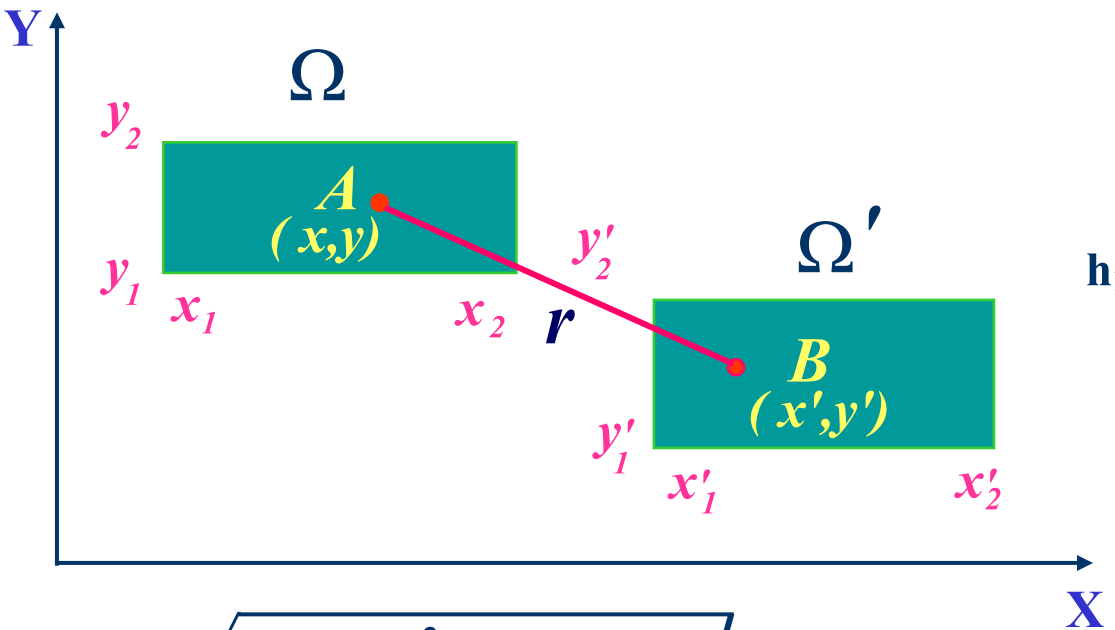

$$L_{i,j} = \int_{s'=s'_1}^{s'_2} \int_{s=s_1}^{s_2} \frac{\vec{u}\,\vec{v}}{r}\, ds\, ds'$$

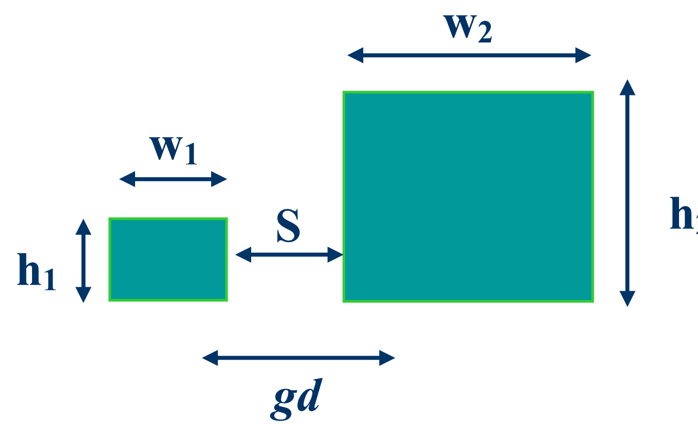
$\vec{u}$ → unit vector along *AB*

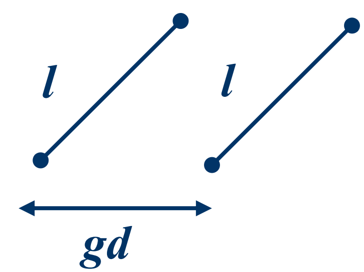
$\vec{v}$ → unit vector along *CD*

$$r = \sqrt{(x-x')^2 + (y-y')^2 + (z-z')^2}$$

# Geometric Distance Between Objects



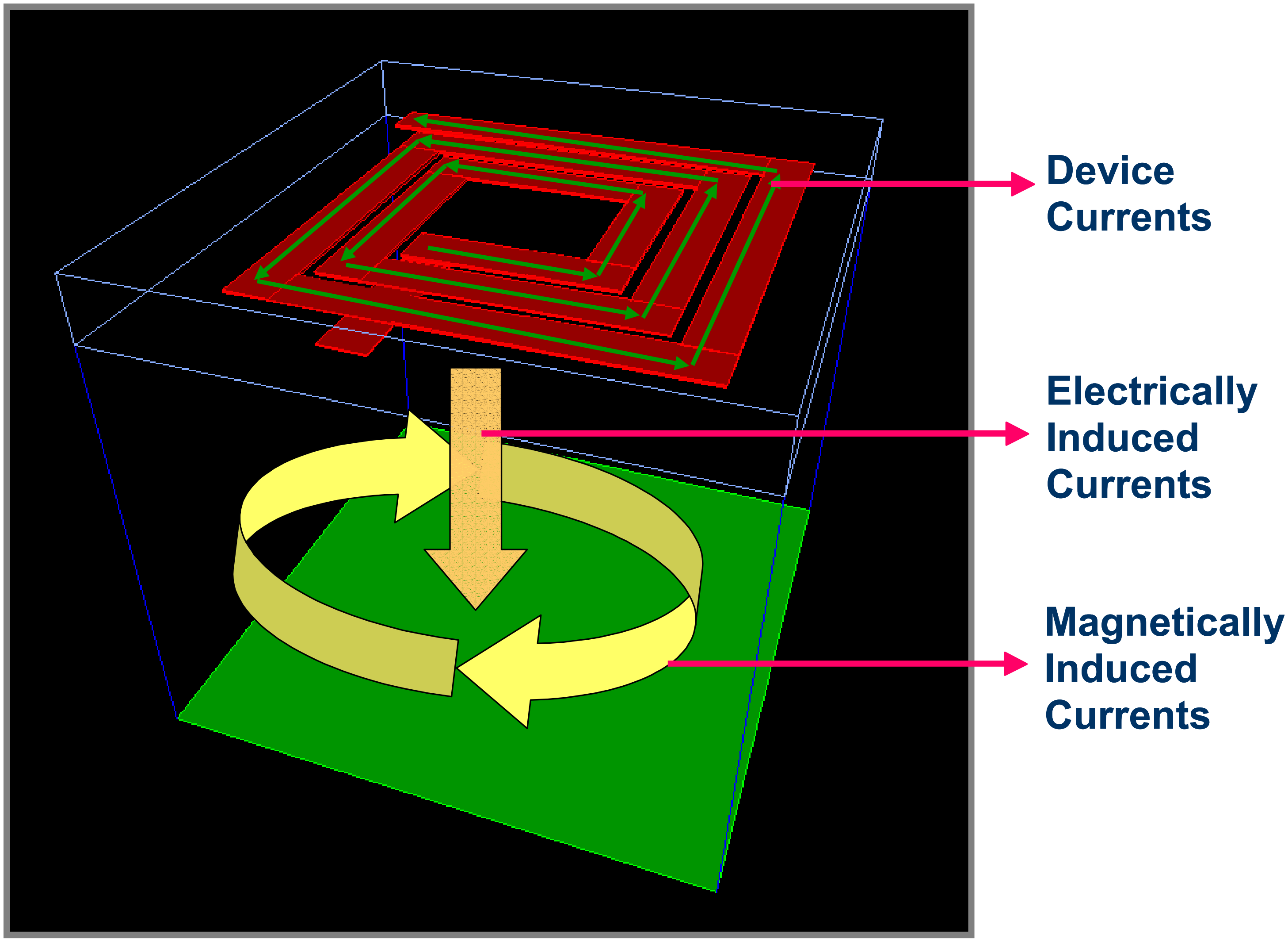




$$r = \sqrt{(x - x')^2 + (y - y')^2}$$

$$gd = \int_{\Omega'}\int_{\Omega} \ln(r)\, d\Omega\, d\Omega'$$

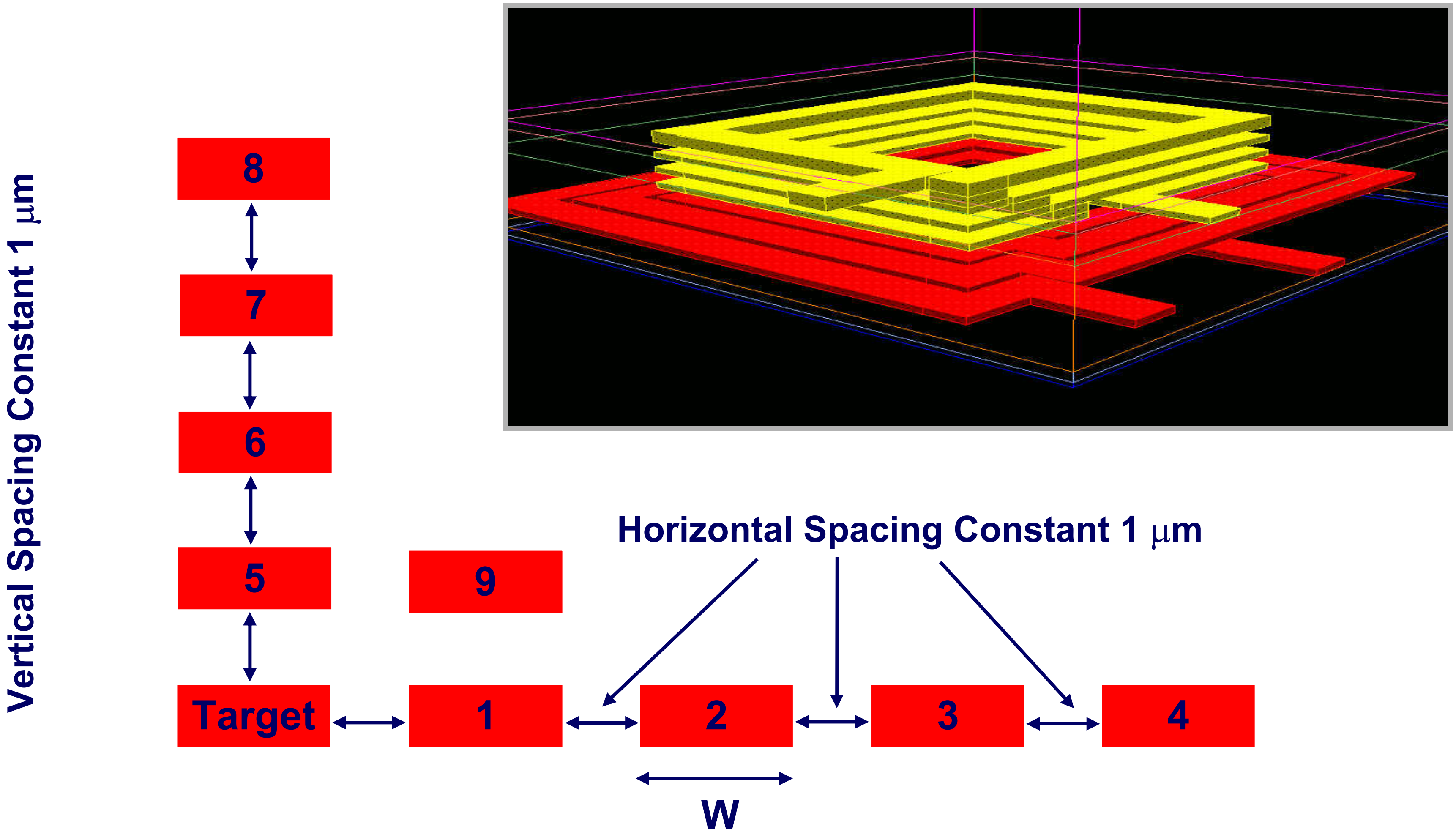
$$gd = \int_{y'=y_1'}^{y_2'} \int_{y=y_1}^{y_2} \int_{x'=x_1'}^{x_2'} \int_{x=x_1}^{x_2} \ln\sqrt{(x - x')^2 + (y - y')^2}\; dx\, dx'\, dy\, dy'$$

# A Difficult Extraction Problem



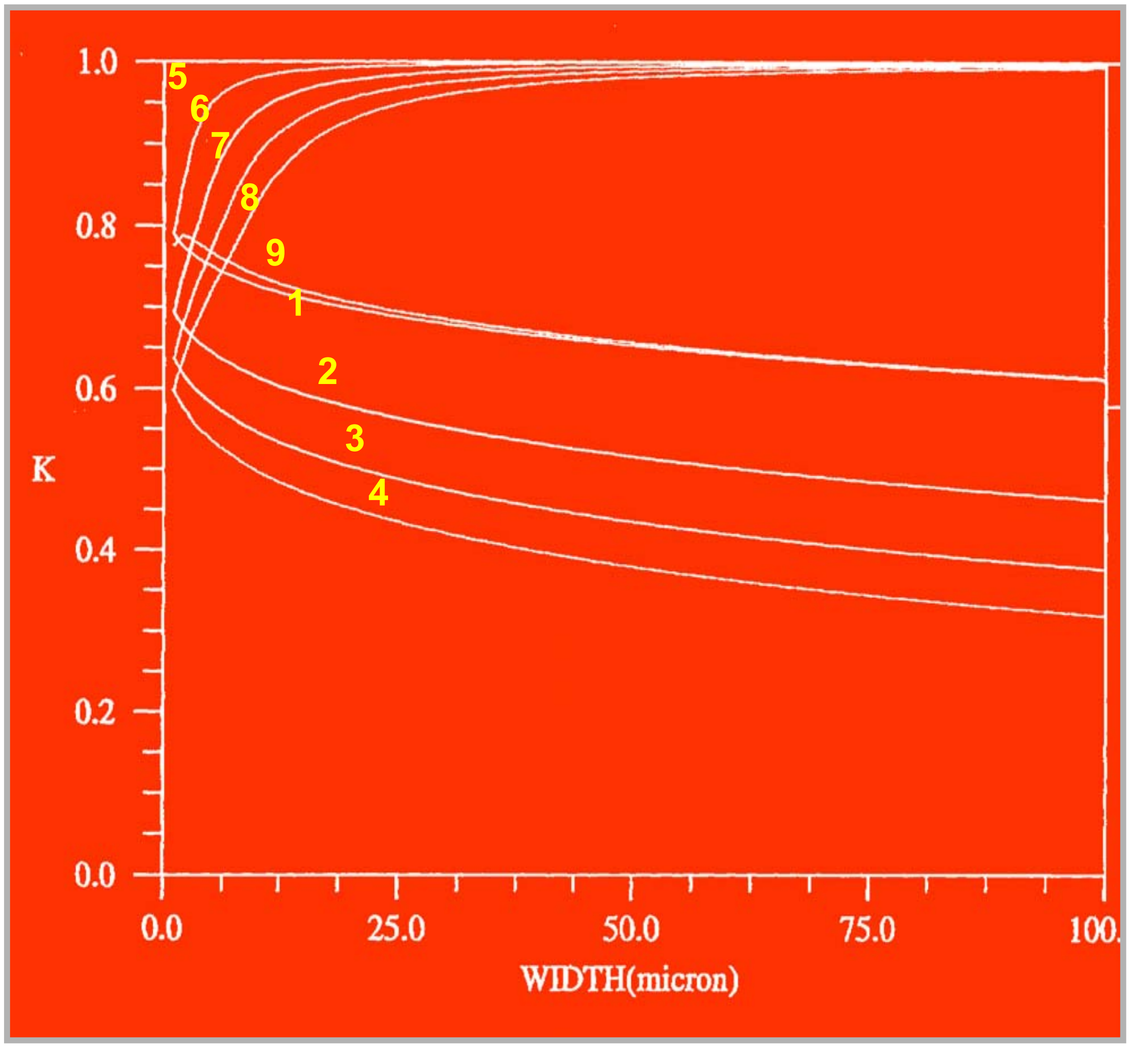

**Self capacitance, Capacitance to Substrate, High Frequency Skin Effect etc...**

# Inductive Coupling: Spirals and Helices

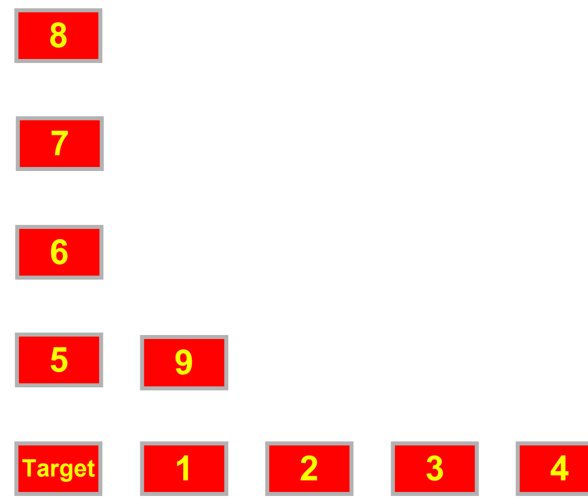



Target and Nine Conductors are all the Same Width

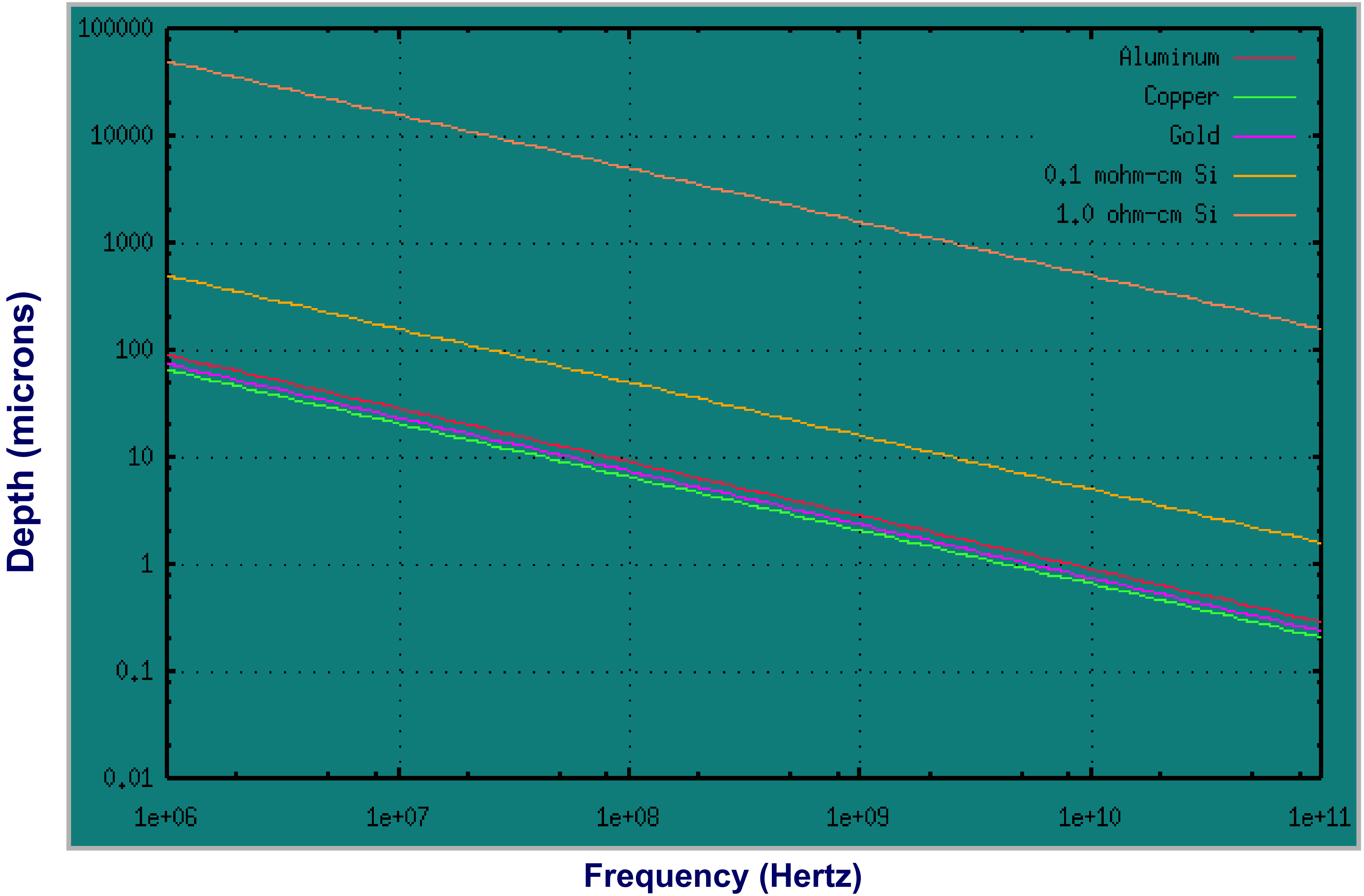
# Mutual Inductive Coupling as a Function of Width



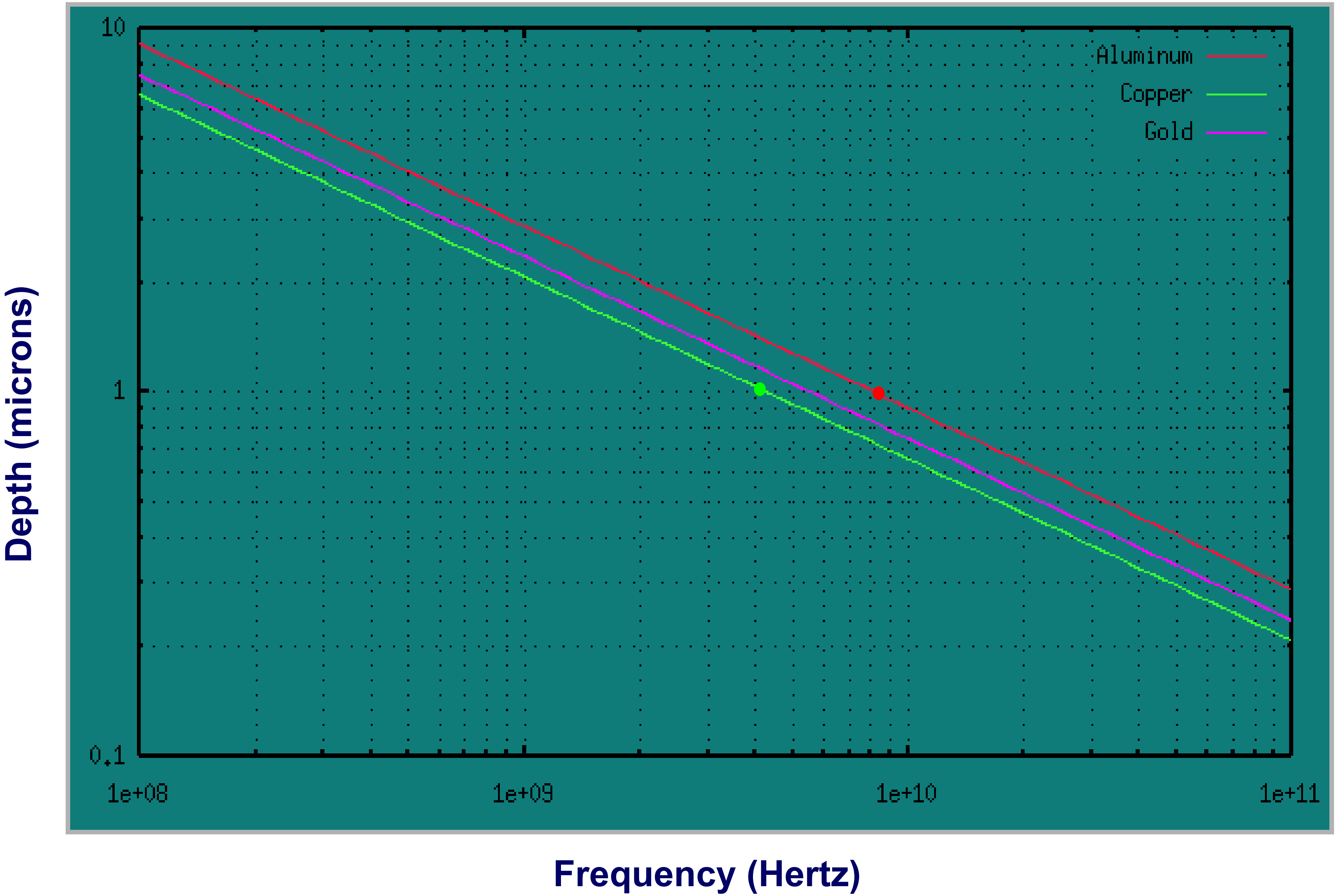

$$K_{nm} = \frac{L_{nm}}{\sqrt{L_{nn} \cdot L_{mm}}}$$



# Skin Depth of Some Materials



# Skin Depth of Commonly Used Metals



# Skin Depth Area of a Conductor

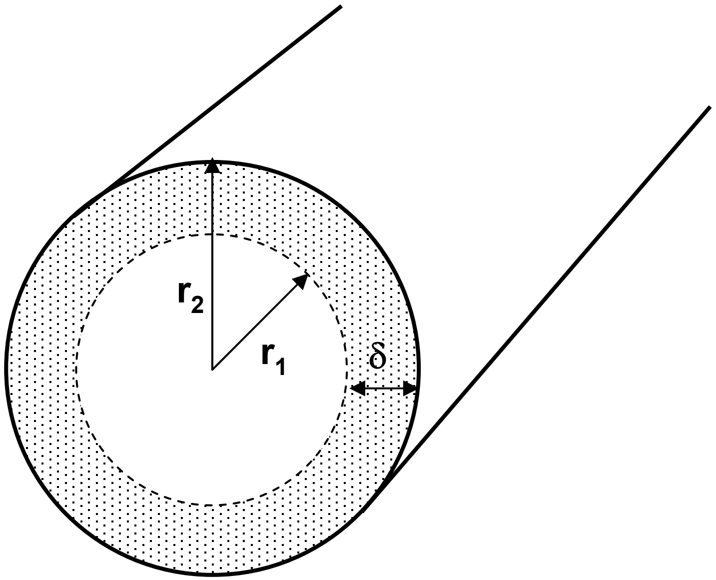
$A_1 = \pi r_1^2$
$A_2 = \pi r_2^2$
Skin Depth Area = $A_2 - A_1 = \pi(r_2^2 - r_1^2)$

$A_1 = w_1 h_1$
$A_2 = w_2 h_2$
Skin Depth Area = $A_2 - A_1 = w_2 h_2 - w_1 h_1$

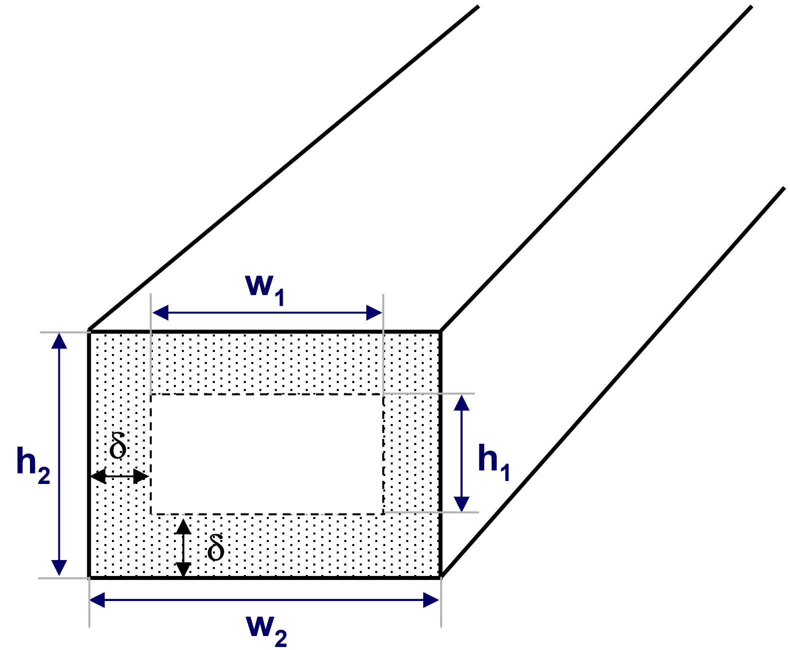
$\delta = r_2 - r_1$

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}}$$

$2\delta = w_2 - w_1 = r_2 - r_1$




RF current flow in shaded region




RF current flow in shaded region

# Radiative Losses

- **On chip inductors make very poor antennas**
  - No need to worry about radiation loss in most cases
  - However, should be careful near quarter wavelength

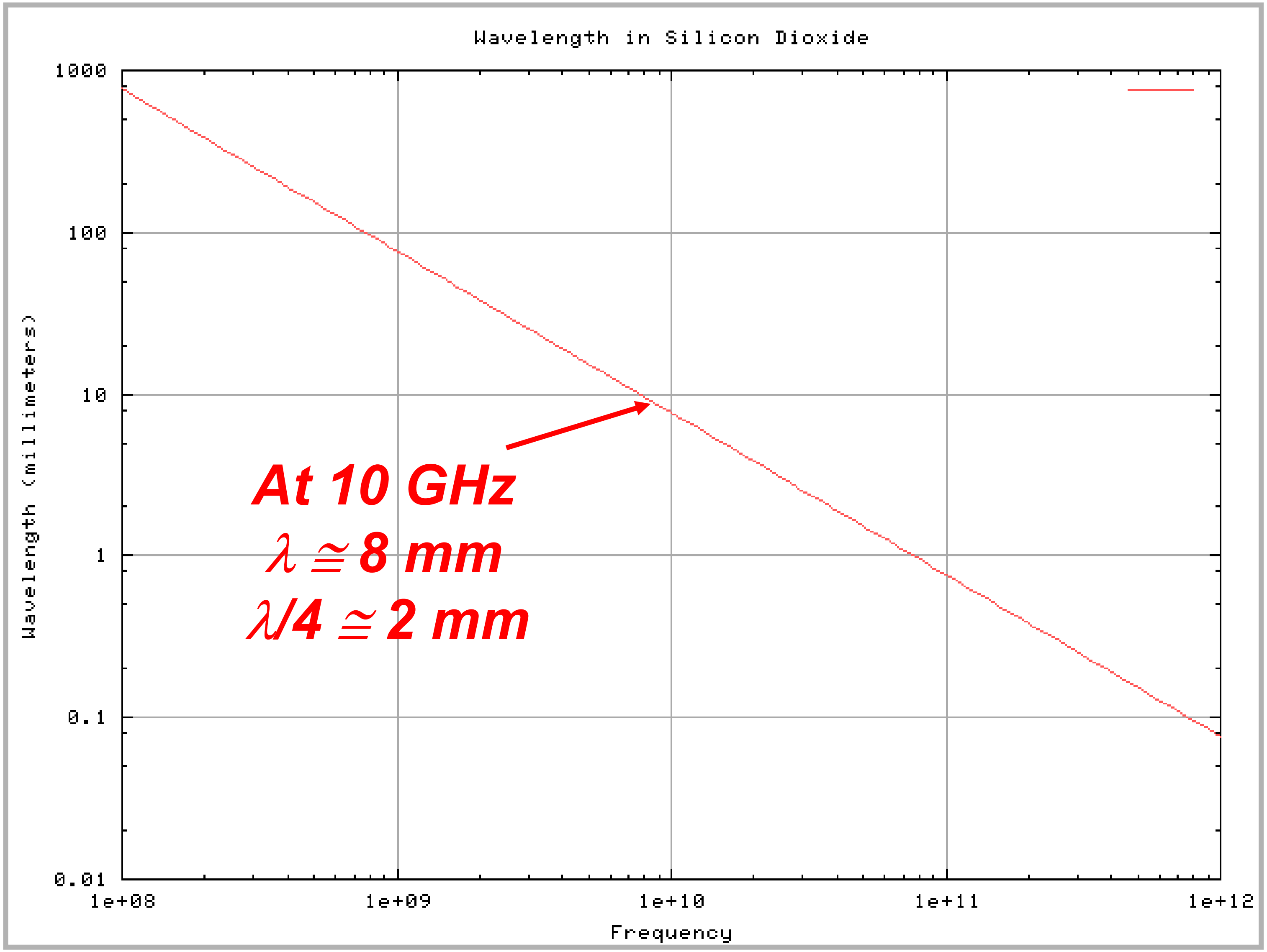
$$V_p = \text{Propagation Velocity} = \text{Phase Velocity}$$

$$V_p = 1/\sqrt{\mu\varepsilon} = 1/\sqrt{LC}$$

$$V_p = f\lambda$$

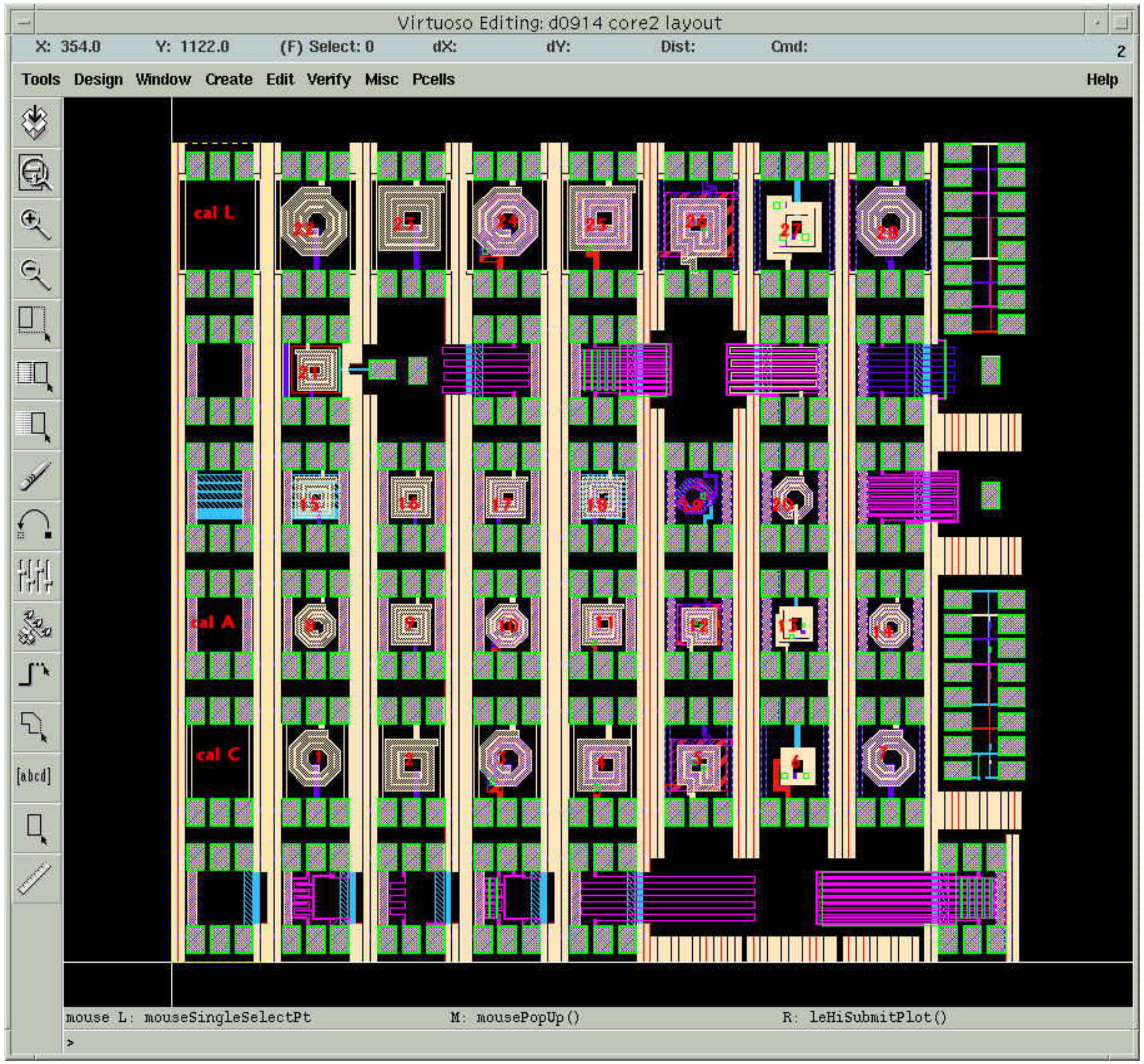
$$\lambda = (1/\sqrt{\mu\varepsilon}) / f$$

# Wavelength vs. Frequency in $SiO_2$

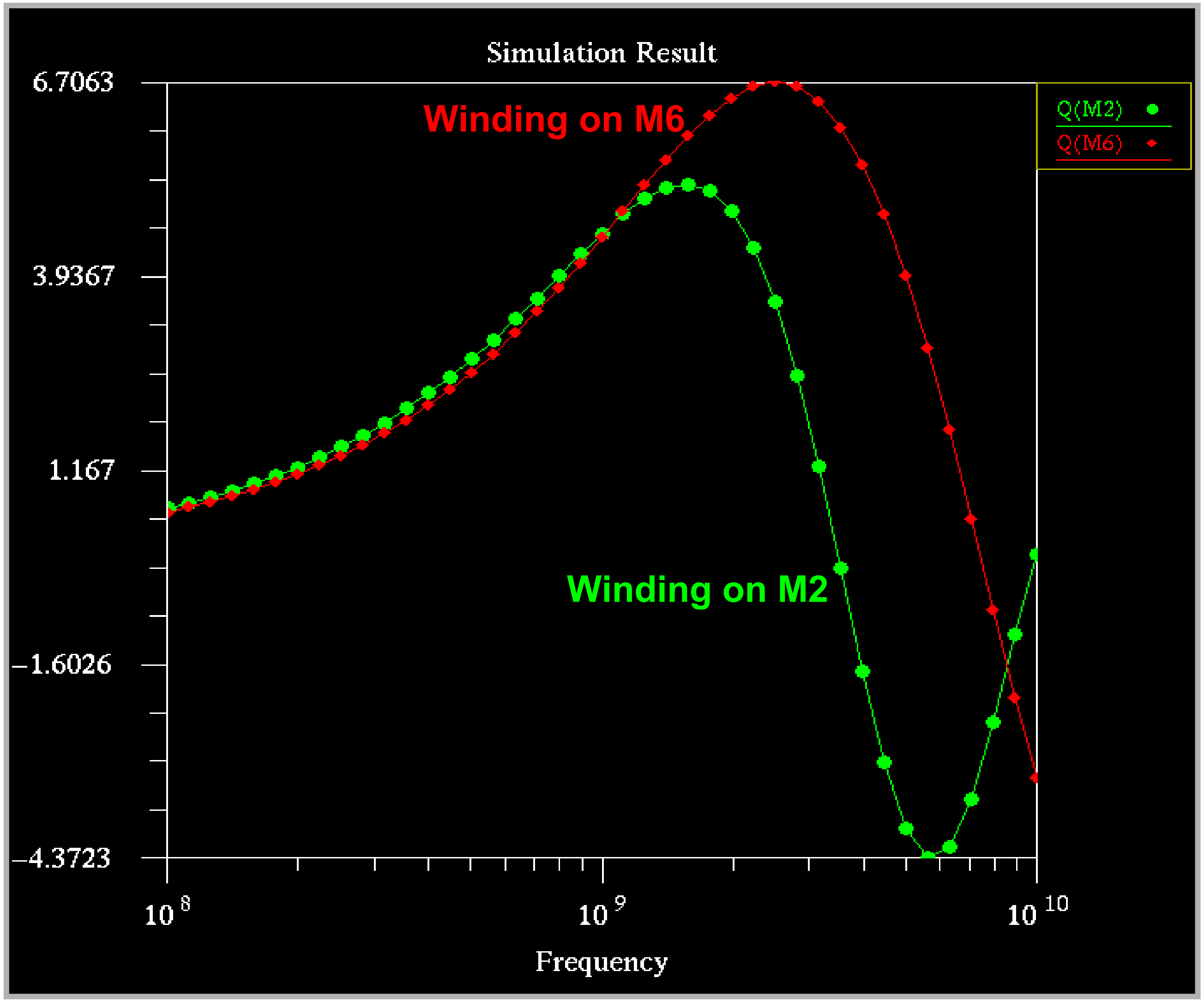


# OEA's Fabricated Test Chip

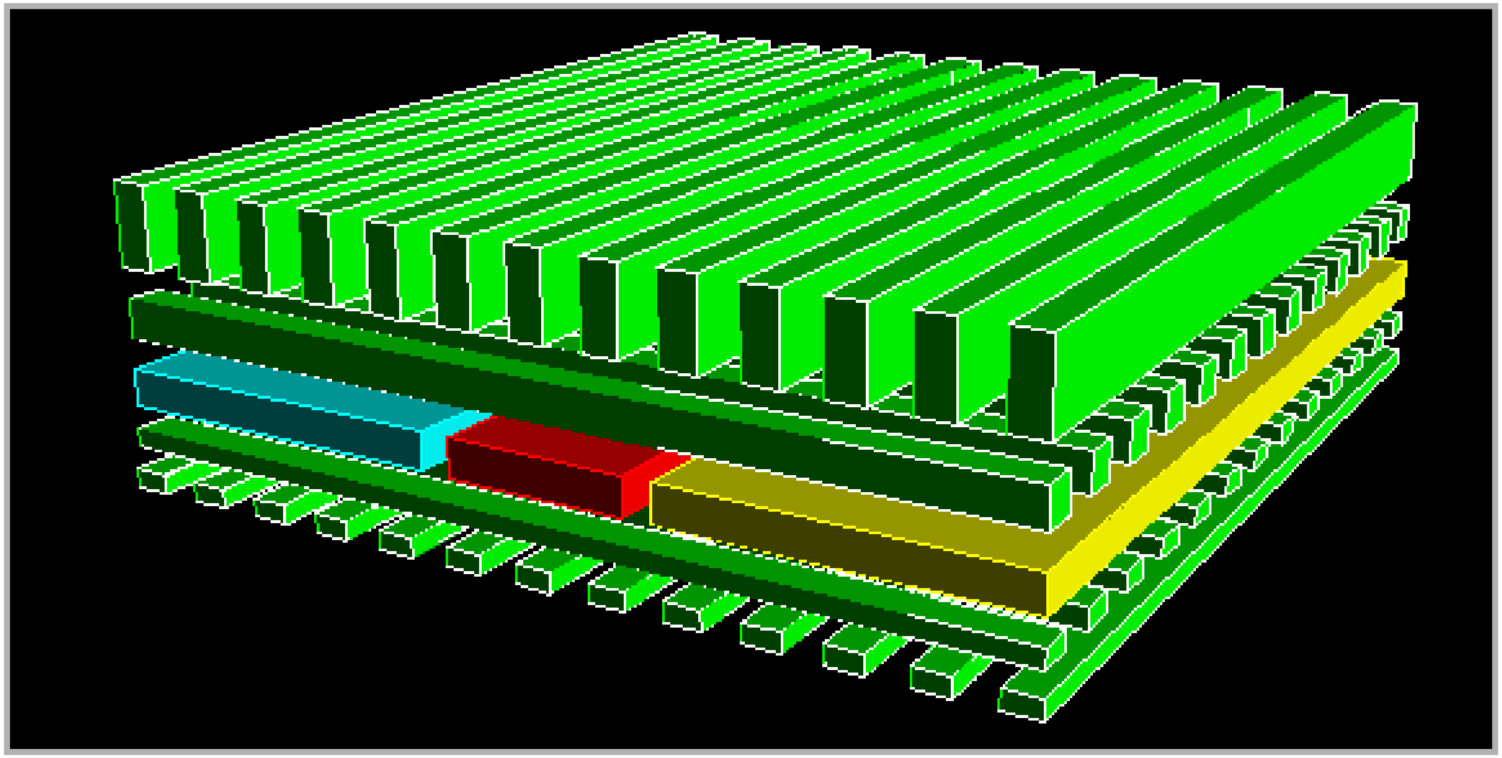
## TSMC 0.25 μm



# Q vs. Frequency for Two Inductors
## (All metal layers have same thickness and ρ)

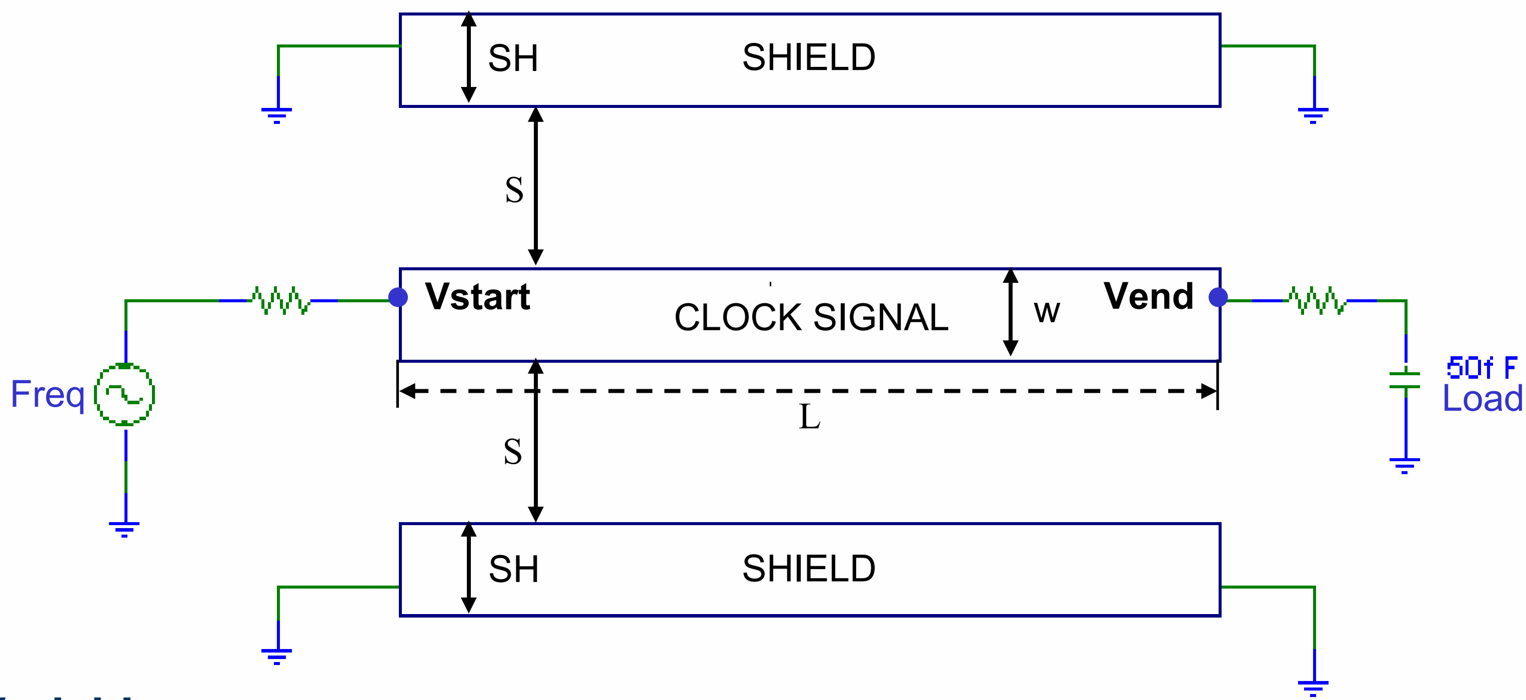


# AC Analysis Cross Section
# Automatic Geometry Generation



- M6 Clock in Red
- VSS/VDD Shields in Blue and Gold
- Proximity Metal on M4, M5, M7 and M8 in Green

# Schematic of AC Analysis on Clock and Shields

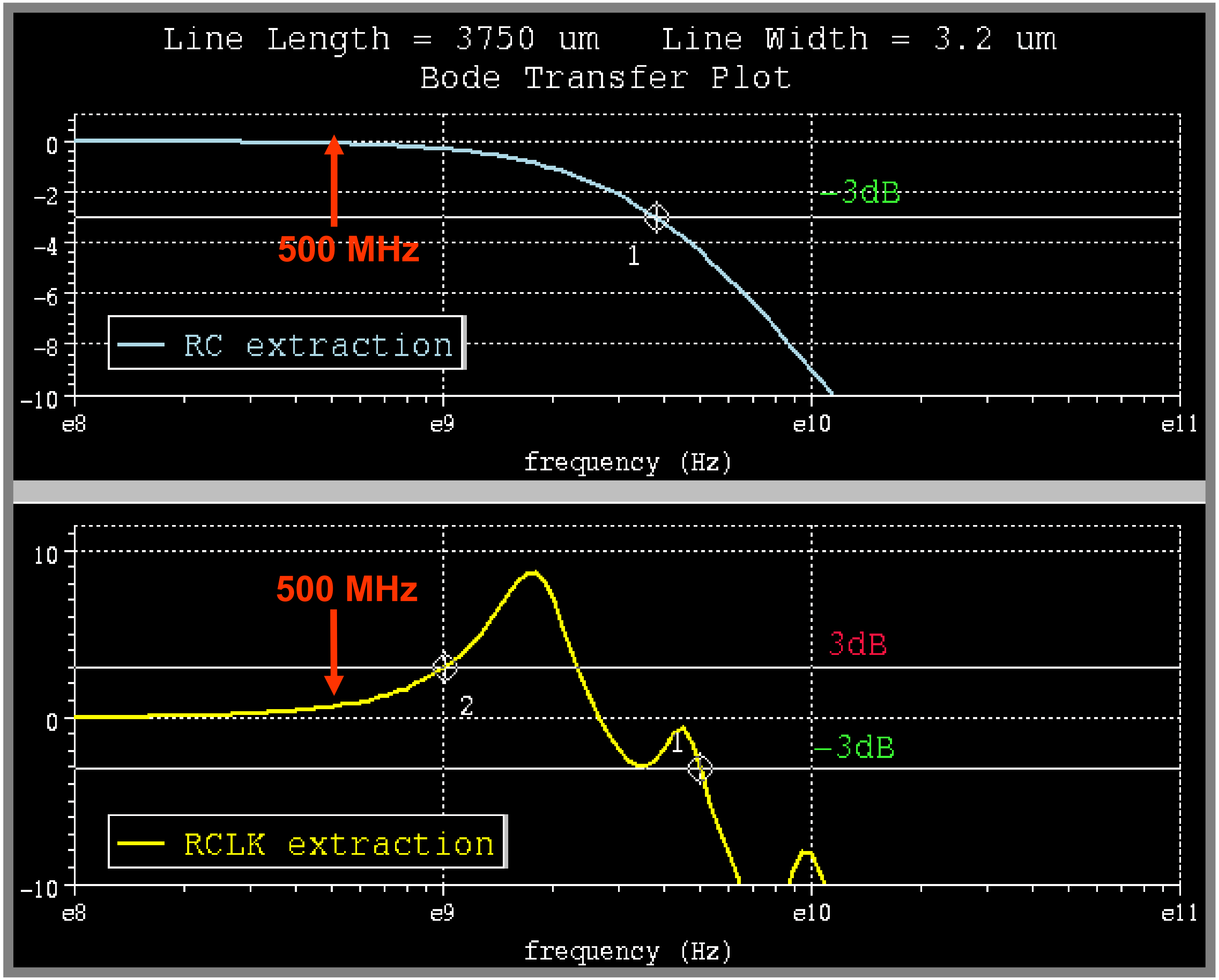



**Variables**:

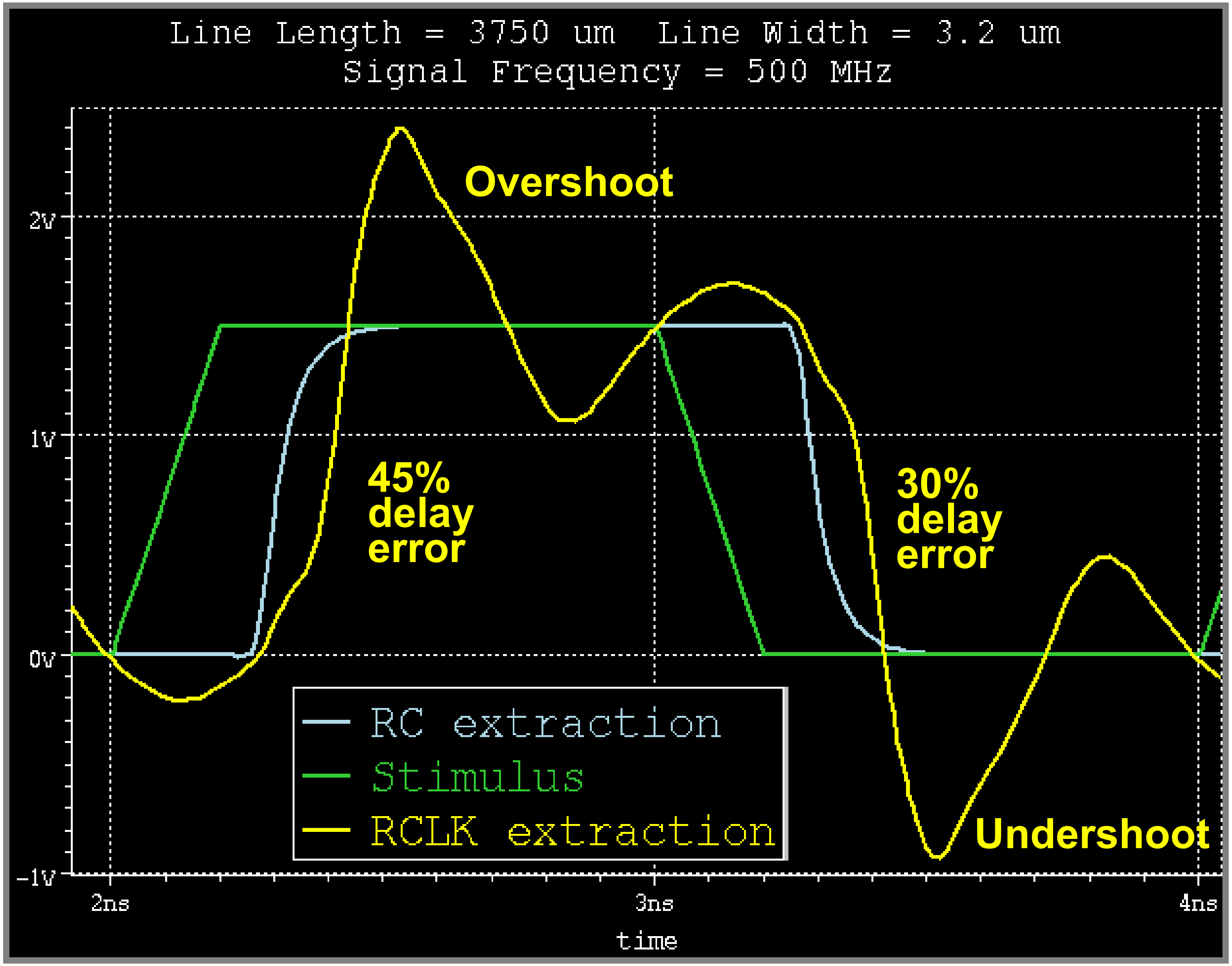
Length: 1 to 15 mm
Width: 1 to 15 µm
Spacing: 0.8 to 3.0 µm

Shield Width: 1 to 20 µm
Metal Layer for Clock: M4, M5, M6
RC & RCLK Models, Capacitive Loads

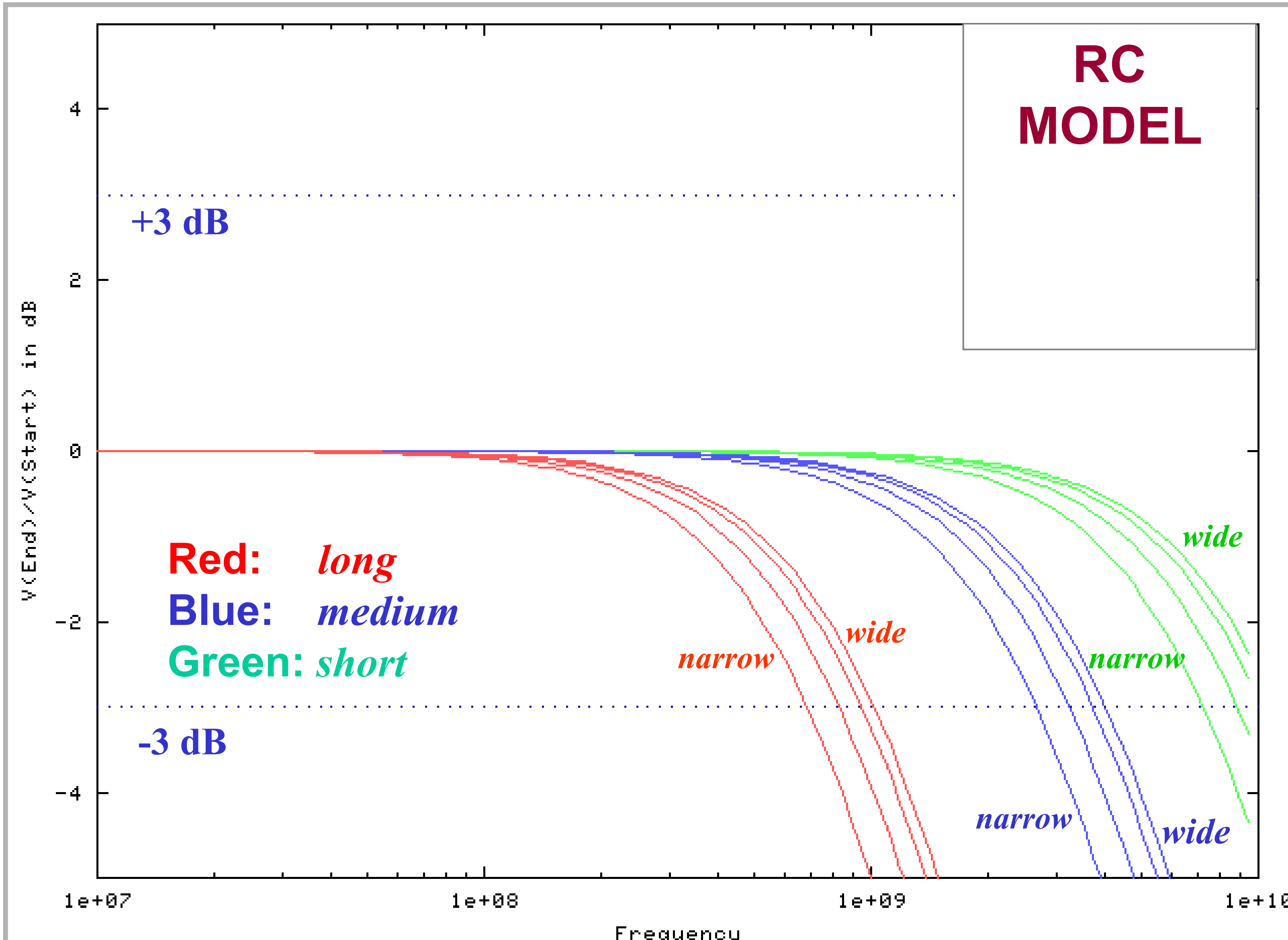
# Frequency Behavior of 3.2μ by 3.75 mm Line



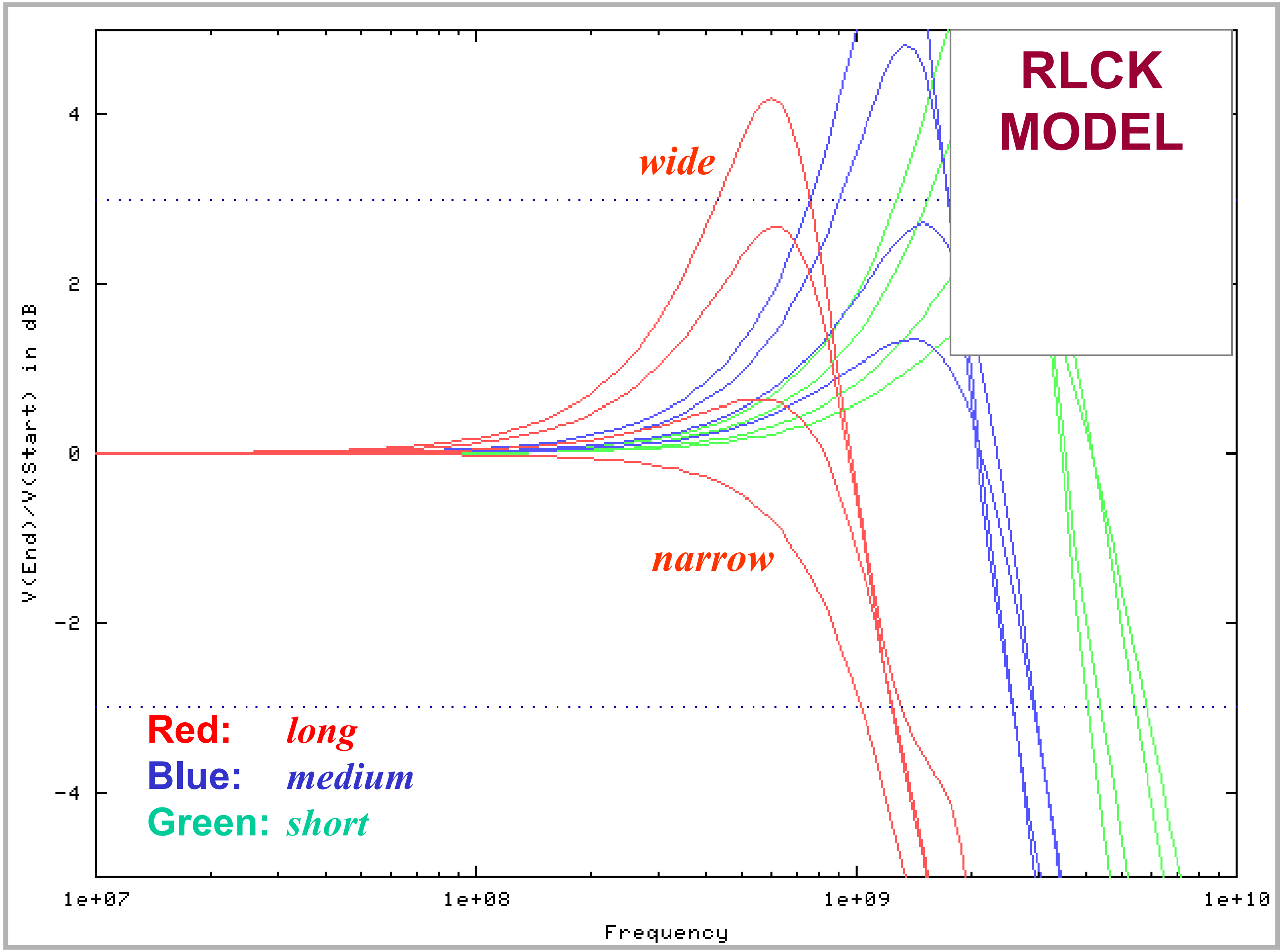
# Transient Behavior of 3.2μ by 3.75 mm Line



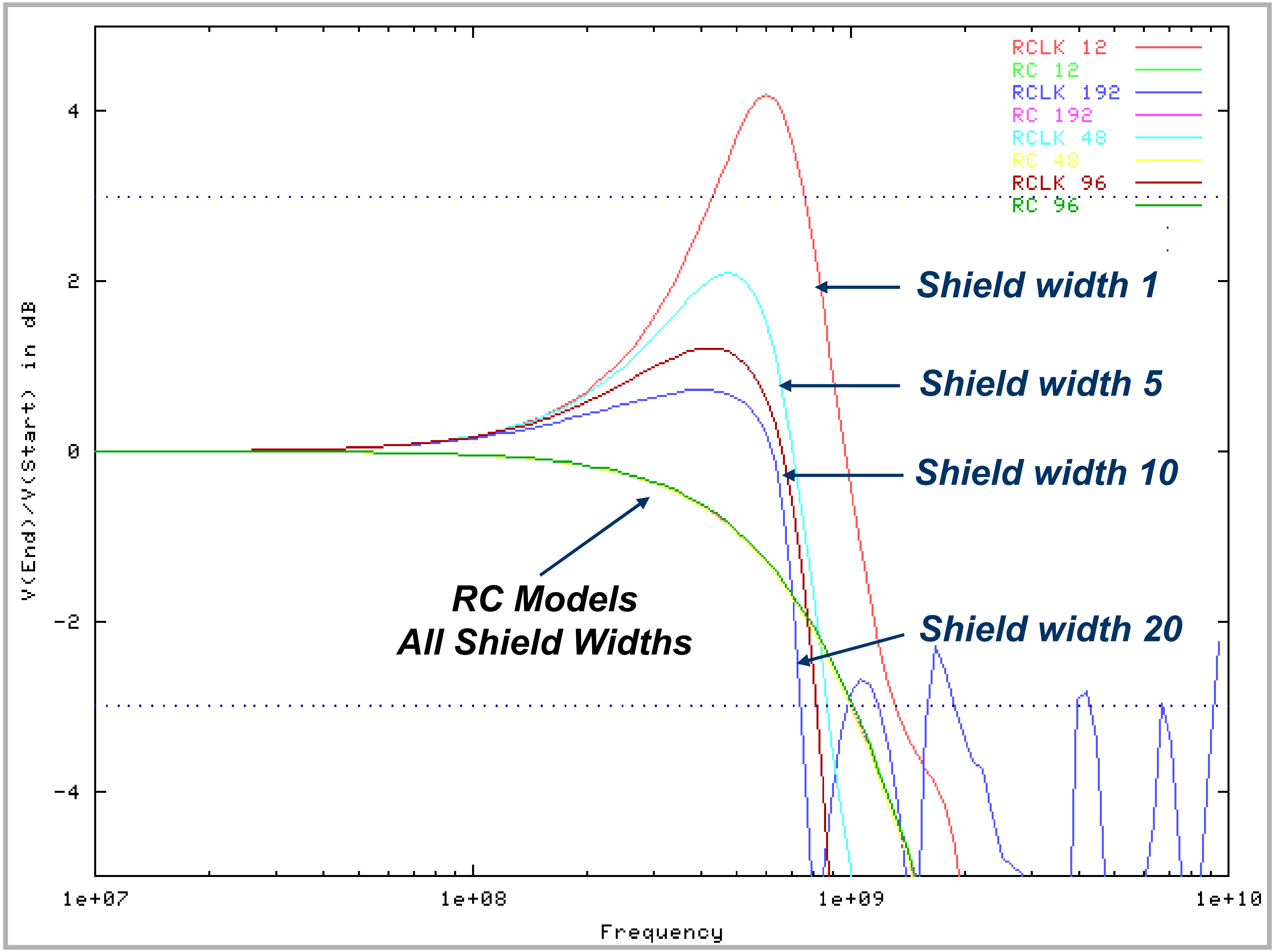
# Bode Plot: Resistance & Capacitance Model



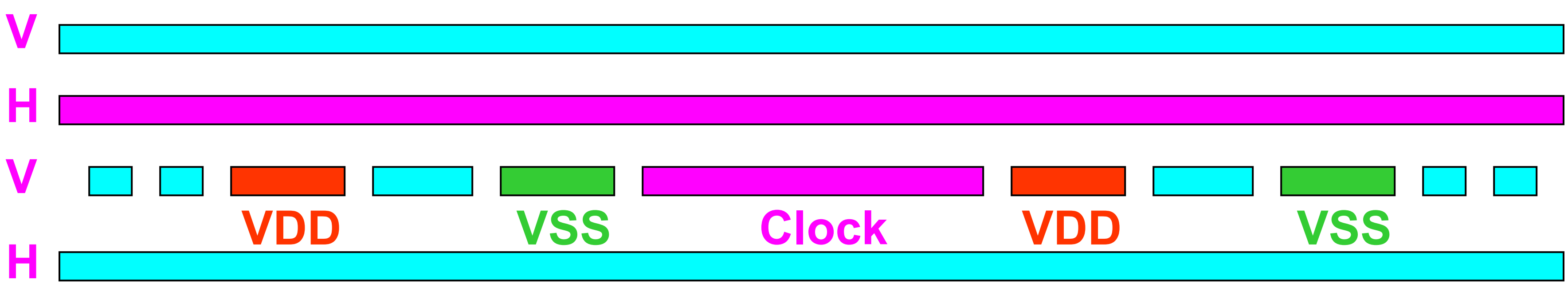
# Resistance, Capacitance, Inductance and Mutual Inductance Model



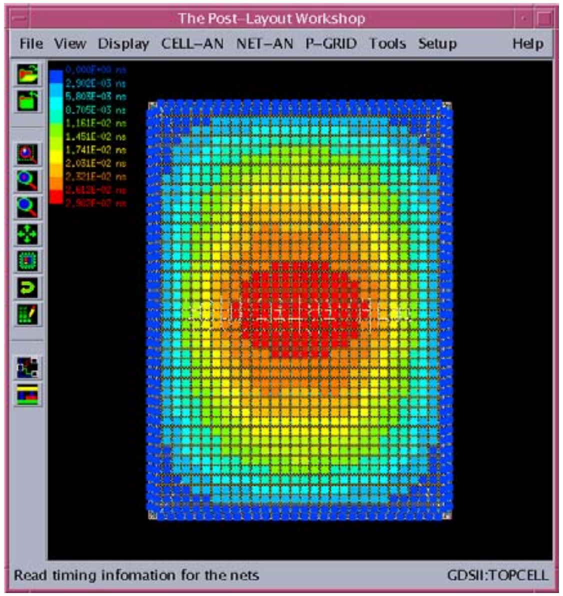
# Varying Shield Widths from 1μ to 20μ (Constant Width and Length)



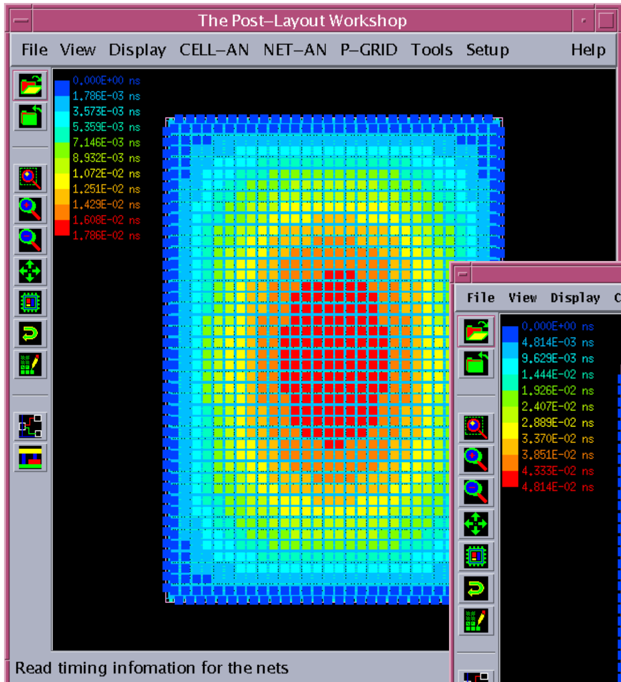
# Clock Grid Routing with Shield Grid as the Return Path



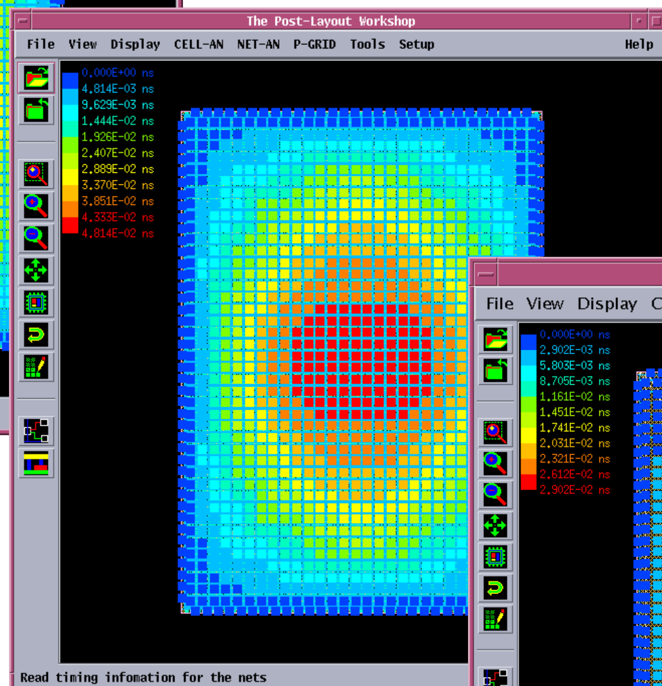

- Drivers on all four sides
- Clock Grid on Multiple Metal Layers
- All same net crossings tied with vias



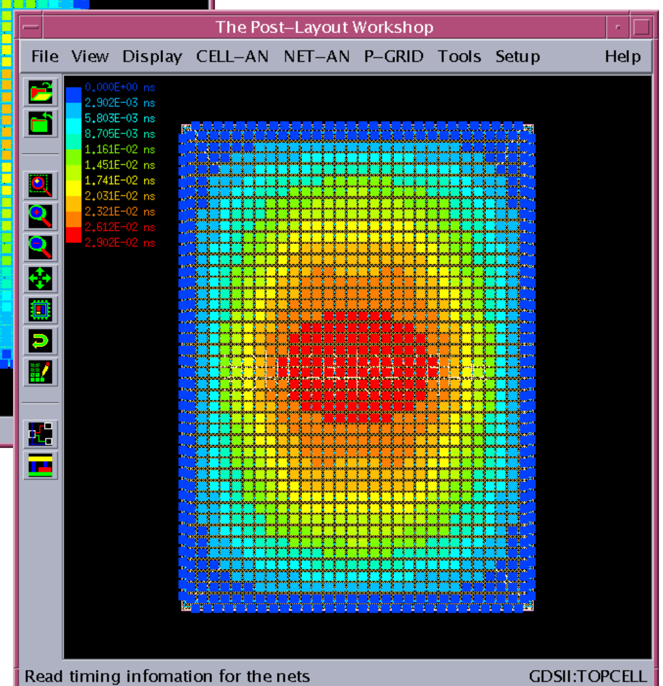
# Clock Skew Comparison @ 2GHz




**RC skew**
**17.86 ps**

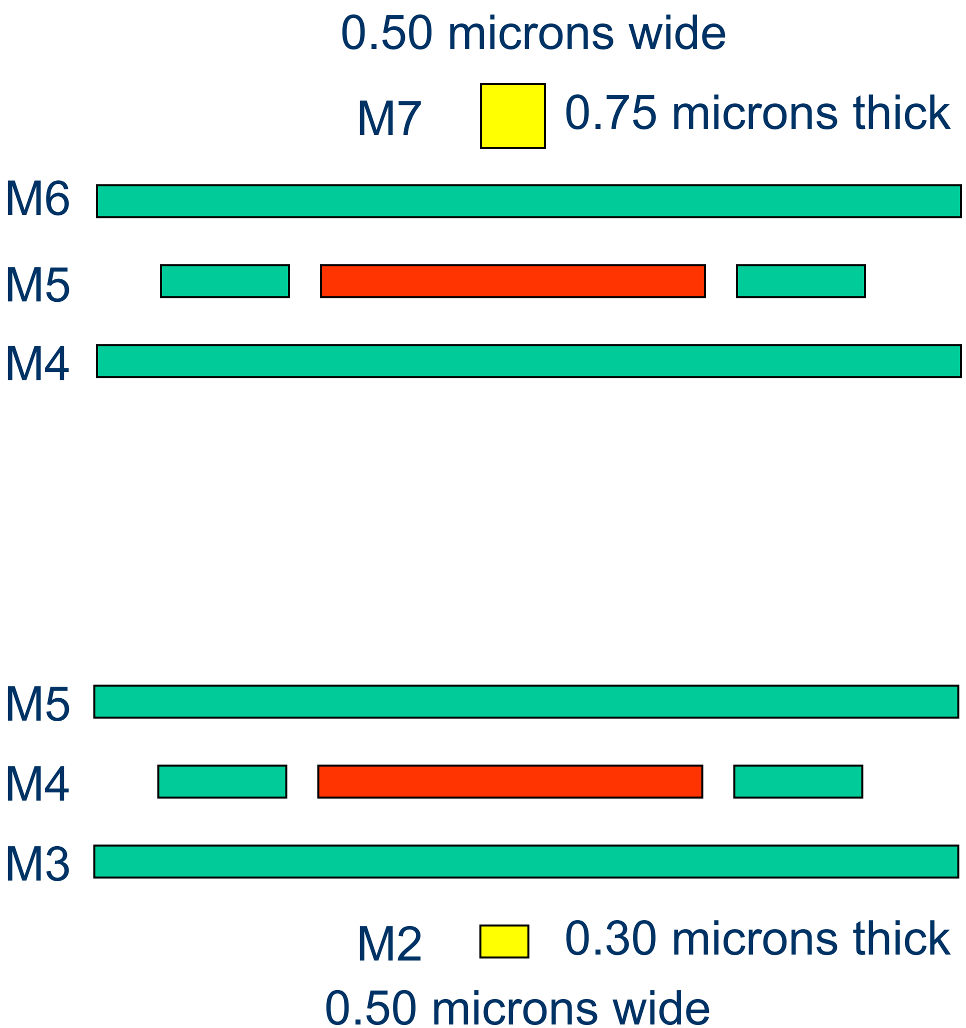


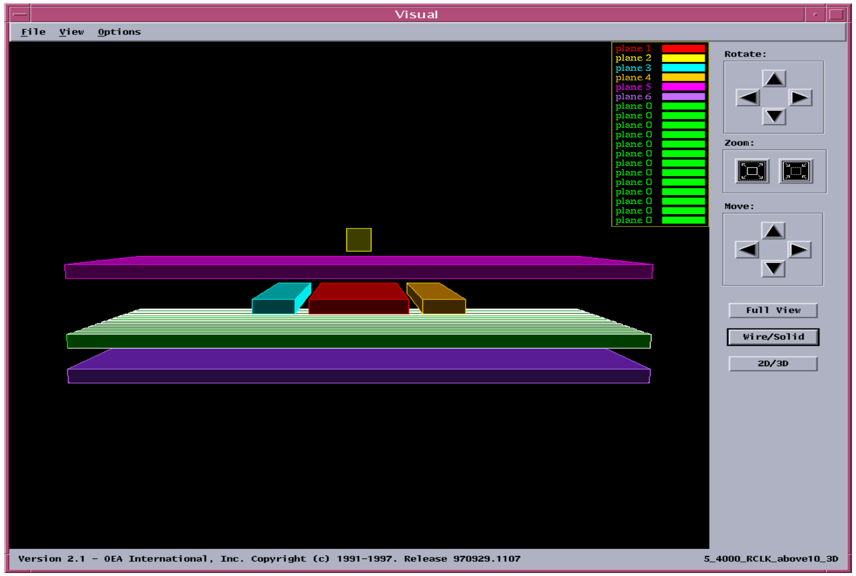

**RCL skew**
**48.14 ps**

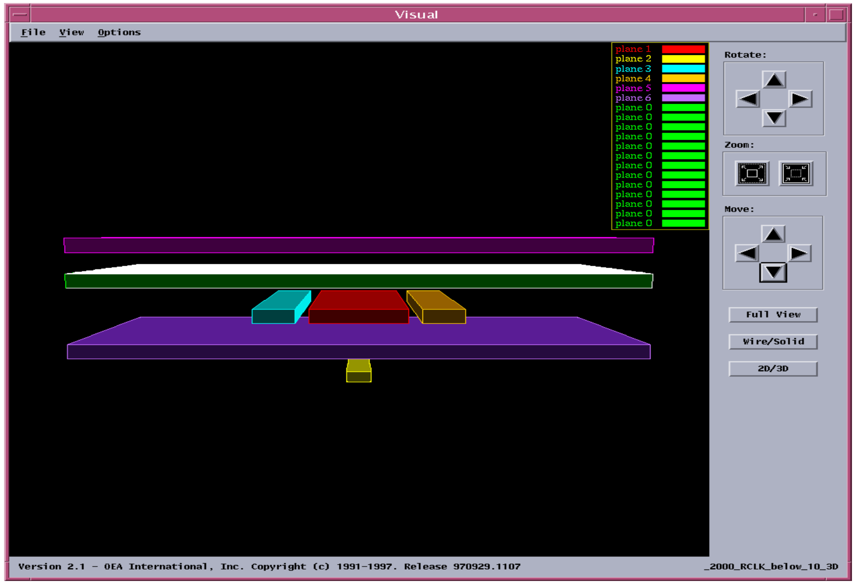



**RCLK skew**
**29.02 ps**

# Crosstalk From Aggressor to Victim Lines Through Non-Ideal Metal Shields

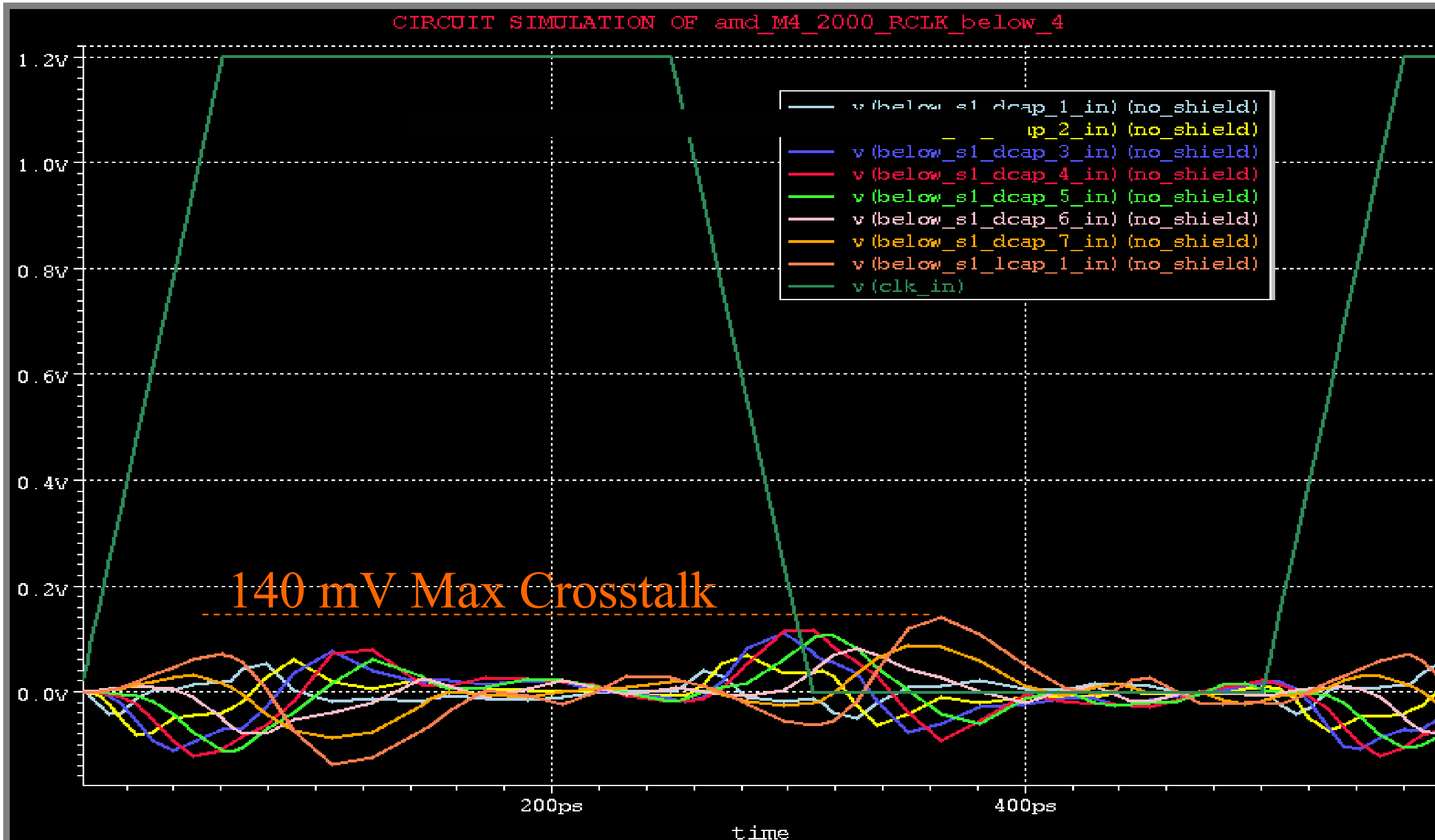


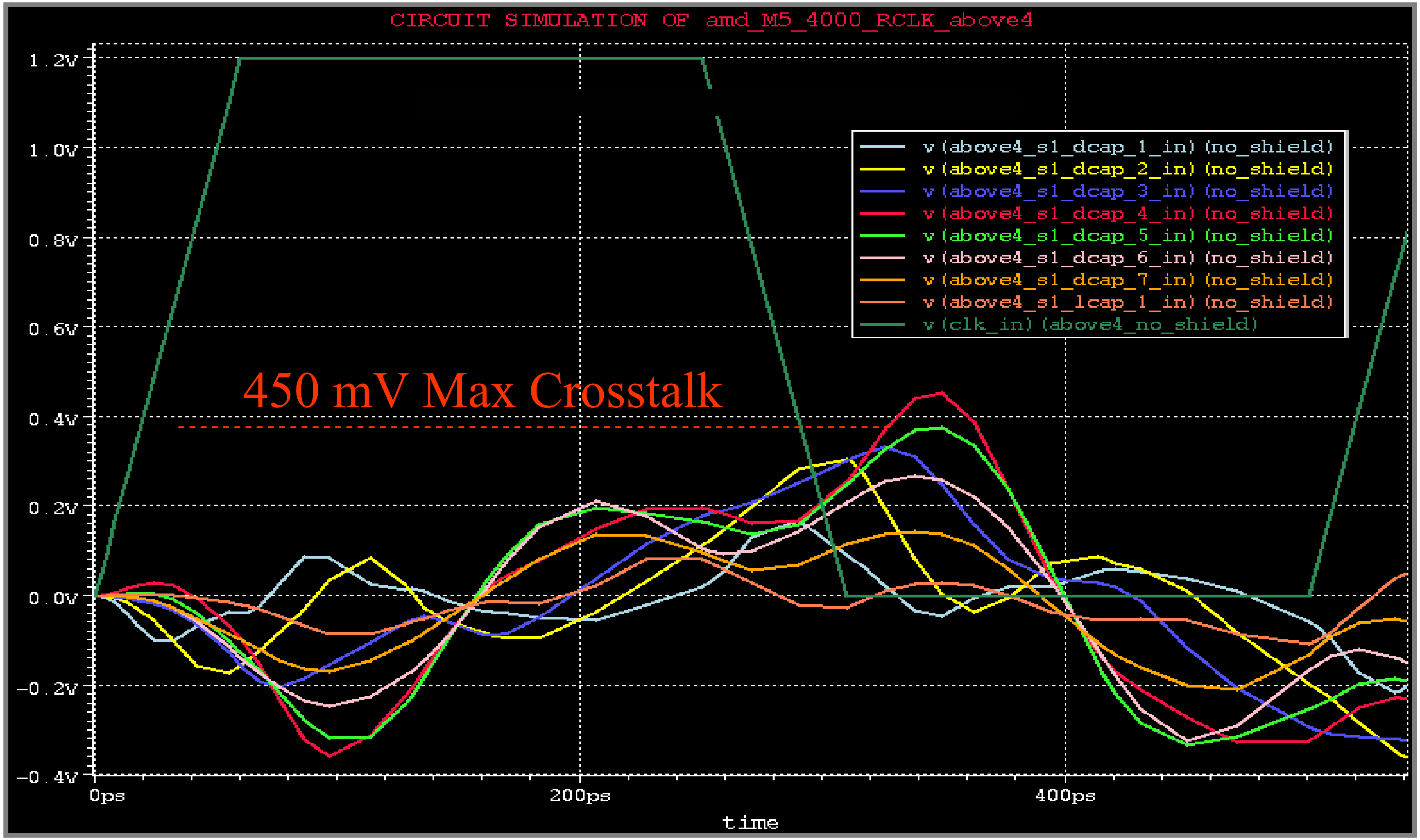



isQED

# M4 Aggressor Crosstalk at Various Points on M2 Victim Line



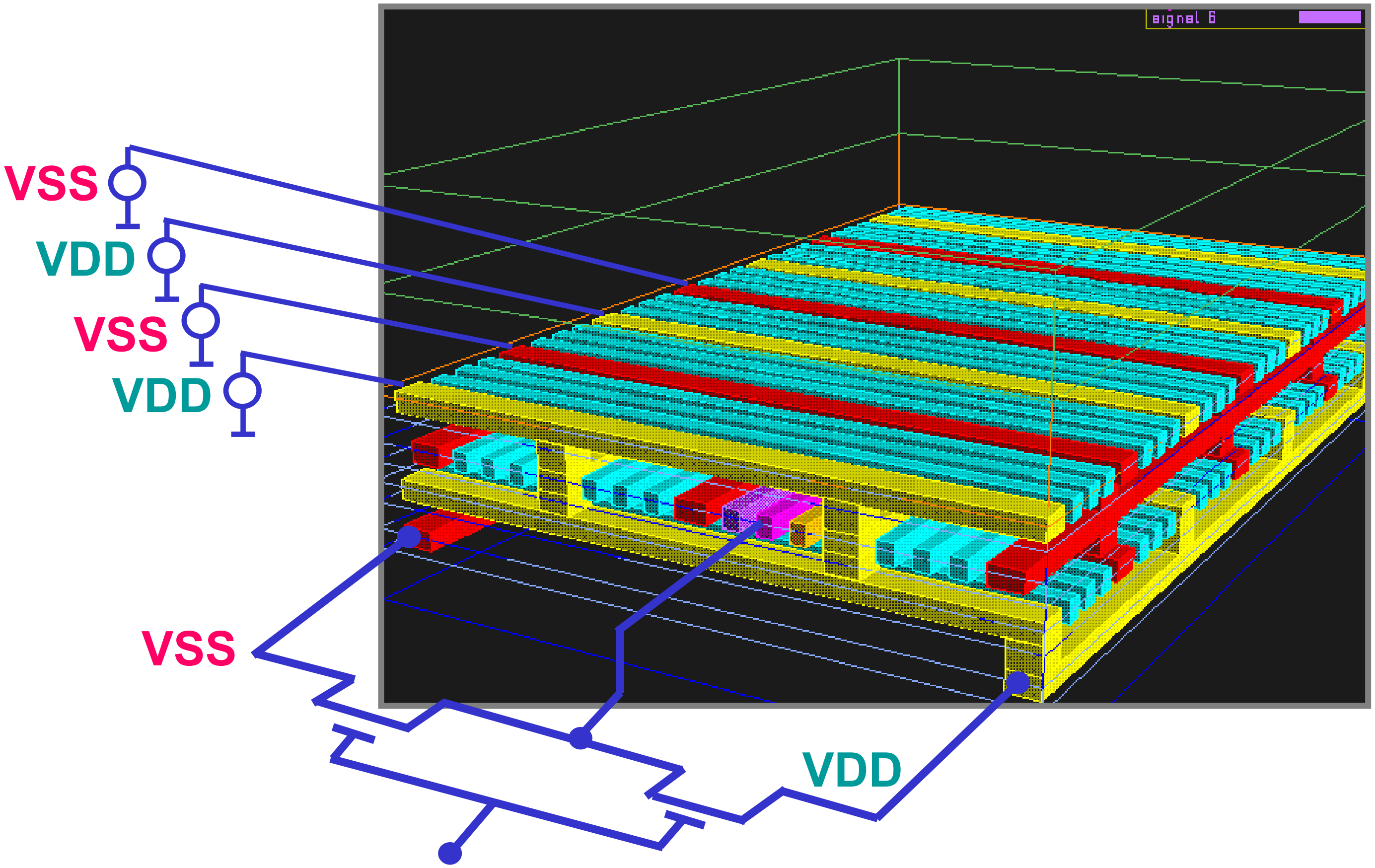
# M5 Aggressor Crosstalk at Various Points on M7 Victim Line



# Techniques for Reducing Crosstalk

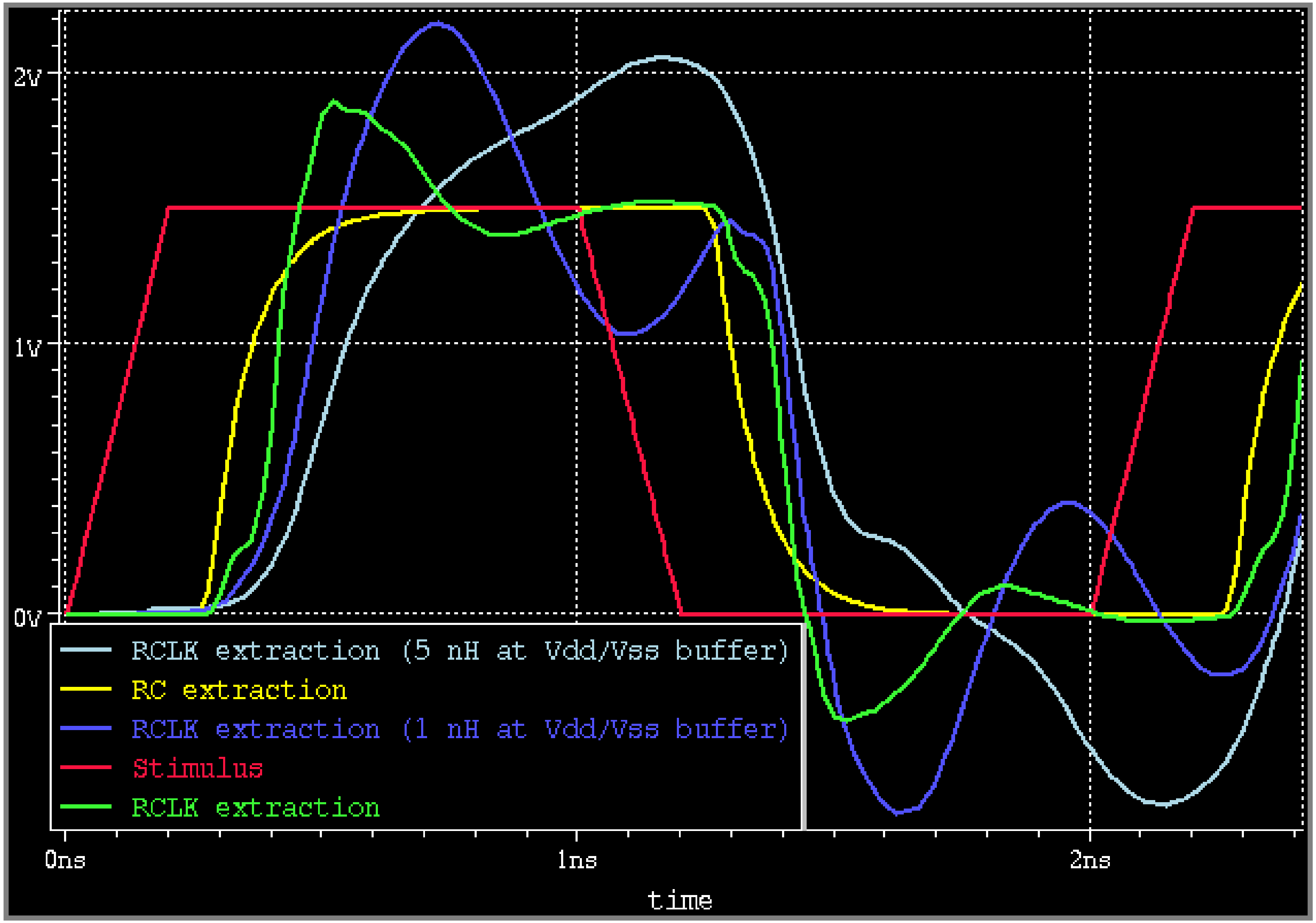
- **Increasing signal line width**
  - Increases signal-to-ground capacitance compared to signal-to-signal capacitance
- **Increase spacing between signals**
  - Decreases capacitive coupling
  - Can increase inductive coupling (larger loops)
- **Shielding signals with power and ground**
  - Provides known low-impedance return paths
- **Buffer insertion**
  - Decrease line lengths, stagger buffers
- **Differential signal lines**
  - Can be very effective for high-speed signals

# Ideal versus Non-Ideal Power and Ground Nets

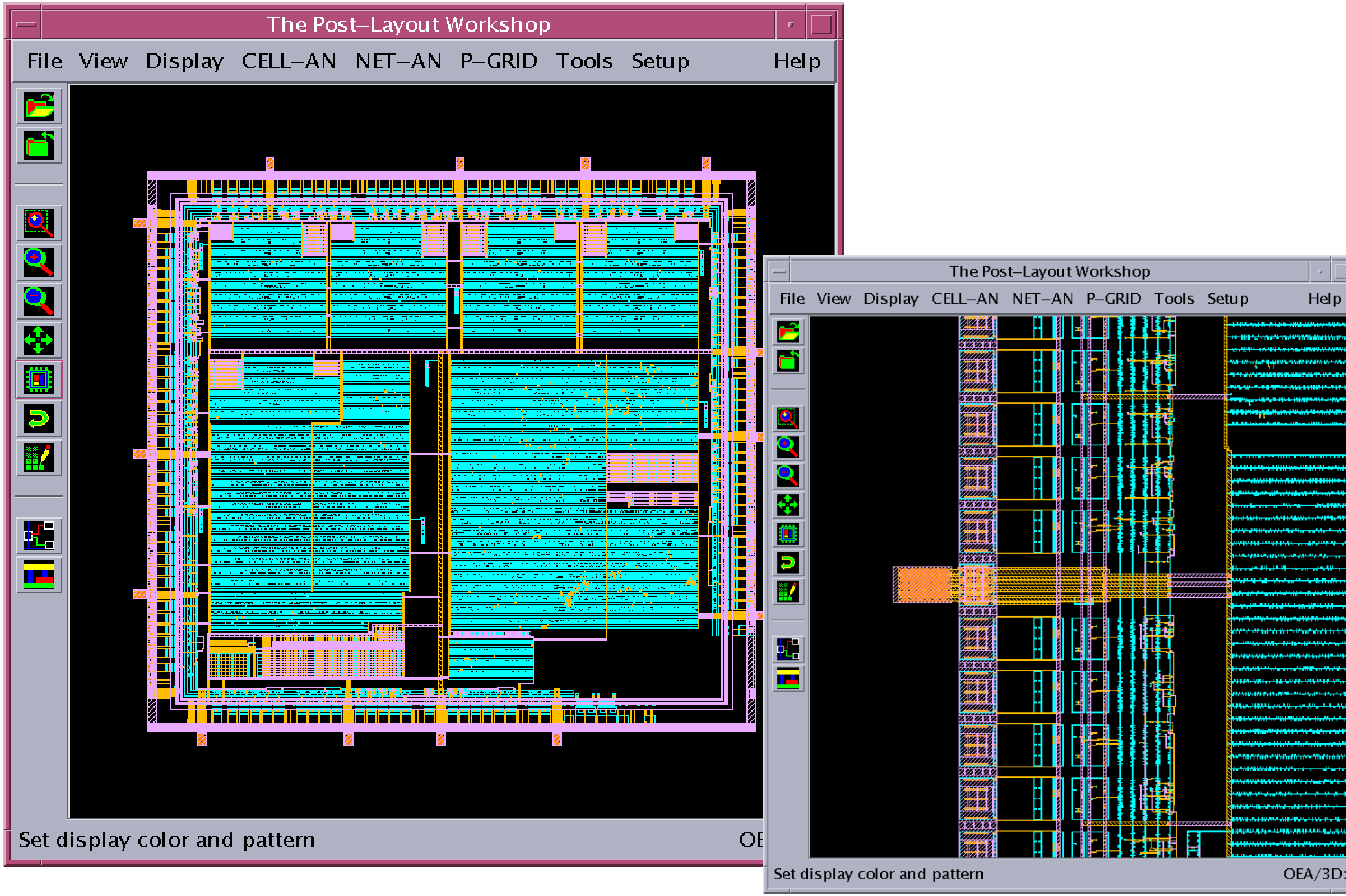



**VDD and VSS couple to the signal and have significant inductance and capacitance**

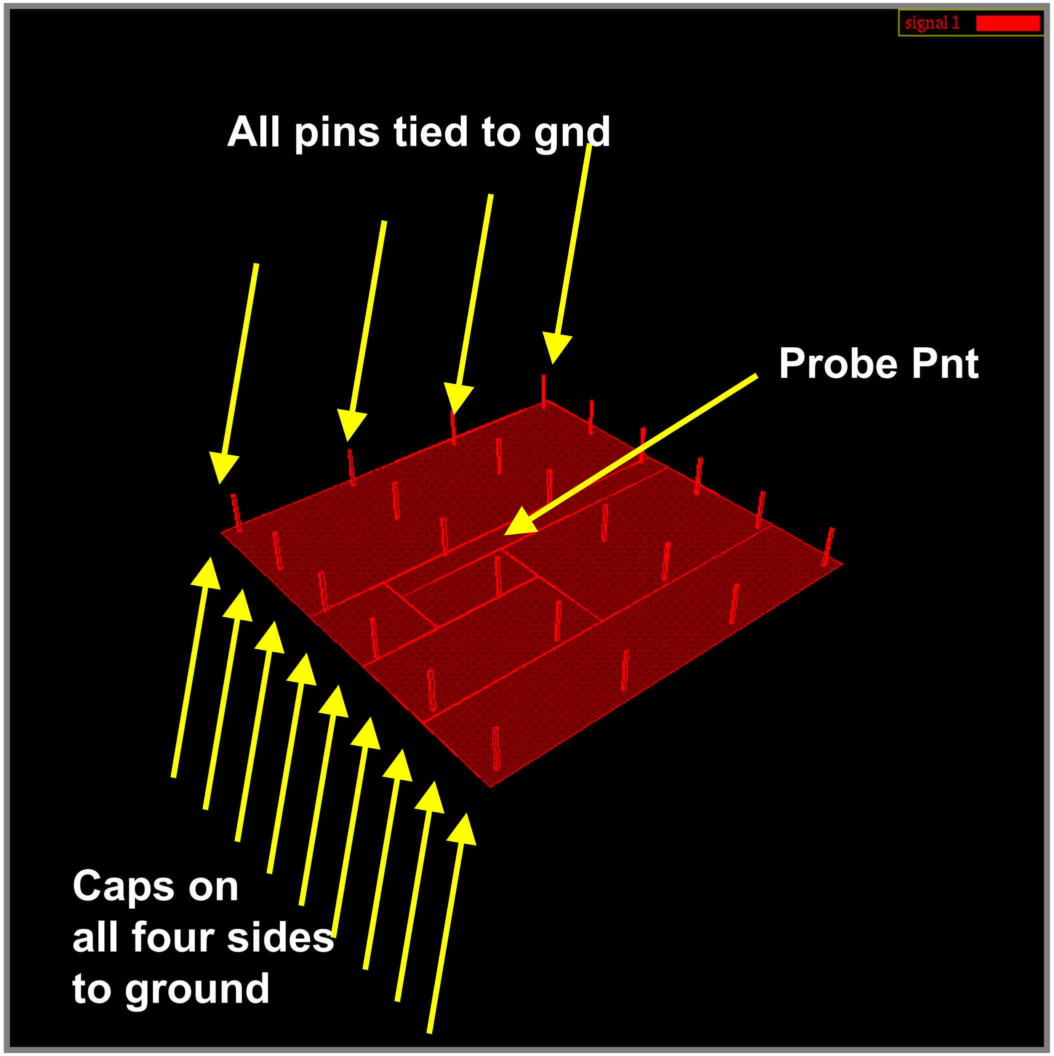
# Effect of VDD/VSS Impedance



# Effective Inductance to any Point on the VDD/VSS grids



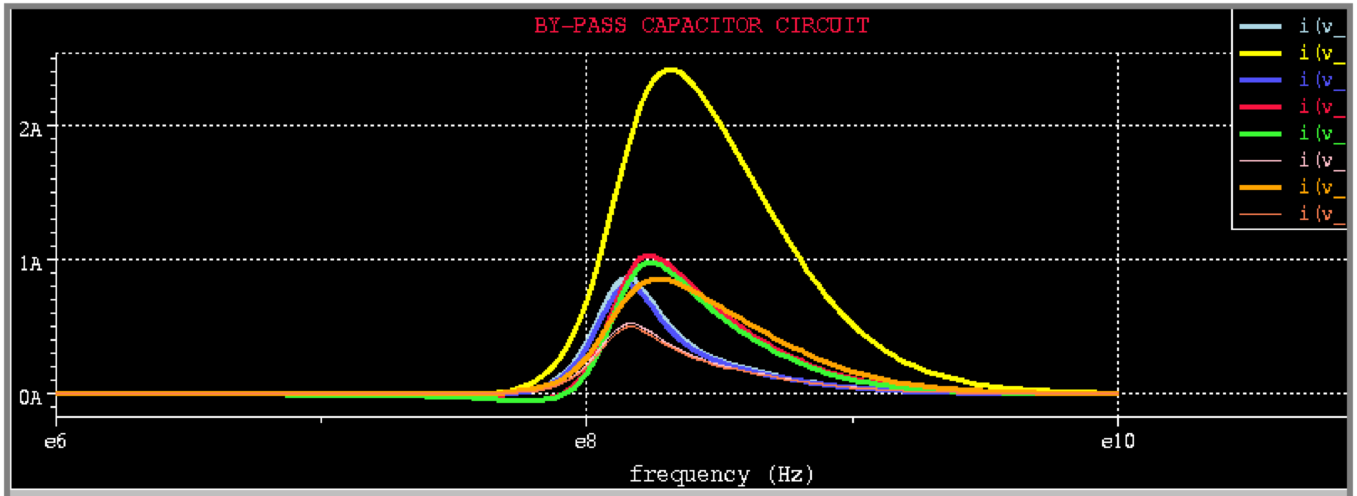
# Simplified Simulation View of C4 Bumps Tied to a Power Plane

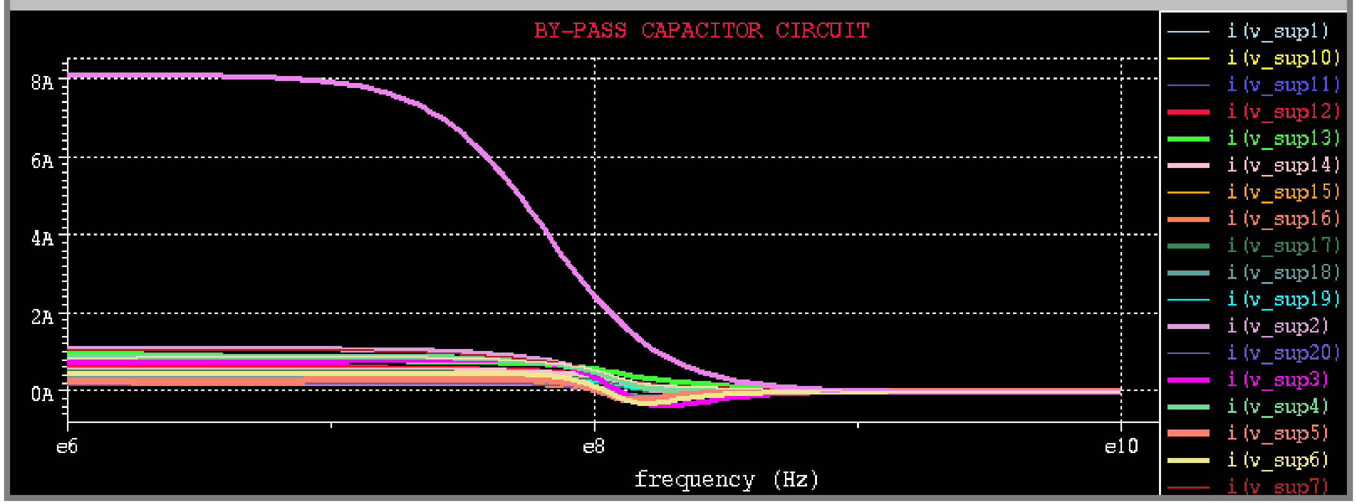


# Capacitor and Pin Currents versus Frequency

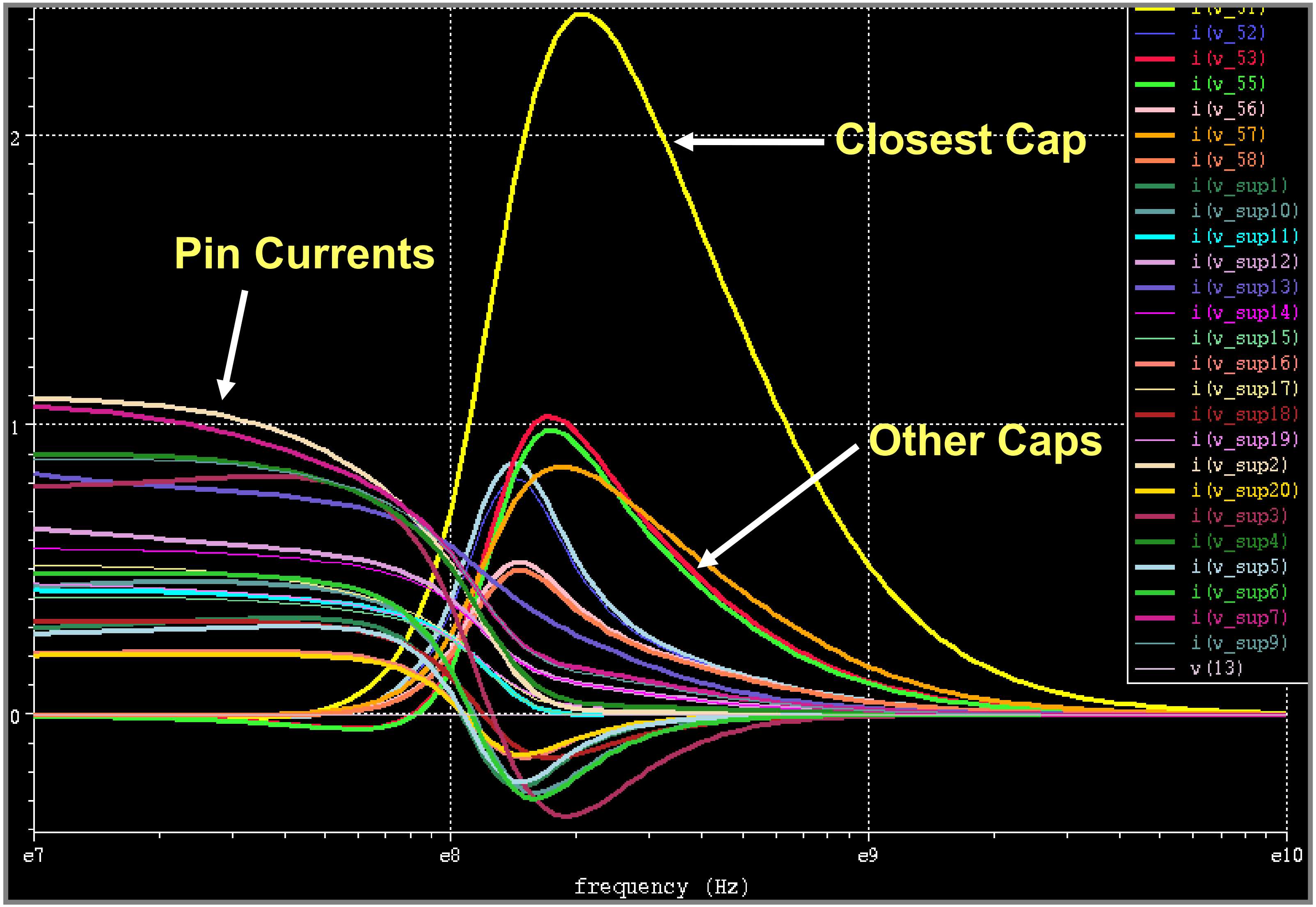
**Capacitor currents:**
**Current starts to be drawn from the capacitors at around 100 MHz**

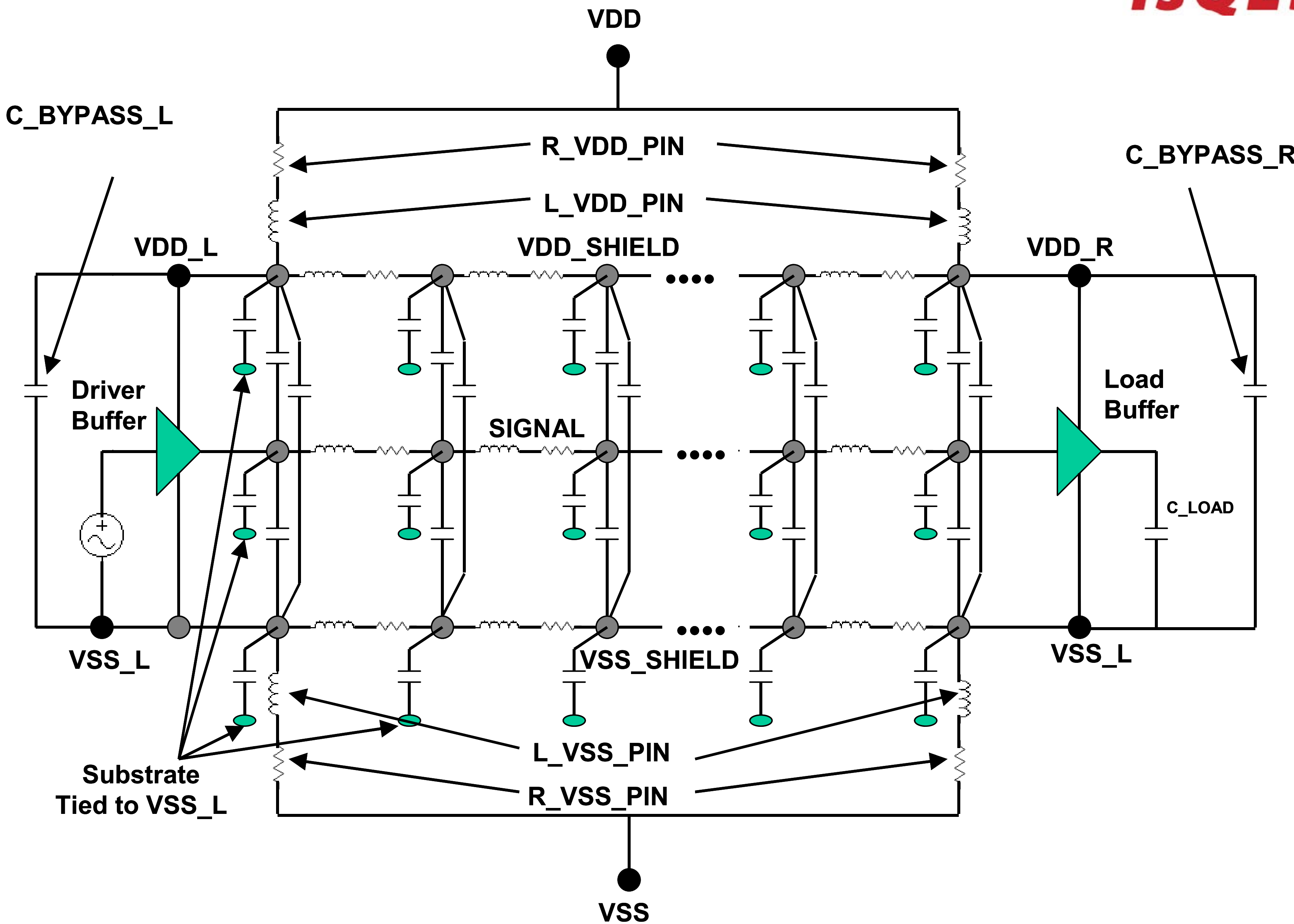
**Pin currents:**
**Most current drawn from closest pin until just before 200 MHz**



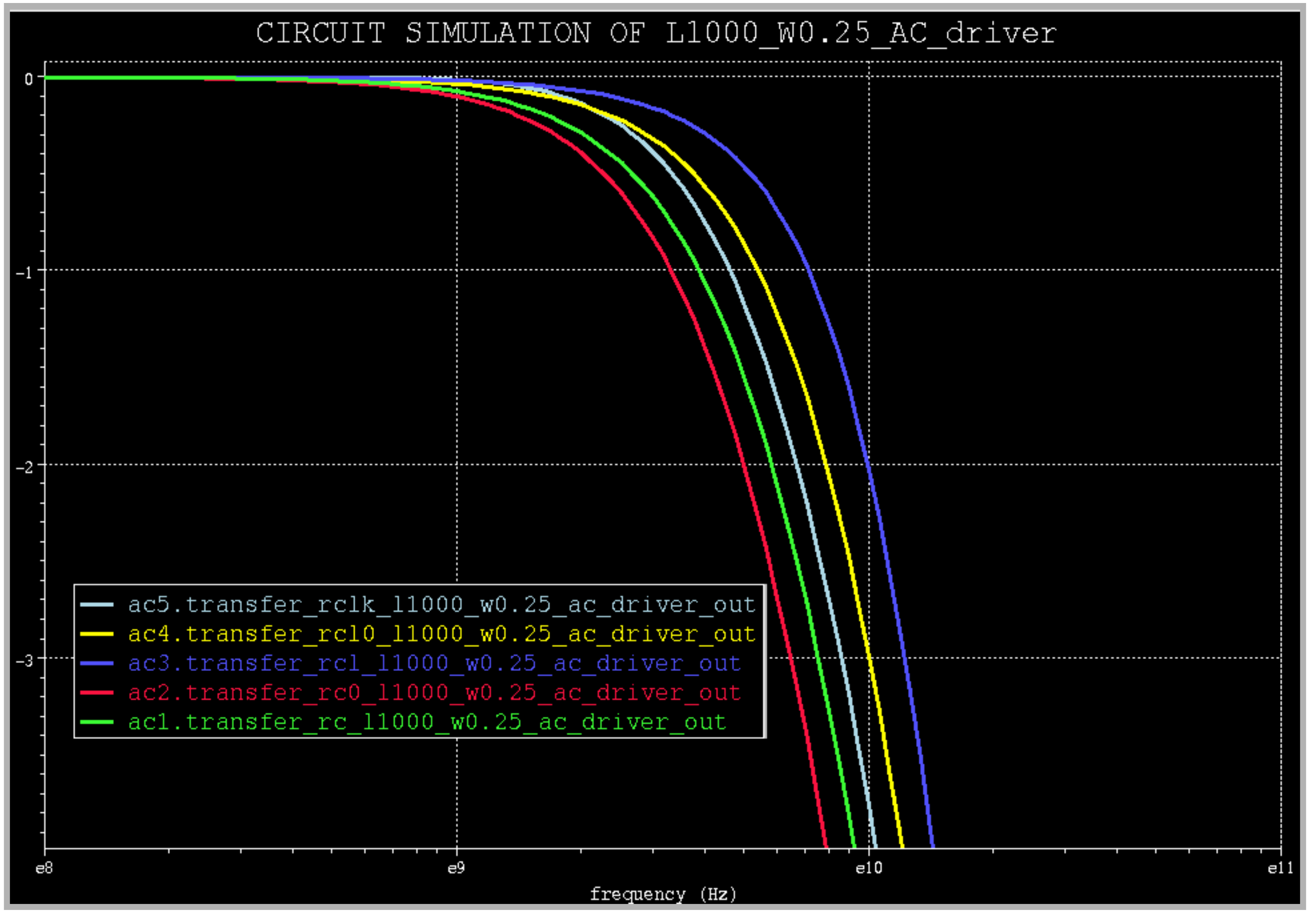



# Capacitor and Pin Currents Crossing Around 200 MHz



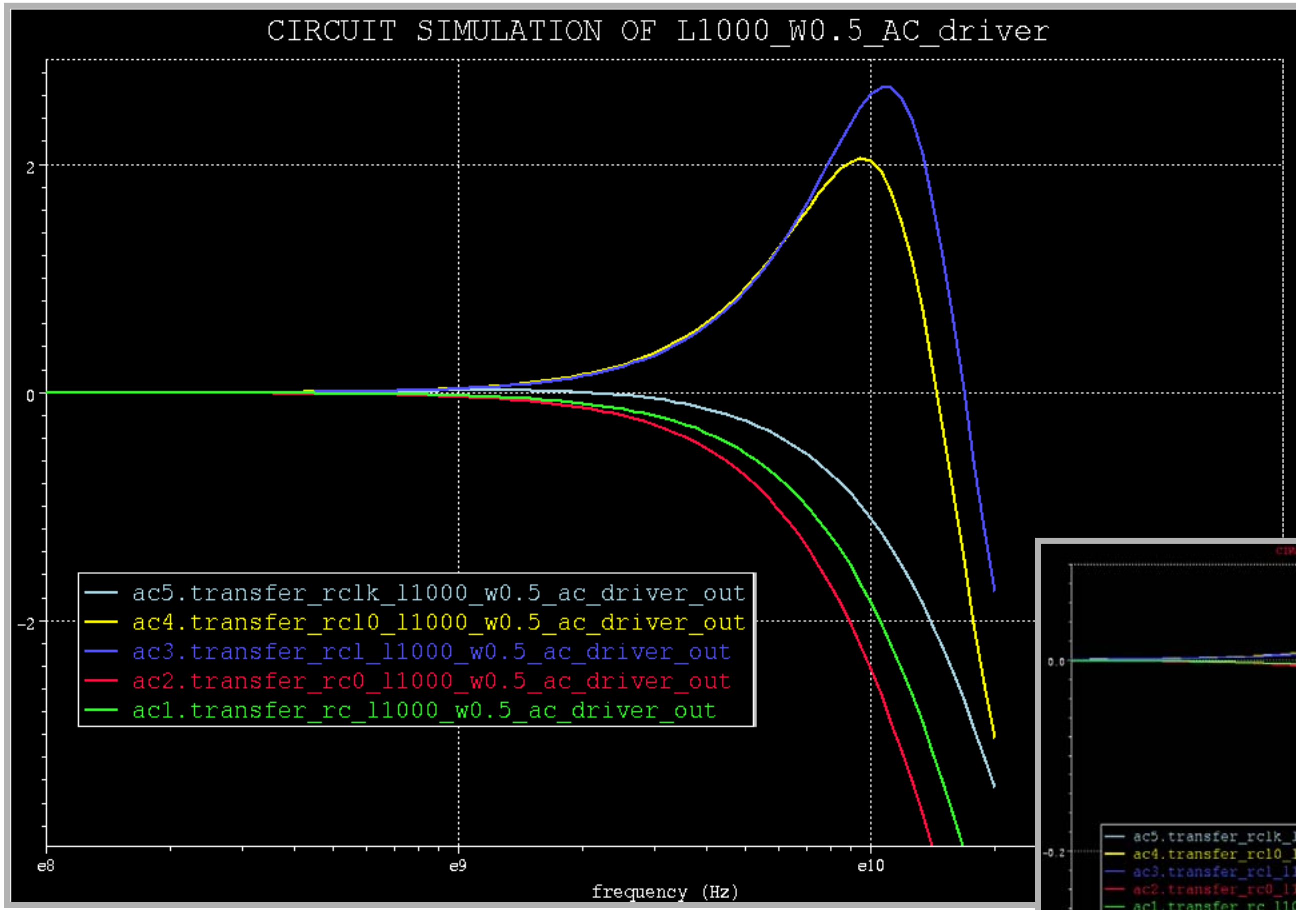

VDD
C_BYPASS_L
R_VDD_PIN
C_BYPASS_R
L_VDD_PIN
VDD_L
VDD_SHIELD
VDD_R
Driver
Buffer
Load
Buffer
SIGNAL
C_LOAD
VSS_L
VSS_SHIELD
VSS_L
L_VSS_PIN
Substrate
Tied to VSS_L
R_VSS_PIN
VSS

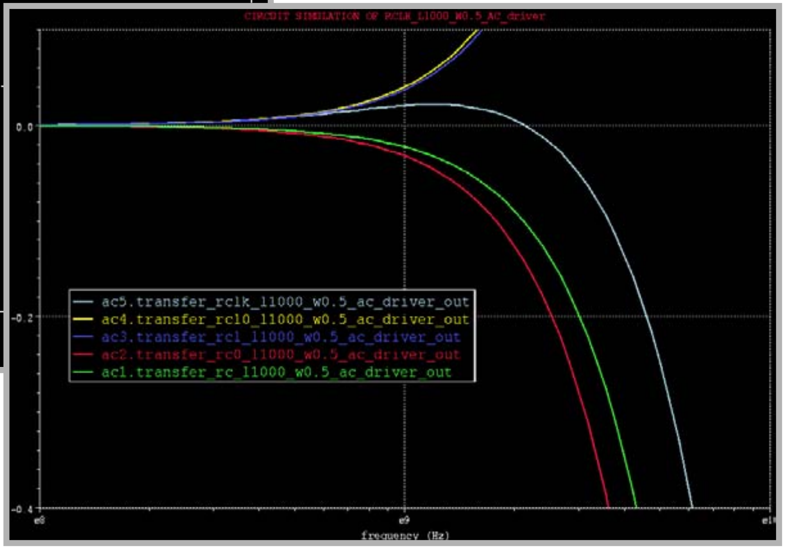
# $RC^{(0)}$, $RLC^{(0)}$, RC, RCL, RCLK Transfer Characteristics




Length = 1000 μ
Width = 0.25 μ

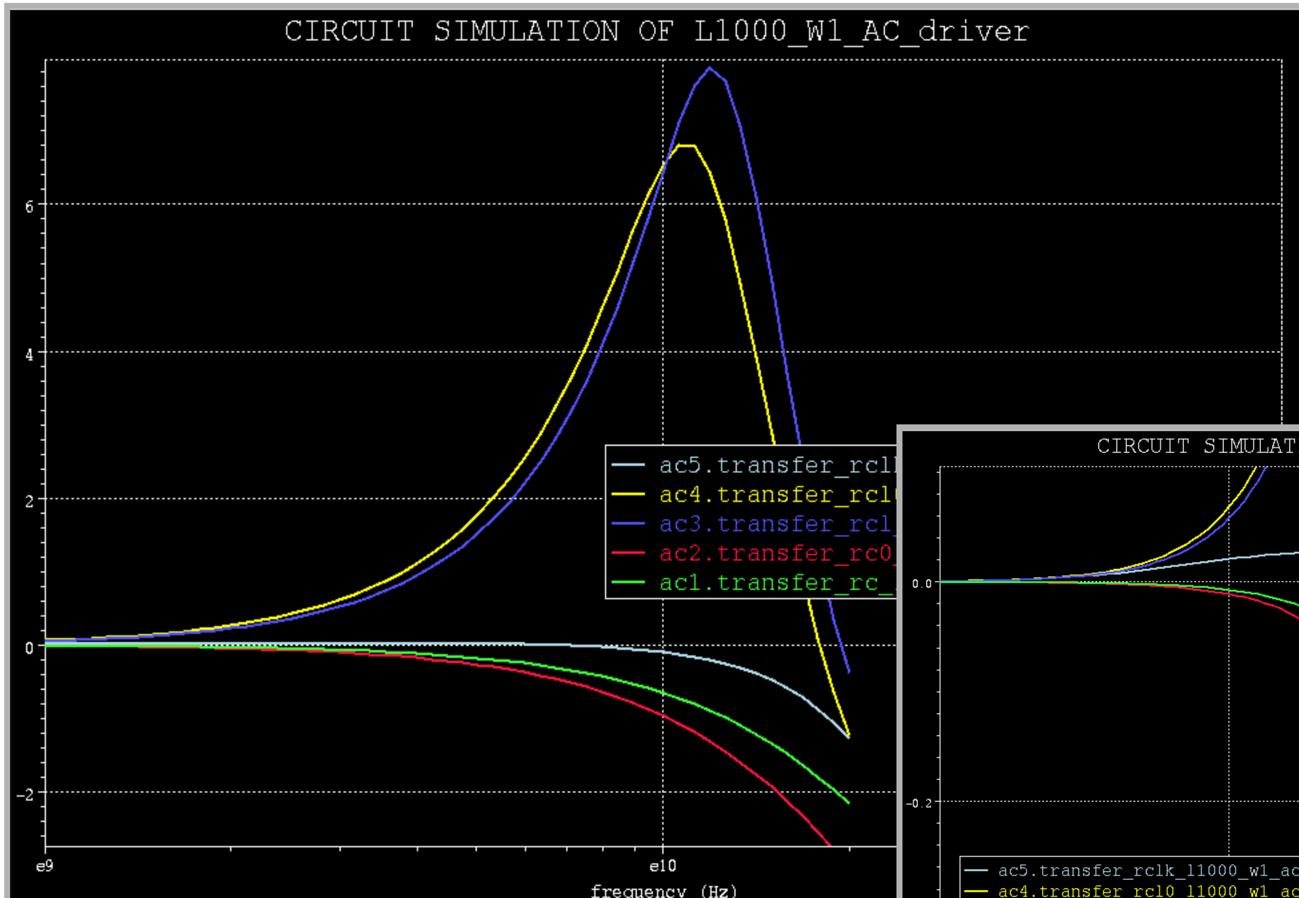
# RC(0), RLC(0), RC, RCL, RCLK Transfer Characteristics

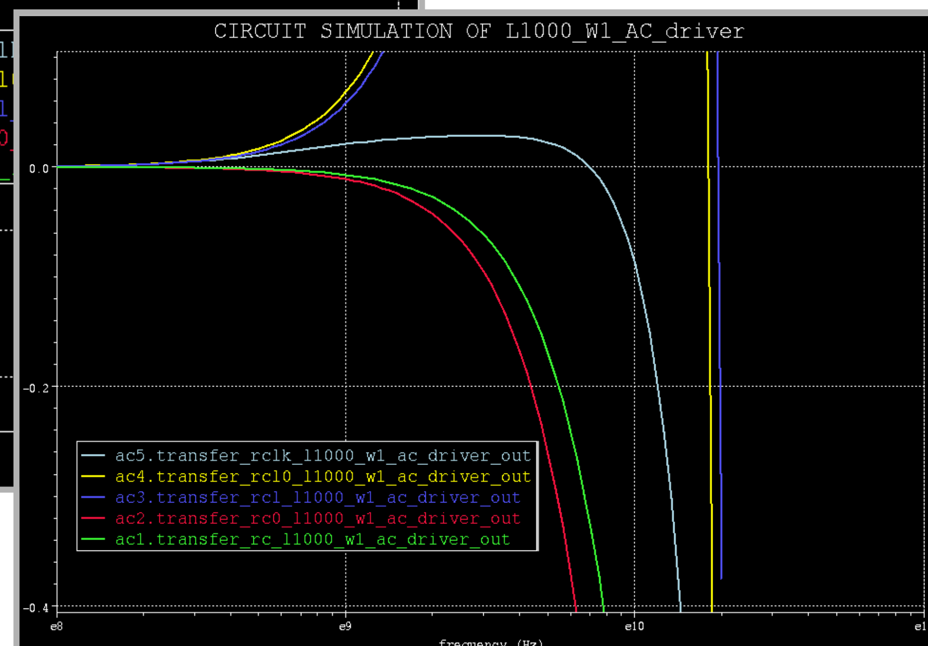



Length = 1000 μ
Width = 0.5 μ

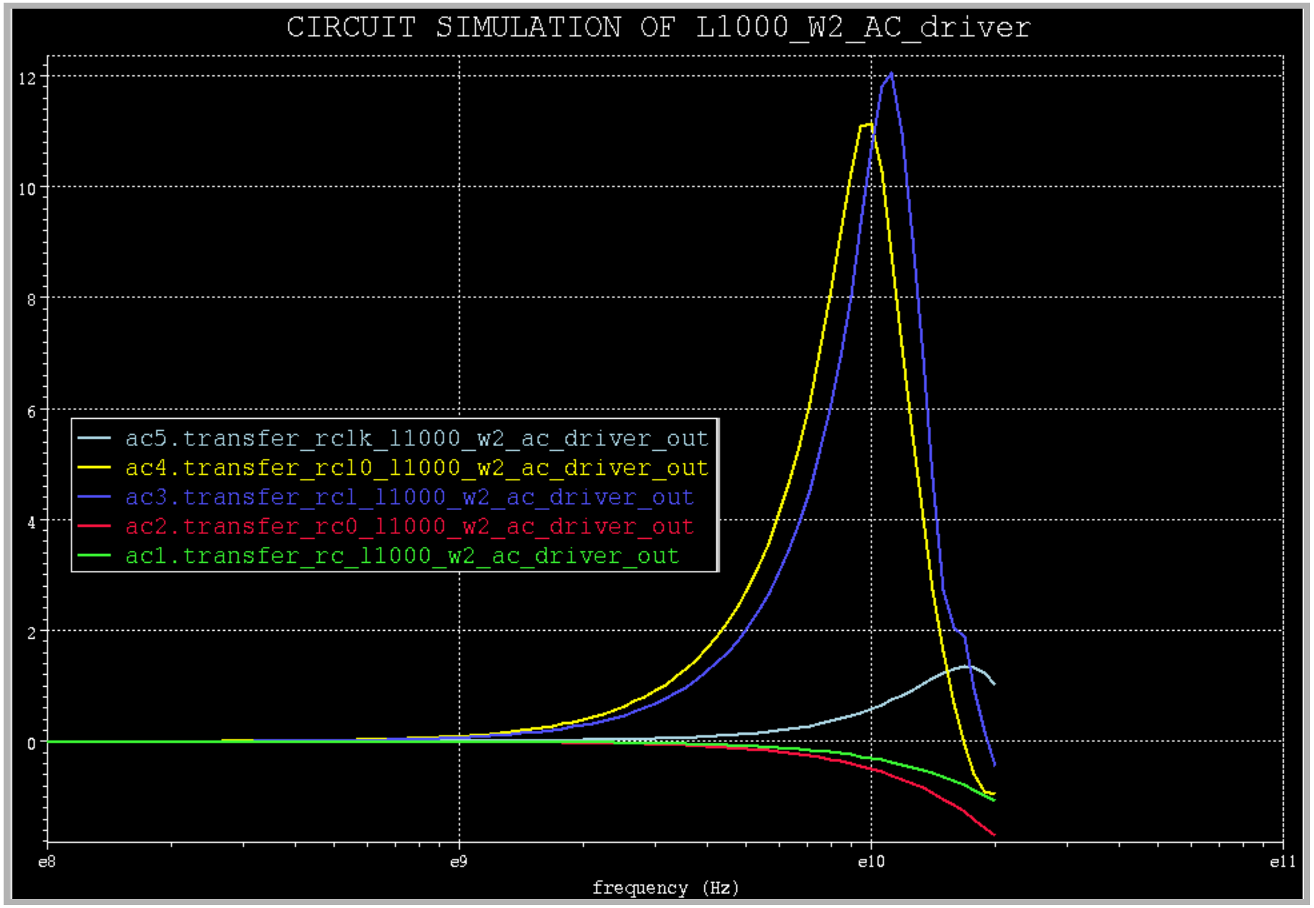
# RC$^{(0)}$, RLC$^{(0)}$, RC, RCL, RCLK Transfer Characteristics



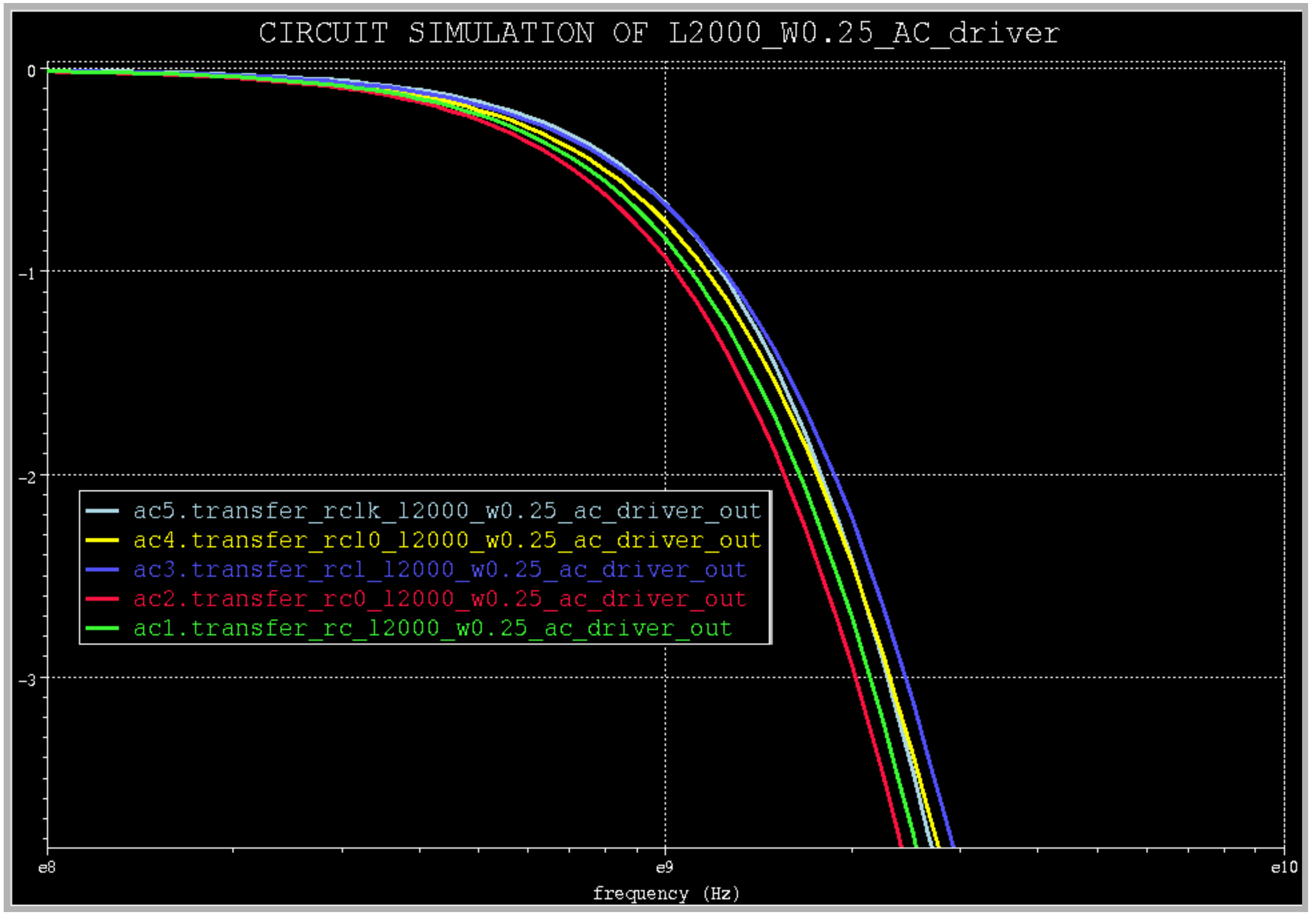

Length = 1000 μ
Width = 1.0 μ

# RC$^{(0)}$, RLC$^{(0)}$, RC, RCL, RCLK Transfer Characteristics



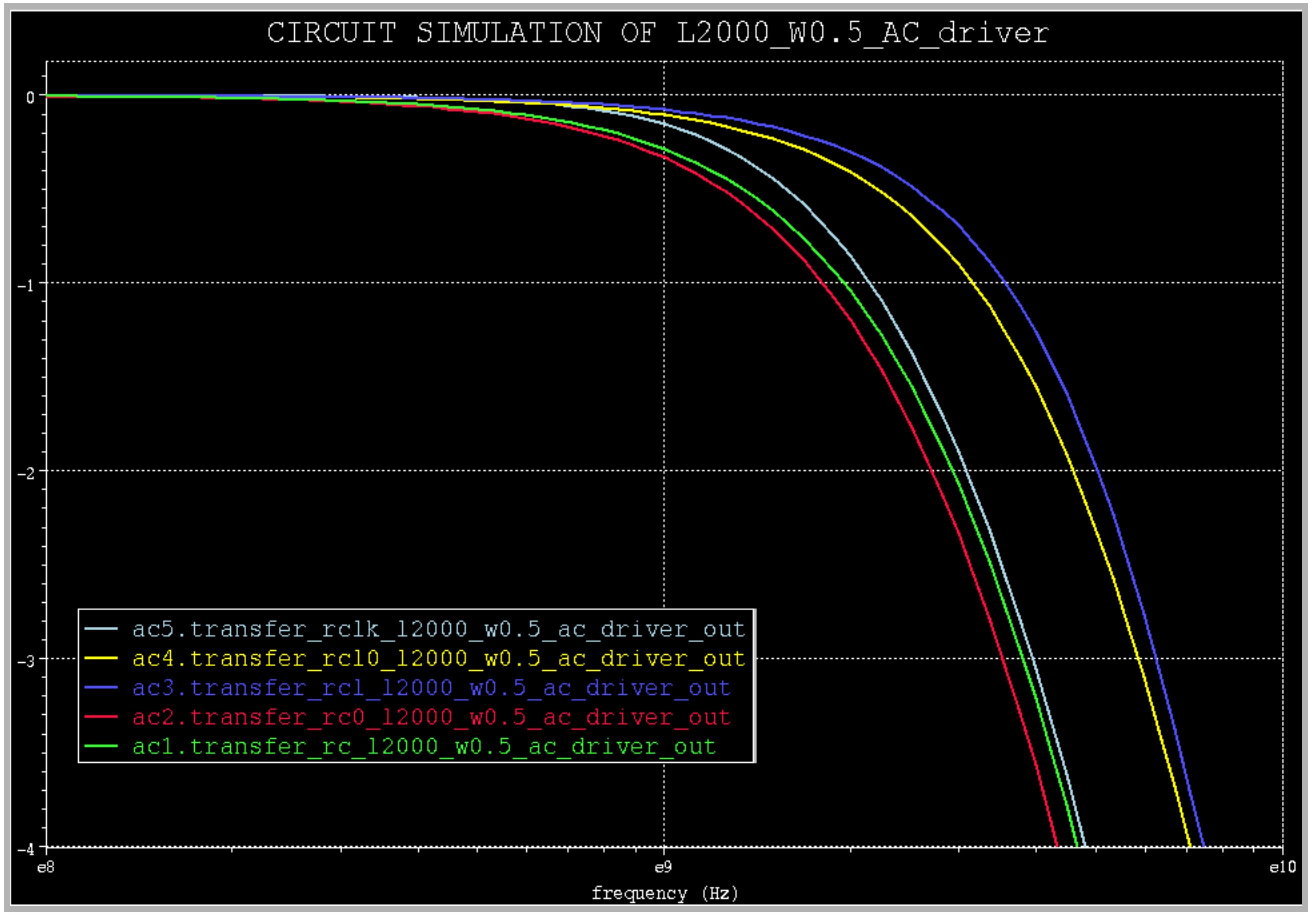

Length = 1000 μ
Width = 2.0 μ

# RC$^{(0)}$, RLC$^{(0)}$, RC, RCL, RCLK Transfer Characteristics



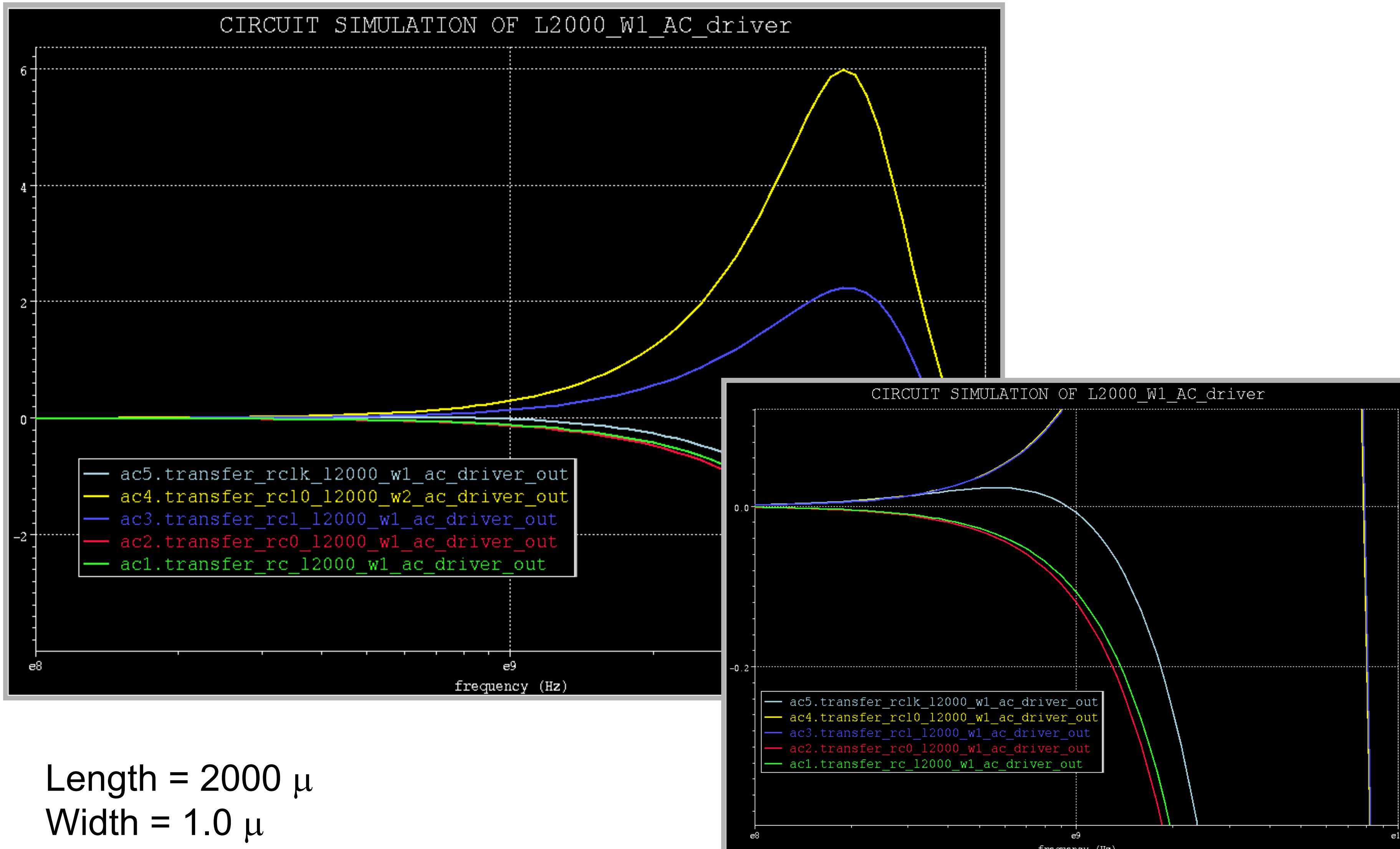

Length = 2000 μ
Width = 0.25 μ

# RC$^{(0)}$, RLC$^{(0)}$, RC, RCL, RCLK Transfer Characteristics



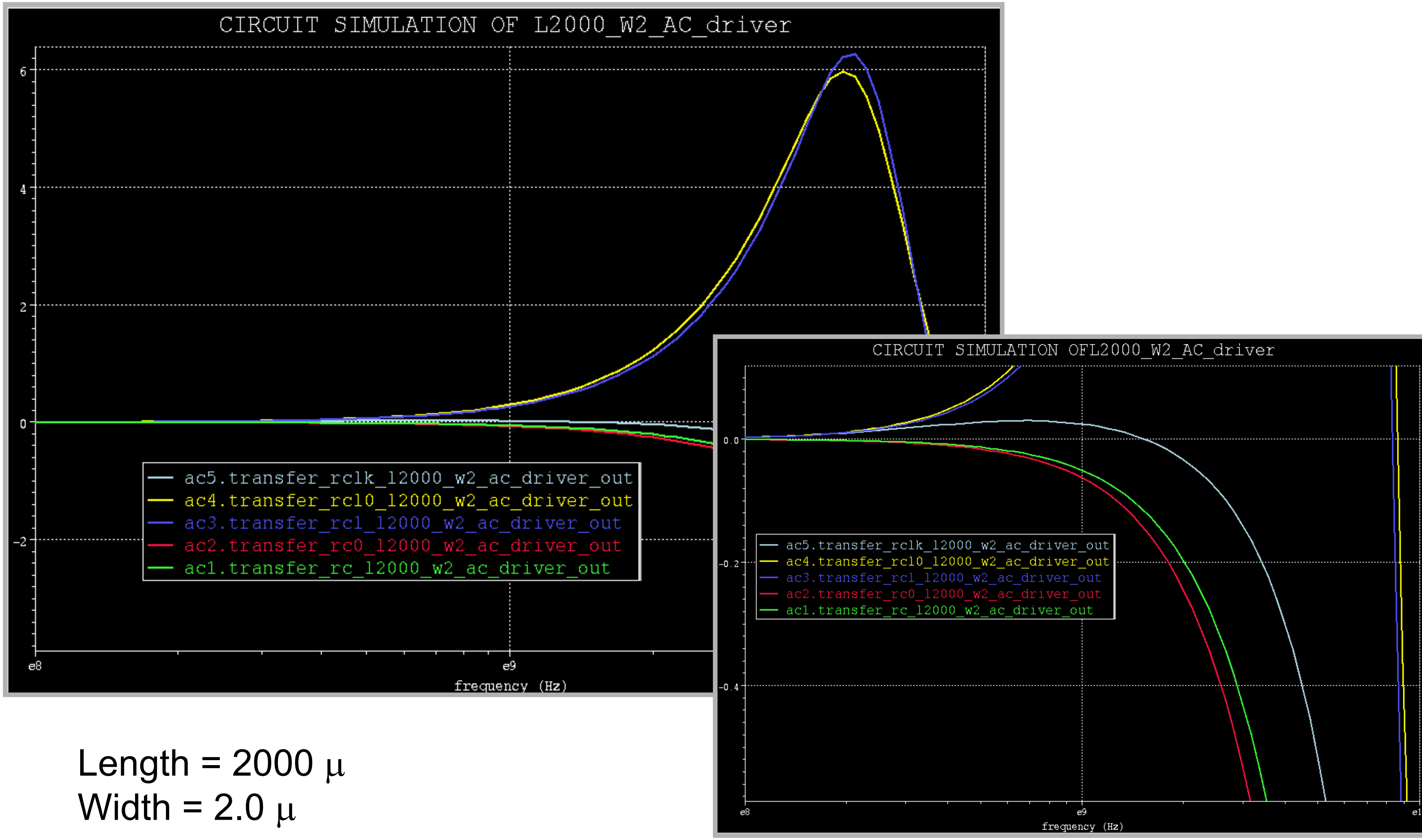

Length = 2000 μ
Width = 0.5 μ

# RC$^{(0)}$, RLC$^{(0)}$, RC, RCL, RCLK Transfer Characteristics



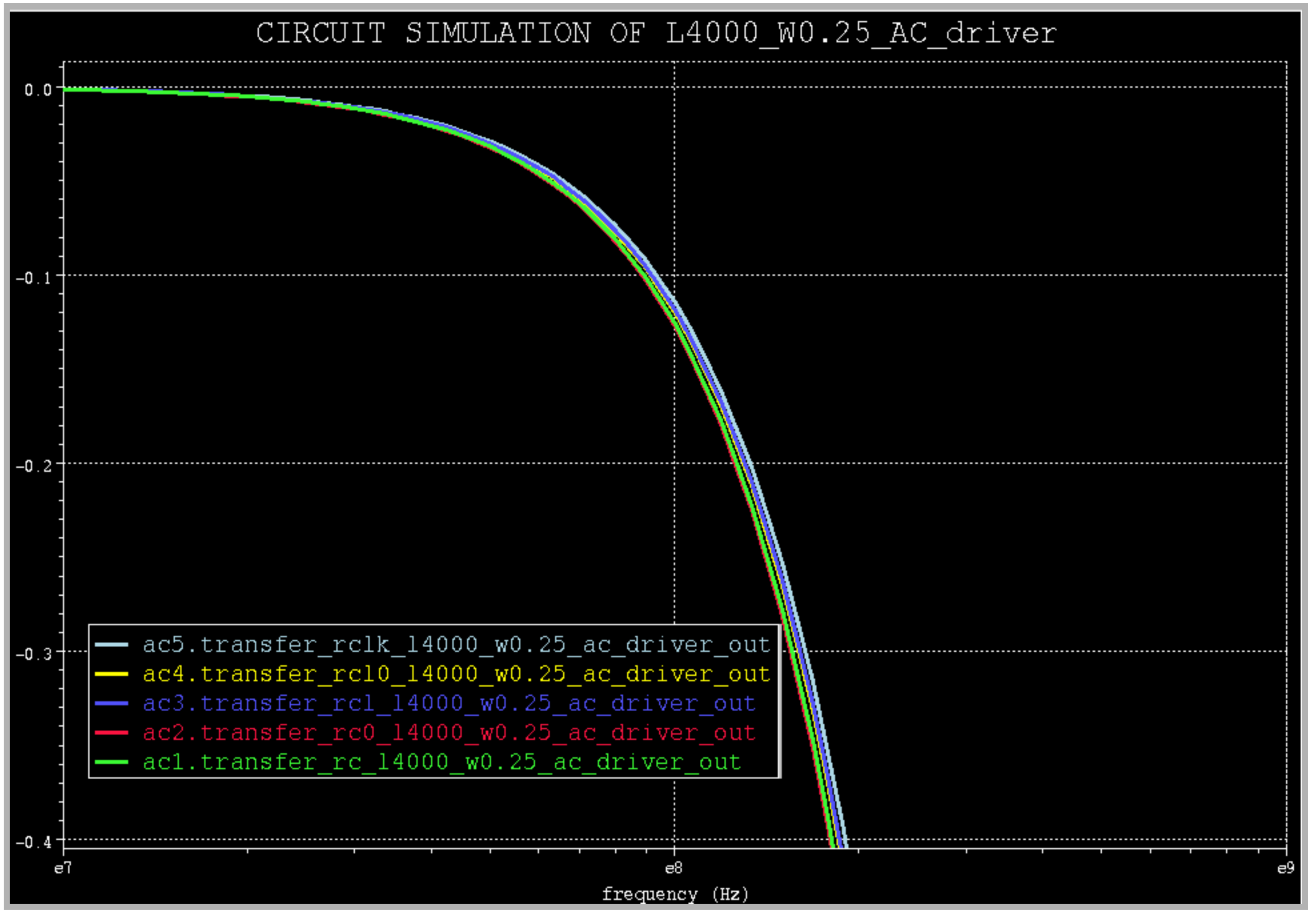

Length = 2000 μ
Width = 1.0 μ

# $RC^{(0)}$, $RLC^{(0)}$, RC, RCL, RCLK Transfer Characteristics



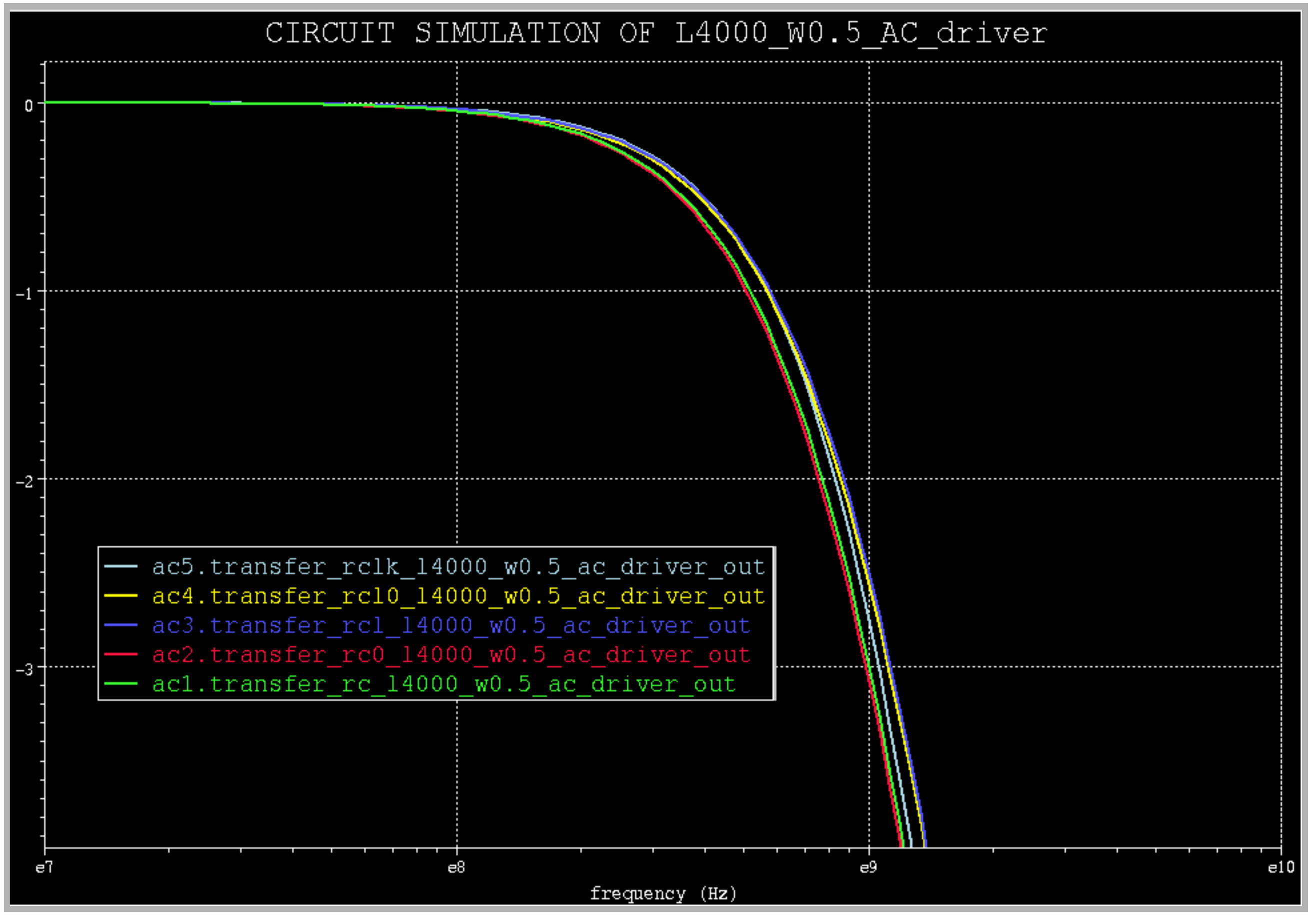

Length = 2000 μ
Width = 2.0 μ

# $RC^{(0)}$, $RLC^{(0)}$, RC, RCL, RCLK Transfer Characteristics



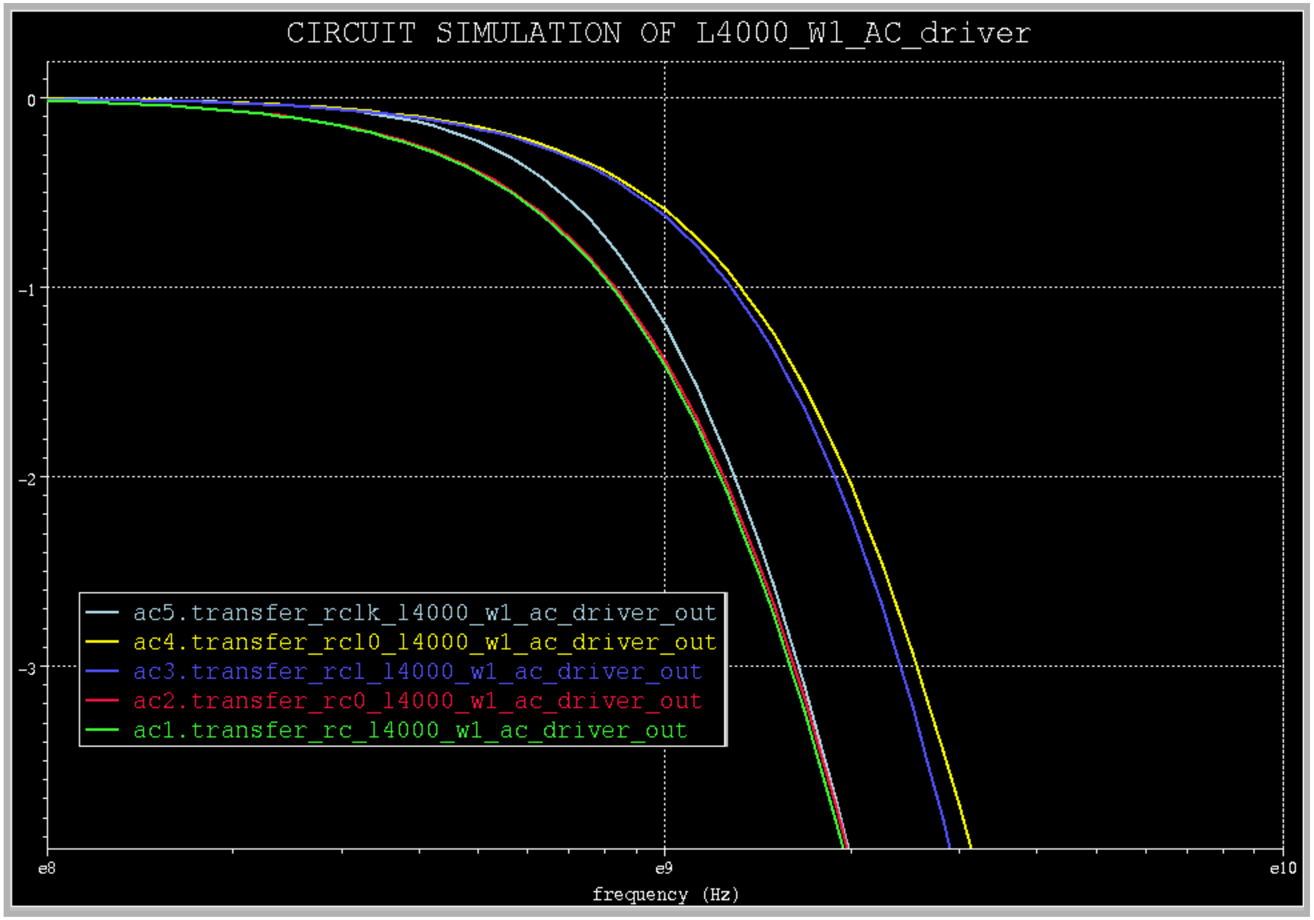

Length = 4000 μ
Width = 0.25 μ

# RC$^{(0)}$, RLC$^{(0)}$, RC, RCL, RCLK Transfer Characteristics



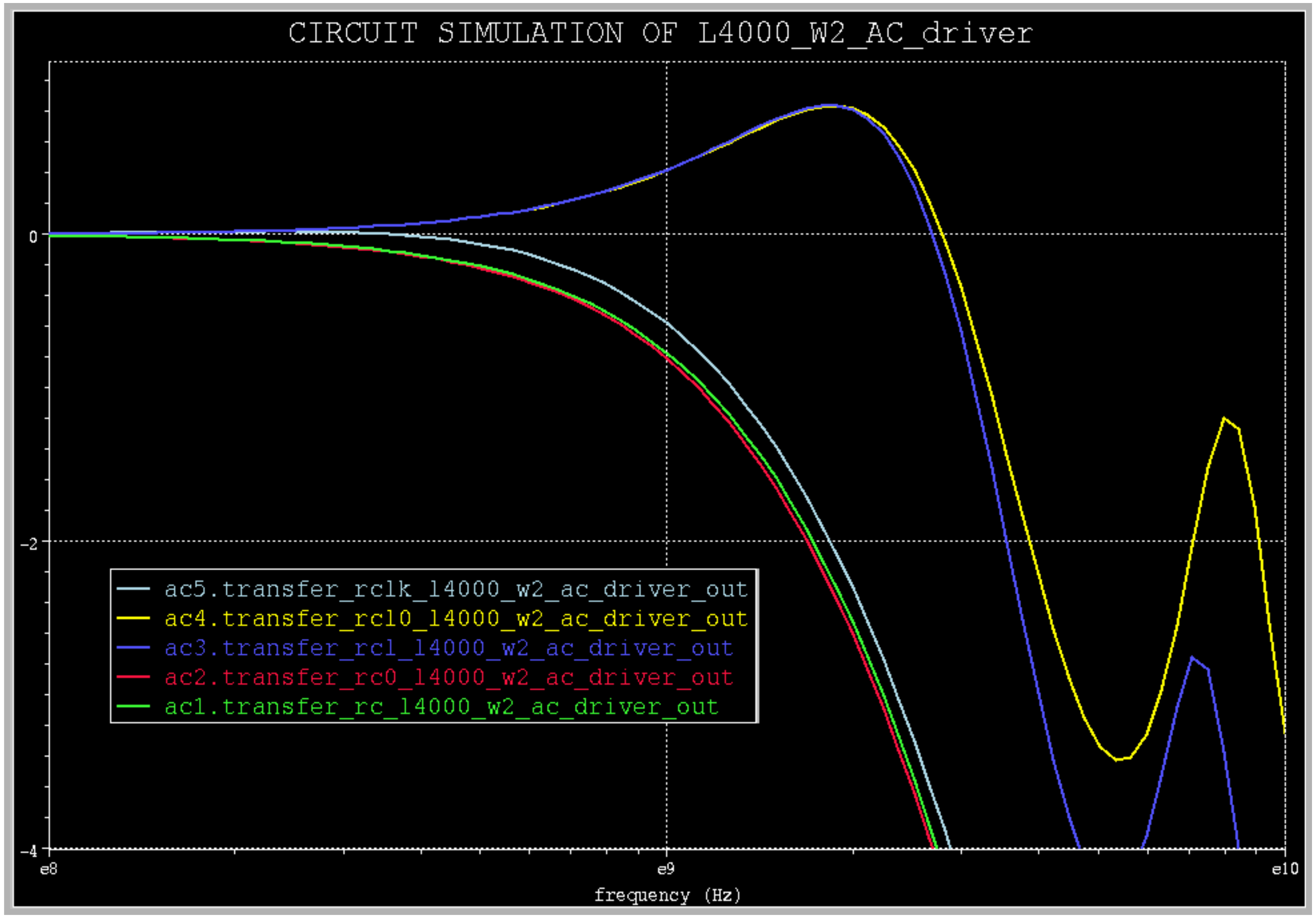

Length = 4000 μ
Width = 0.5 μ

# RC$^{(0)}$, RLC$^{(0)}$, RC, RCL, RCLK Transfer Characteristics



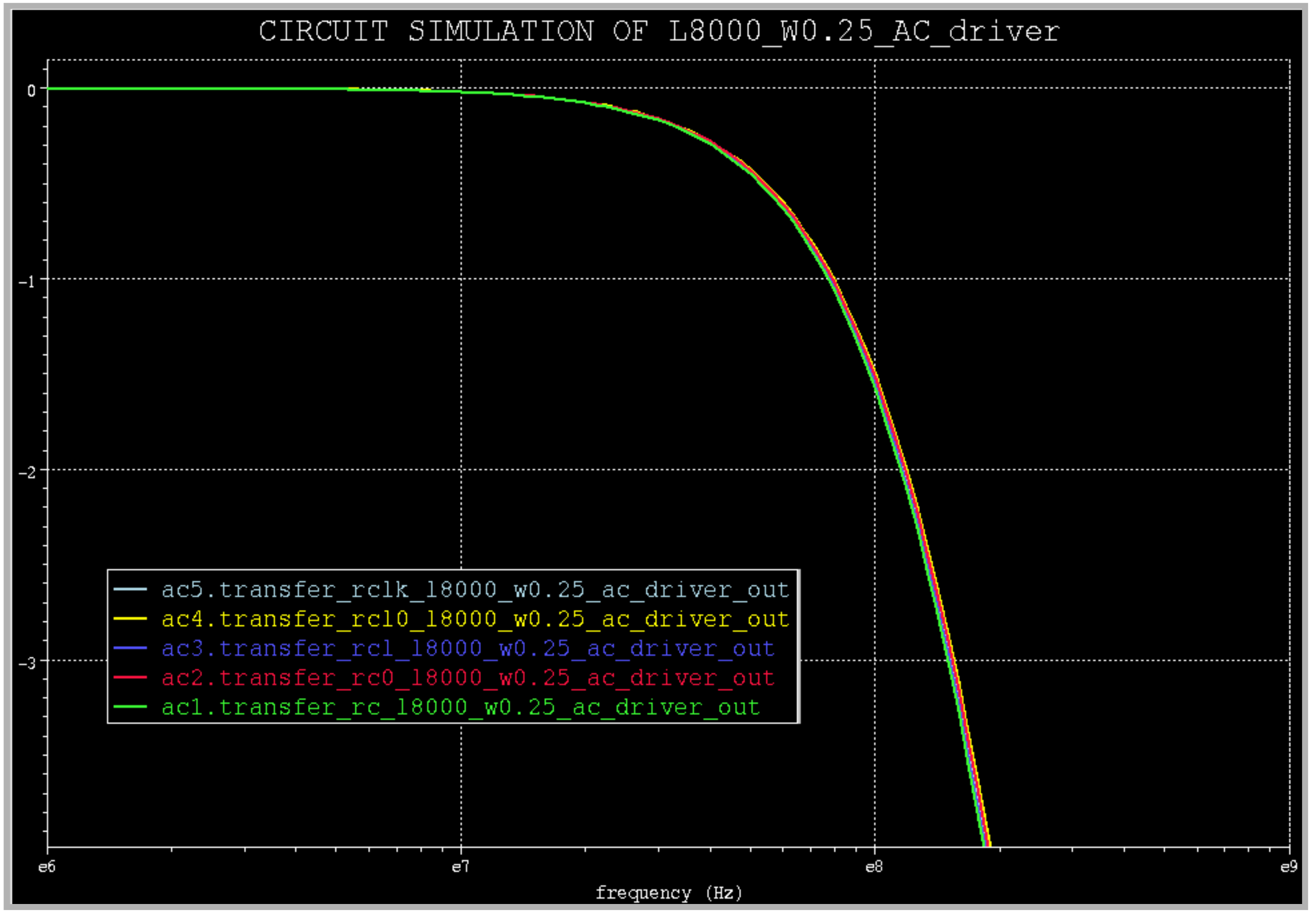

Length = 4000 μ
Width = 1.0 μ

# $RC^{(0)}$, $RLC^{(0)}$, RC, RCL, RCLK Transfer Characteristics



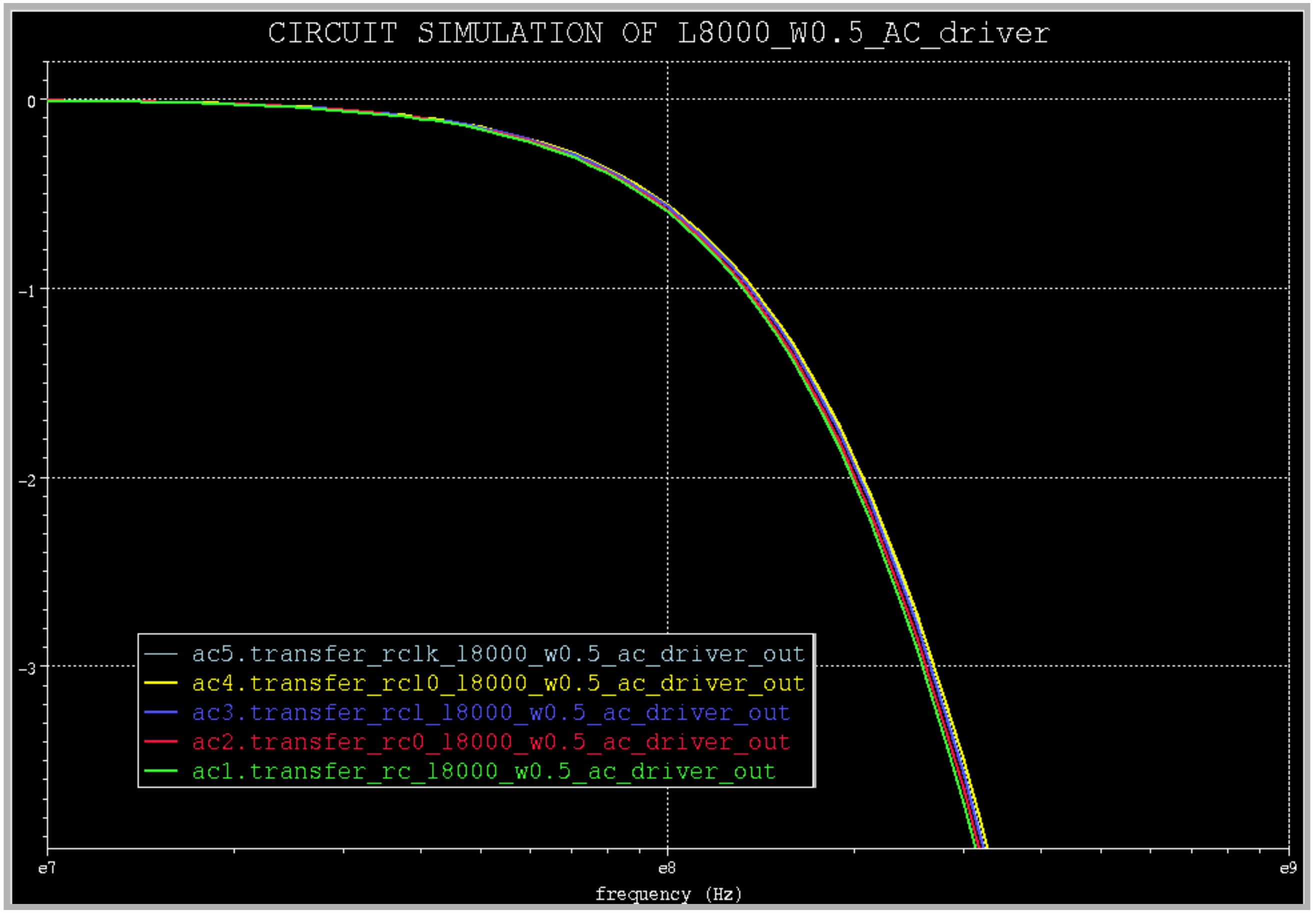

Length = 4000 μ
Width = 2.0 μ

# $RC^{(0)}$, $RLC^{(0)}$, RC, RCL, RCLK Transfer Characteristics



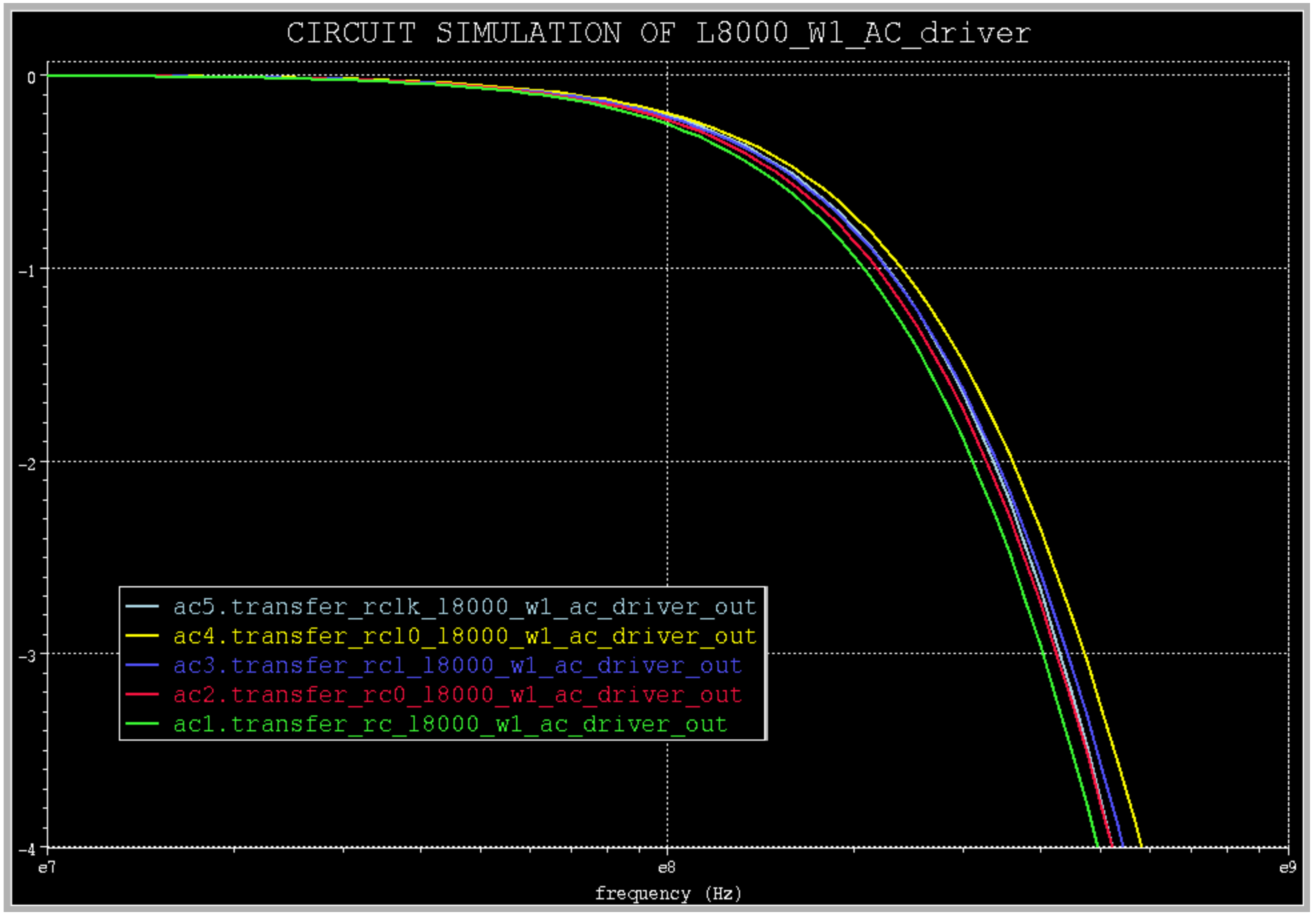

Length = 8000 μ
Width = 0.25 μ

# $RC^{(0)}$, $RLC^{(0)}$, RC, RCL, RCLK Transfer Characteristics



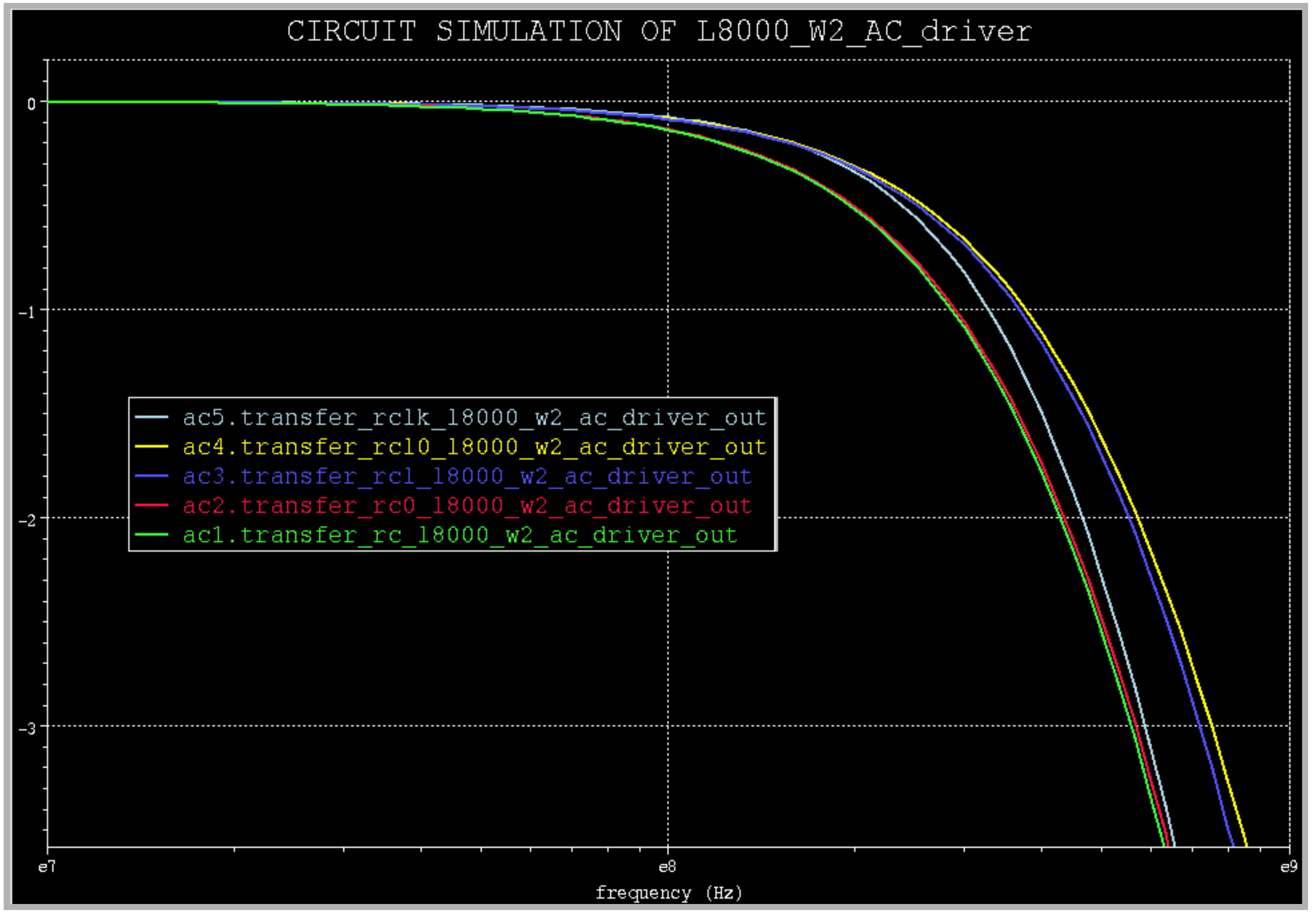

Length = 8000 μ
Width = 0.5 μ

# RC$^{(0)}$, RLC$^{(0)}$, RC, RCL, RCLK Transfer Characteristics



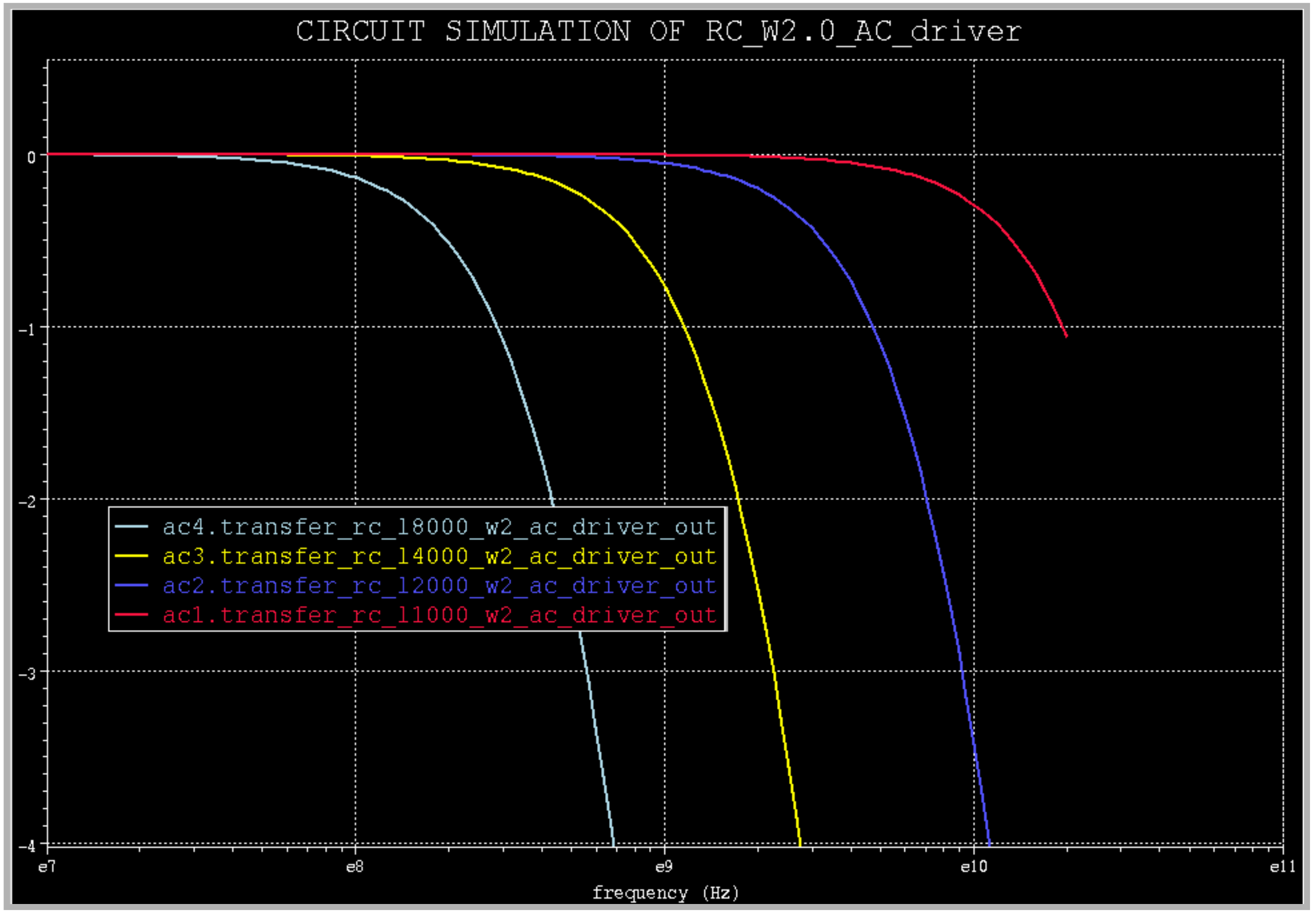

Length = 8000 μ
Width = 1.0 μ

# $RC^{(0)}$, $RLC^{(0)}$, RC, RCL, RCLK Transfer Characteristics



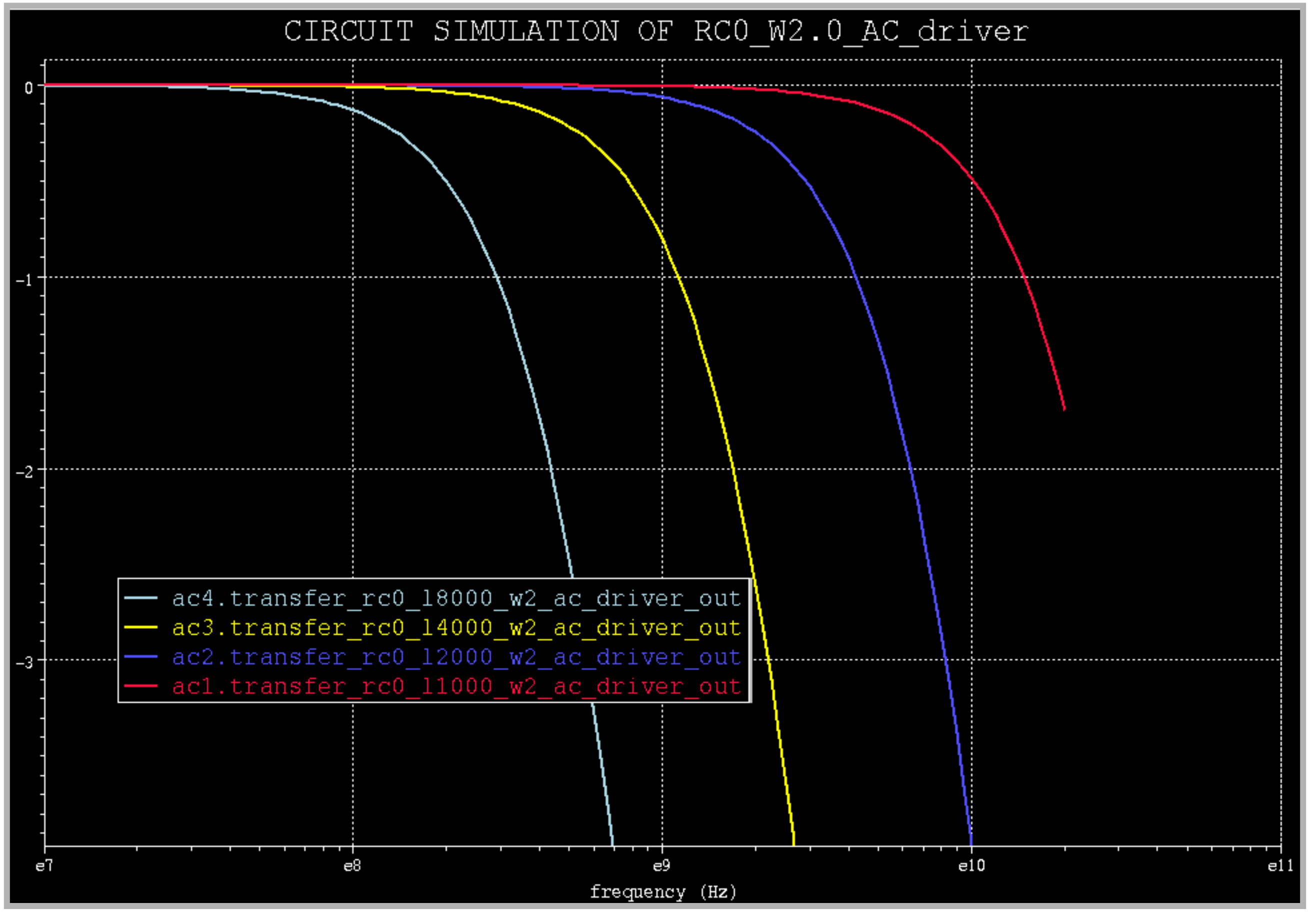

Length = 8000 $\mu$
Width = 2.0 $\mu$

# RC Transfer Characteristics



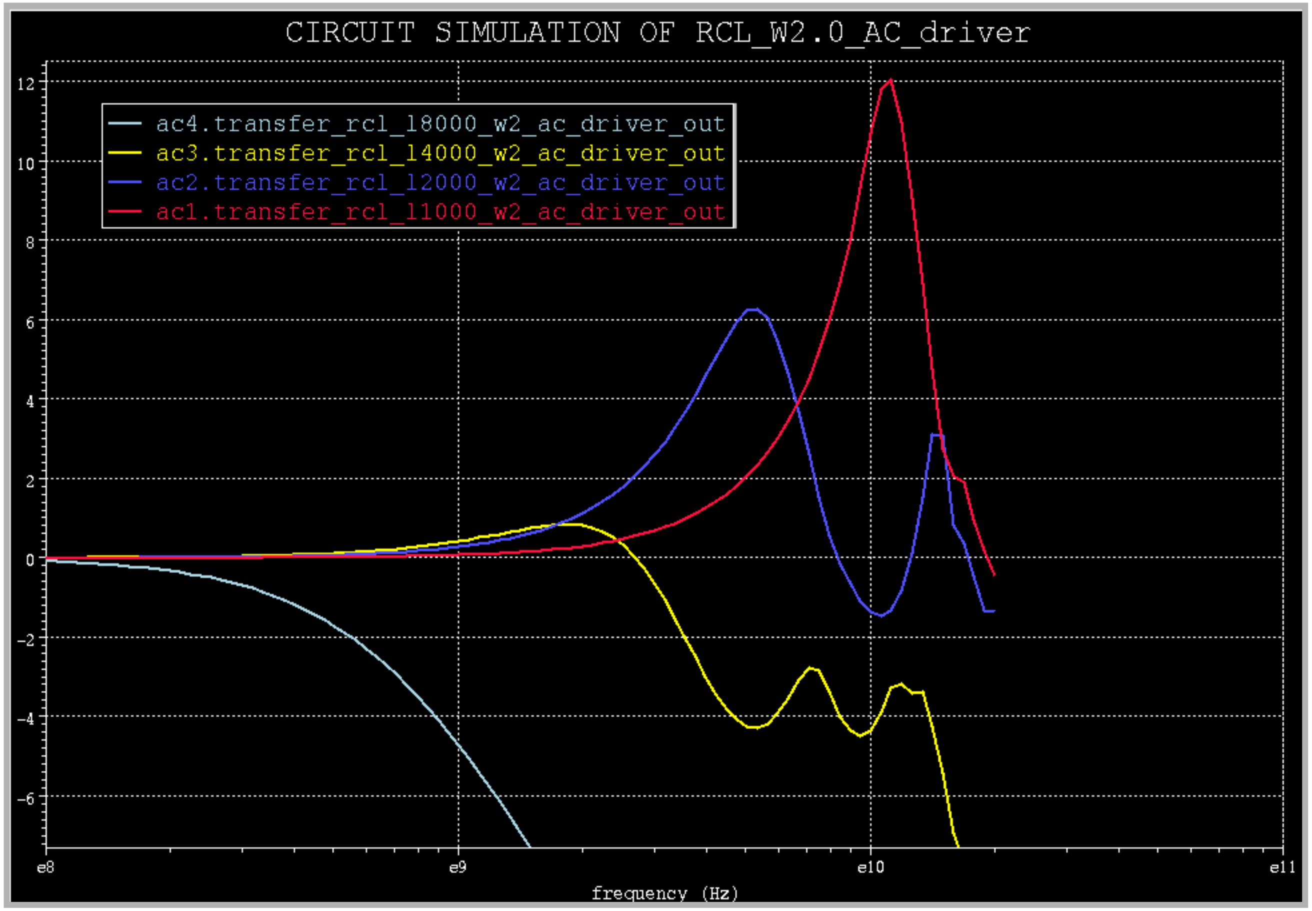

Length = 1000, 2000, 4000, 8000 μ
Width = 2.0 μ

# $RC^{(0)}$ Transfer Characteristics



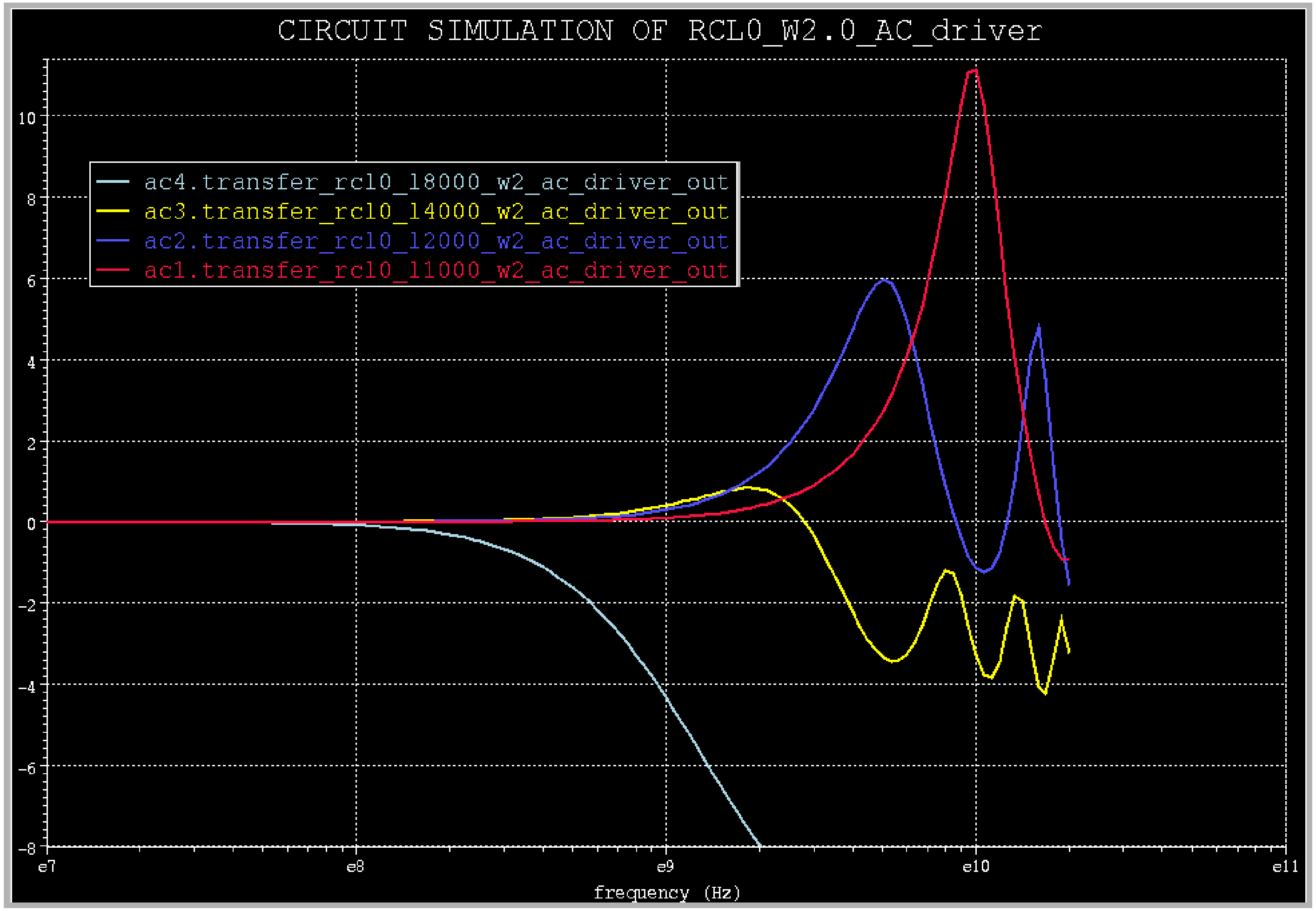

Length = 1000, 2000, 4000, 8000 μ
Width = 2.0 μ

# RCL Transfer Characteristics



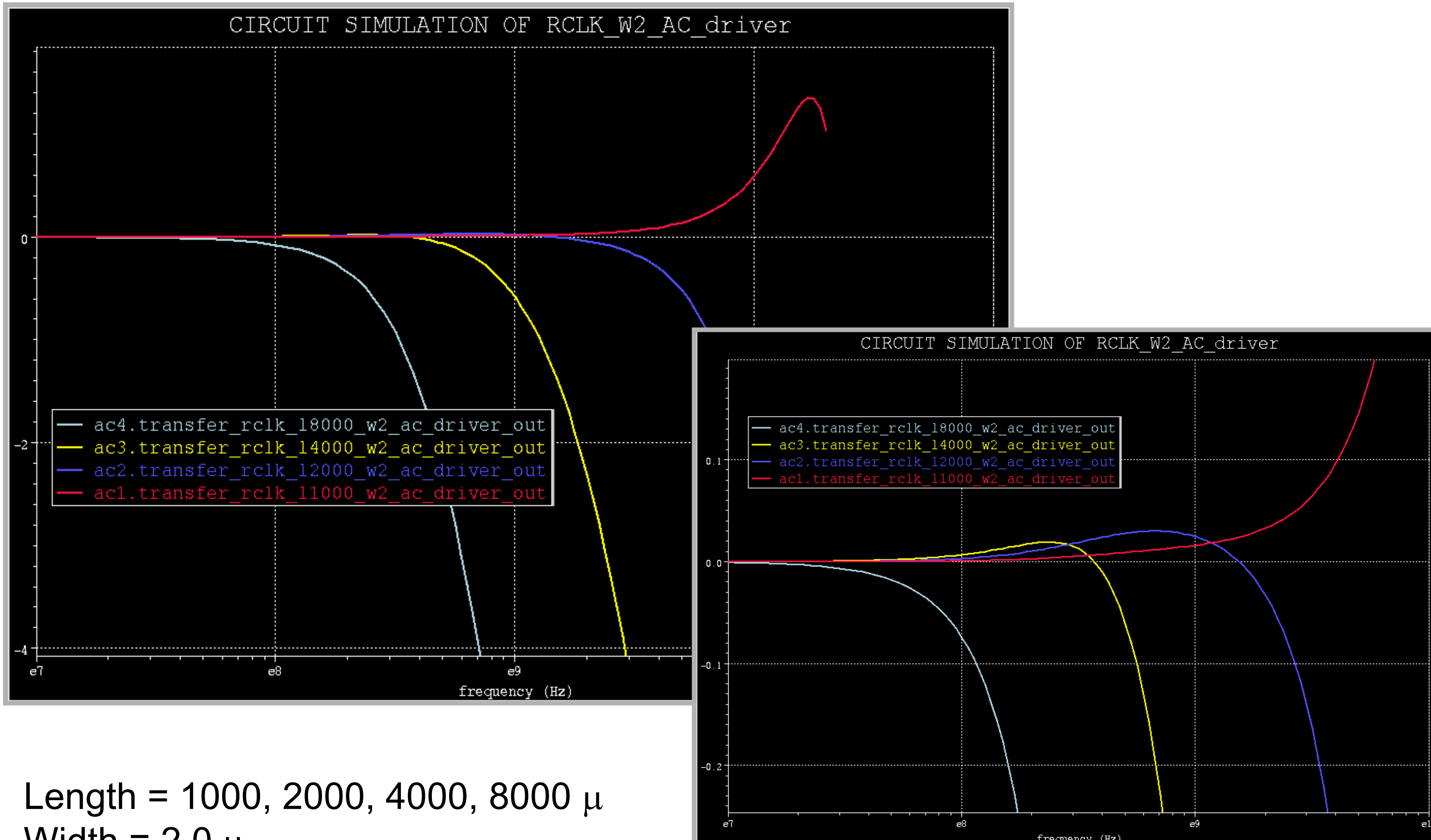

Length = 1000, 2000, 4000, 8000 μ
Width = 2.0 μ

# RLC(0) Transfer Characteristics



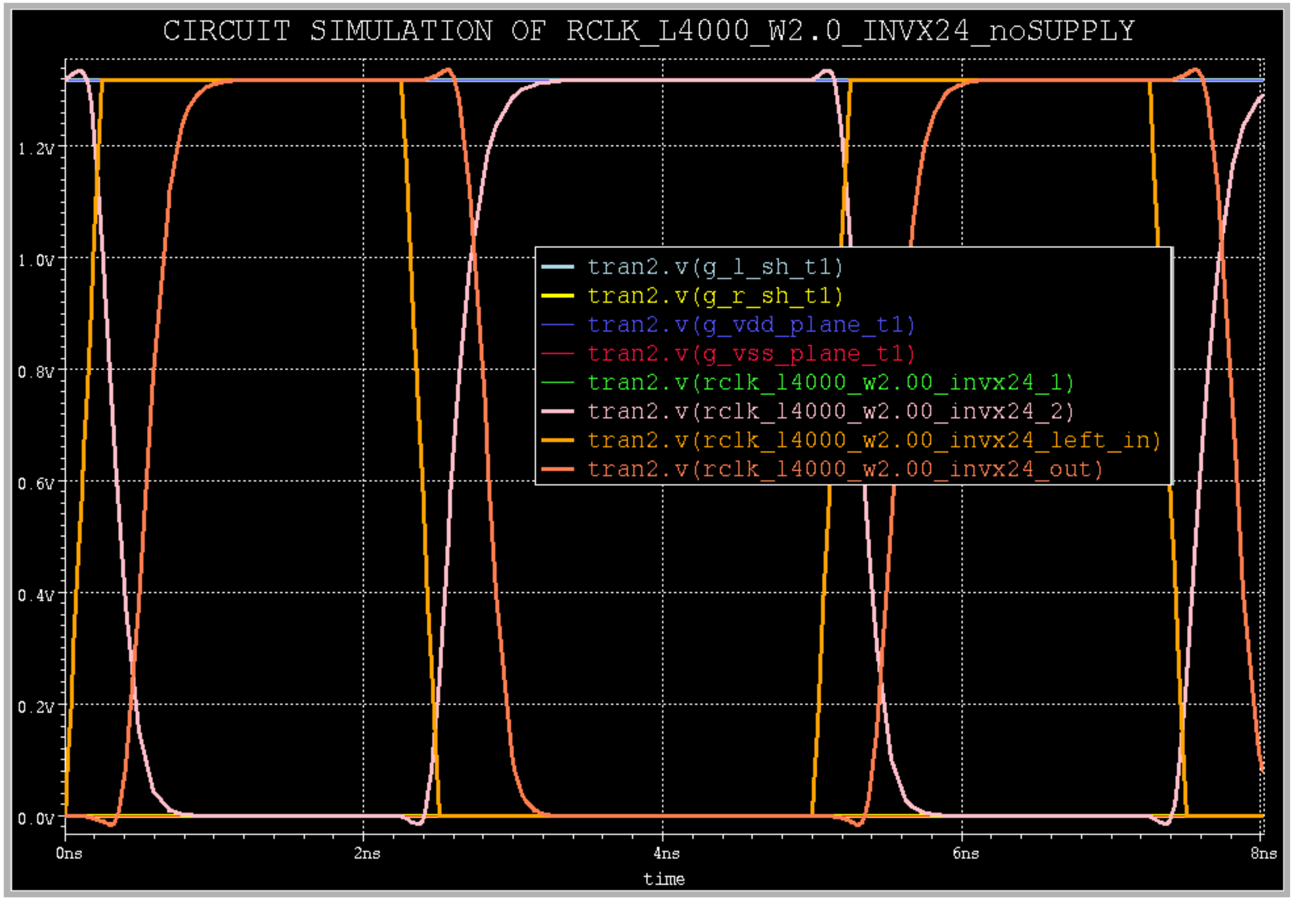

Length = 1000, 2000, 4000, 8000 μ
Width = 2.0 μ

# RCLK Transfer Characteristics



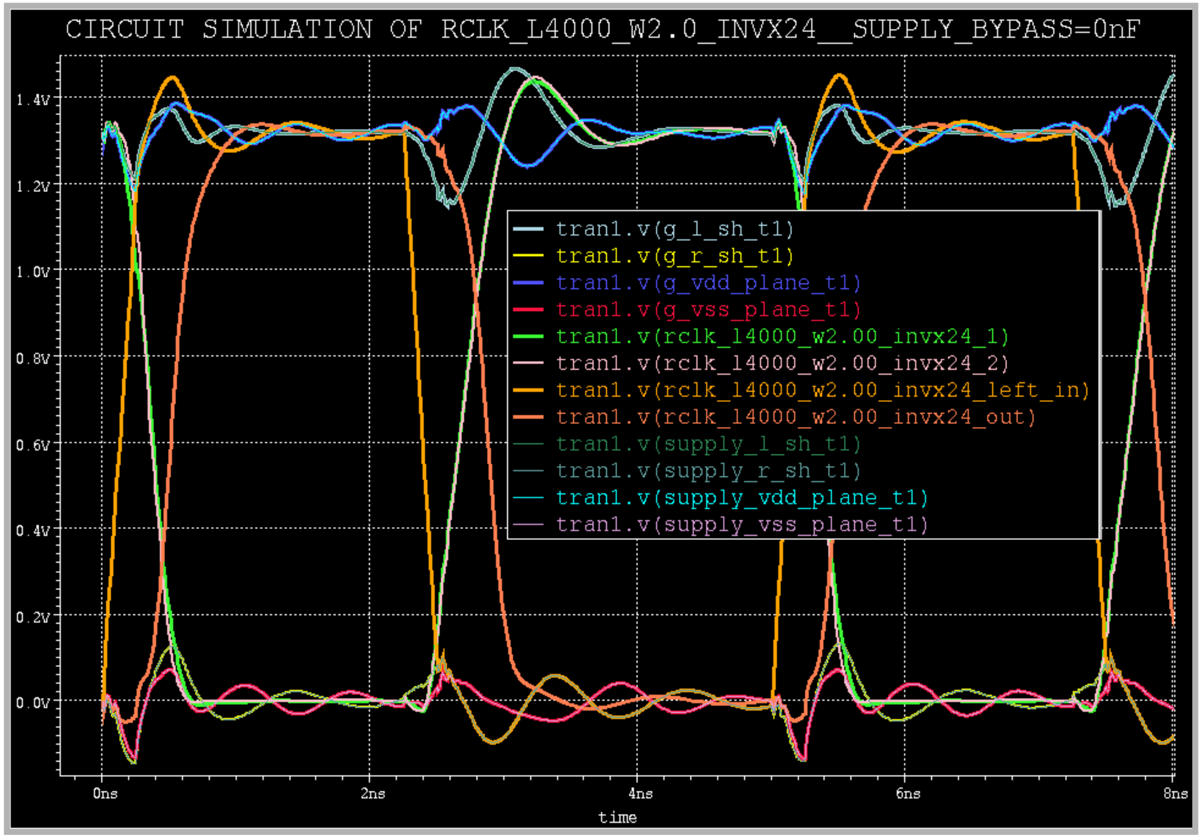

Length = 1000, 2000, 4000, 8000 μ
Width = 2.0 μ

# No VDD/VSS Parasitics



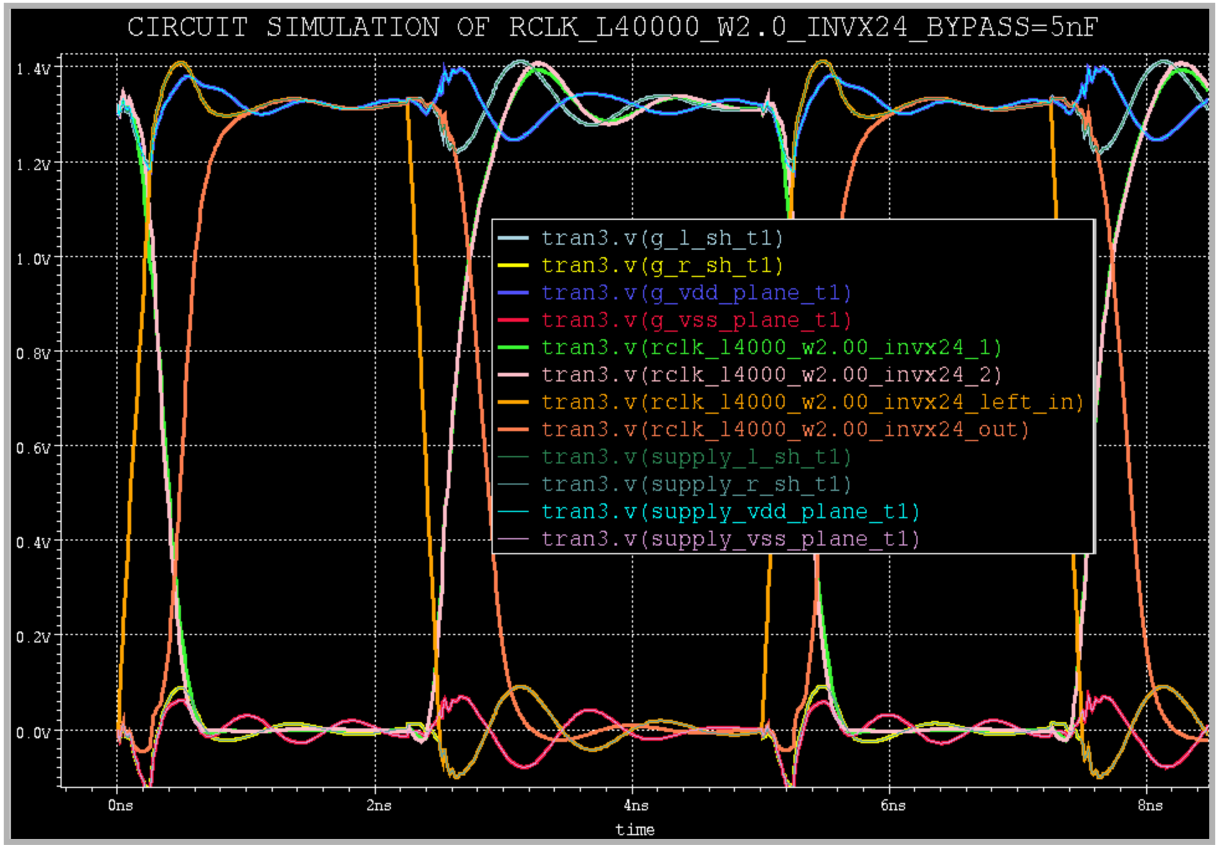

Length = 4000 μ
Width = 2.0 μ
Driver = 24X Inverter
Load = 1X Inverter with 50fF Load

# VDD/VSS Parasitics and No Decoupling Cap




Length = 4000 μ
Width = 2.0 μ
Driver = 24X Inverter
Load = 1X Inverter with 50fF Load

# VDD/VSS Parasitics and 5nF Decoupling Cap




Length = 4000 μ
Width = 2.0 μ
Driver = 24X Inverter
Load = 1X Inverter with 50fF Load

# Summary

1. Choosing $RC^{(0)}$ , $RLC^{(0)}$ , RC, RLC or RLCK Circuit Model for an Arbitrary Interconnect for a Required Degree of Accuracy is not an Easy problem. Selection Depends on the Width, Length and Proximity Circuitry of the Net. Generally "Long" and "Wide" Interconnects Require More Complicated RLCK Circuit Models.

2. For many cases such as, I/O rings, Clocks, Wide and Long Buses VDD/VSS Circuit or its Equivalent With the Package Models Have to be Included into the RLCK Circuit Model of the Signal Nets.

3. On-Chip Inductance Effects, can be controlled with effective shielding. Deciding on a shielding Strategy Could be Determined with a Large Number of Simulations.

4. Including the On-Chip Decoupling Capacitors into the Simulations with the VDD/VSS Networks is a "Must" for Critical Nets. Too Risky to Ignore!!