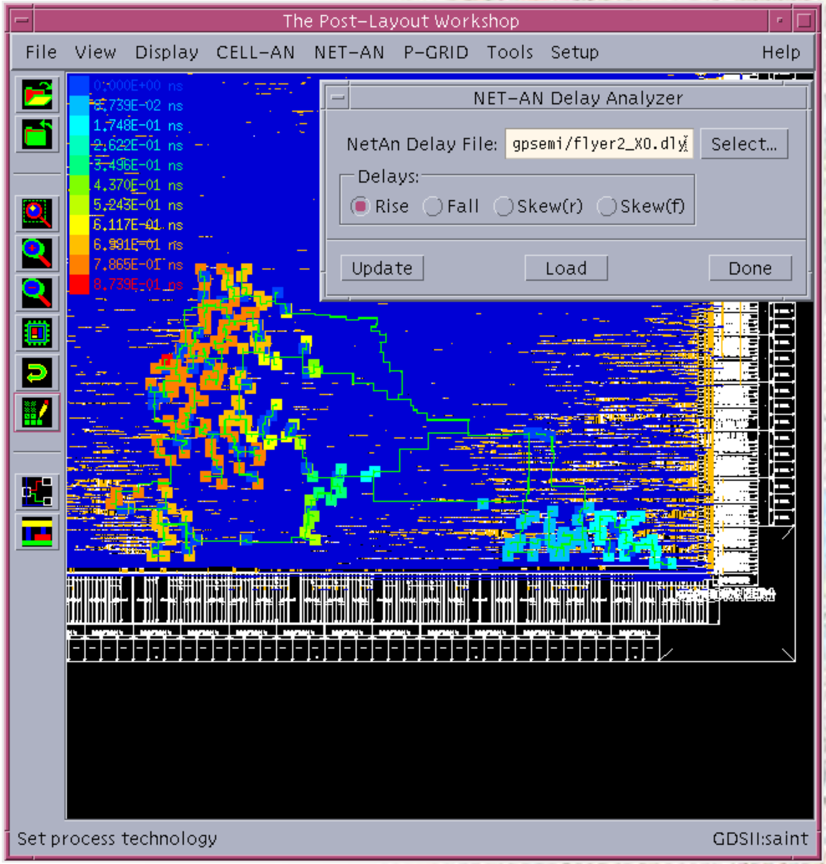
OEA International, Inc.

The Gold Standard for
Parasitic Extraction and
Signal Integrity Solutions

NET-AN
Critical Net Extraction and Analysis

- Full 3D seamless field solution
  - High accuracy extraction
  - Extracts net, tree, or entire path
  - Extracts with full net coupling
  - Outputs distributed RCLM SPICE circuit, dspf, spef, or sdf
- Easy to Use
  - Push-button hierarchical extraction
  - Graphical display of delays
  - Graphical net/cell browser
  - GDSII, P&R flow integration
  - Interactive or batch operation



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When do you need NET-AN?

- On nets that should be ‘Designed’ and not left up to the router
  - Clock Nets
  - High Speed Buses
- On nets that you know must be analyzed more closely
  - Top level clock trees
  - High speed buses
  - Critical or marginal timing paths
  - Other long and/or wide nets

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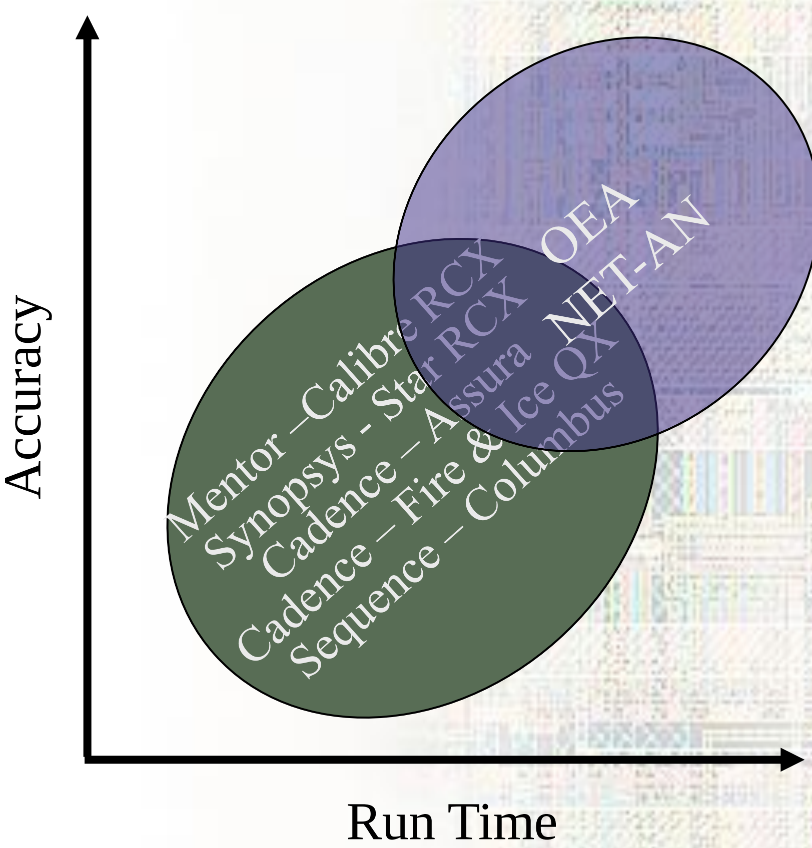
NET-AN Market Position

- **All extractors tradeoff accuracy vs. runtime!**
- **Pattern-based extraction**
  - **Significant accuracy loss at boundaries**
  - **Requires rich pattern library**
  - **Not suited for critical nets analysis**
- **Formula-based extraction**
  - **Requires process dependent parameter tuning**
  - **Accuracy of methodology limited**
  - **Most widely all-net solution**
- **Full 3D field solver (NET-AN)**
  - **Delivers more exact solution**
  - **Fits critical net analysis & design needs**



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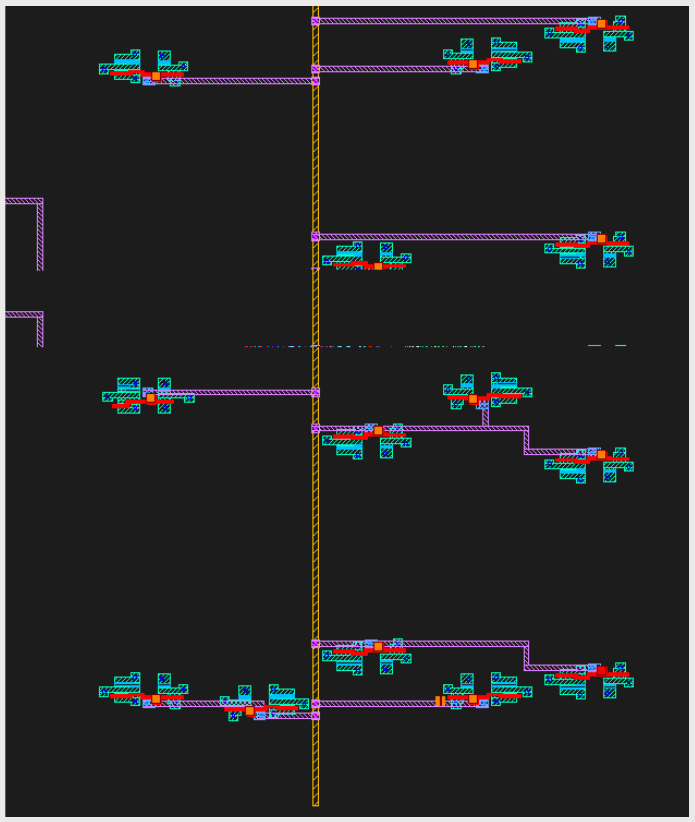
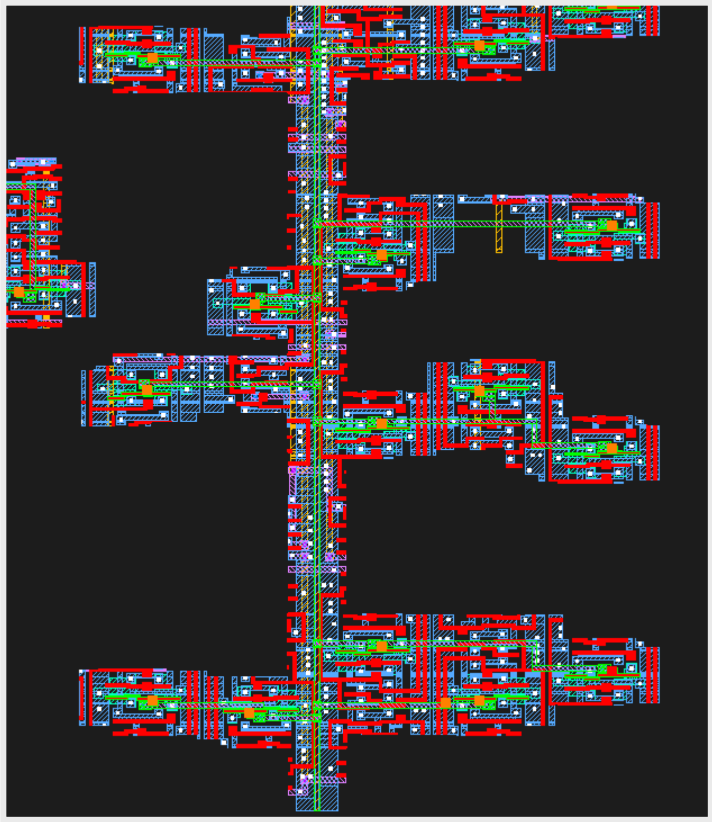
NET-AN

How it creates the 3D Model



One or more 'Target Nets' are identified in the layout. This can be through an XY,layer, net name, or GDSII Reference file.



A 3D model is created with a 'Extraction Halo' for capacitance to neighbors. Inductance coupling is determined by a minimum coupling value.

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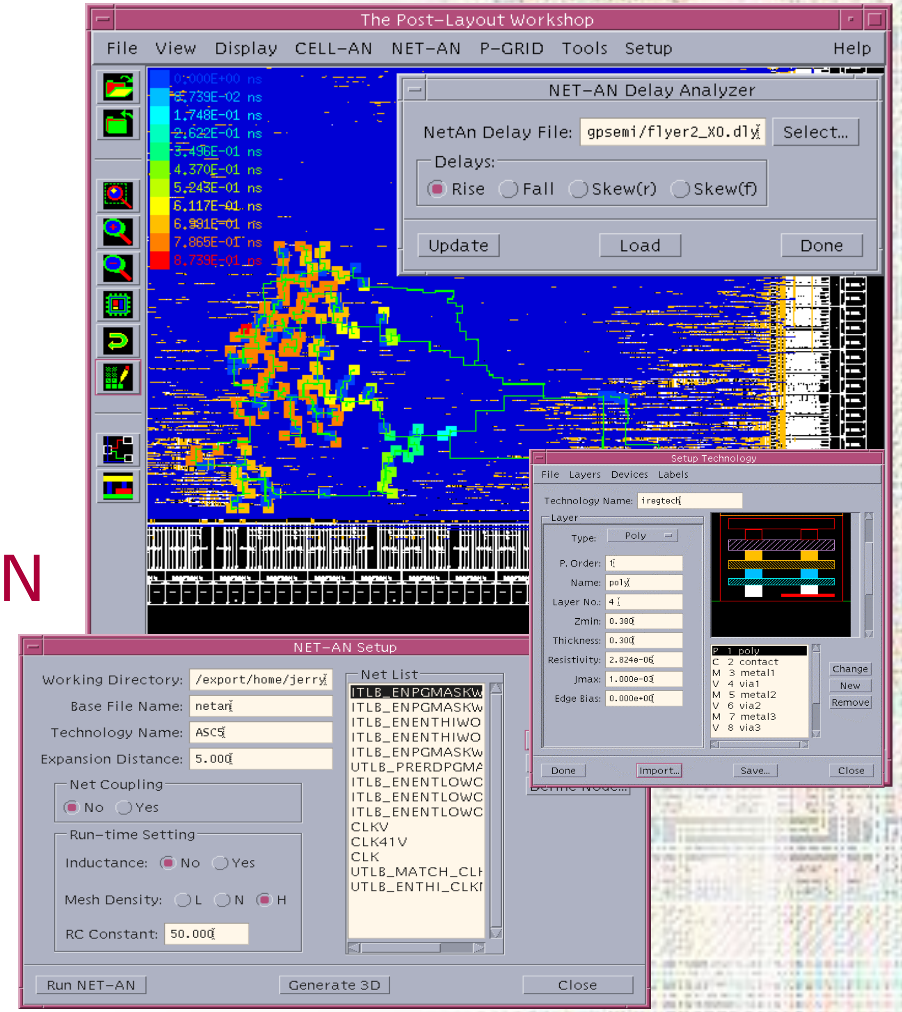
Post-Layout WorkShop (PLWS)
OEA's Graphical User Interface

- Hierarchical GDSII input
  - Creates full-chip transistor-level connectivity
- Hierarchical net browser
  - User-assigned SPICE nodes
- Builds 3D model for NET-AN
  - Includes critical nets & surrounding metal



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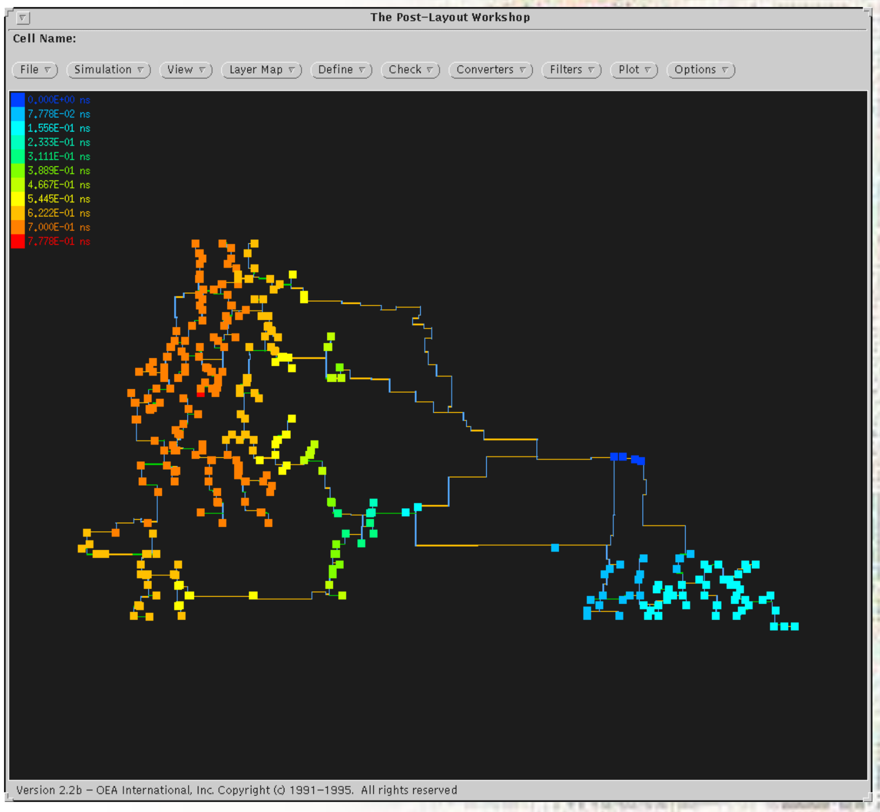
PLWS Post-Layout
Critical Path Analysis

- Context Sensitive Display
  - Color coded critical paths
- NET-AN SPICE Deck Generation
  - Compact PI-model based upon user selected RC time constant
  - No further RC reduction required!
  - Ensures fast SPICE simulations



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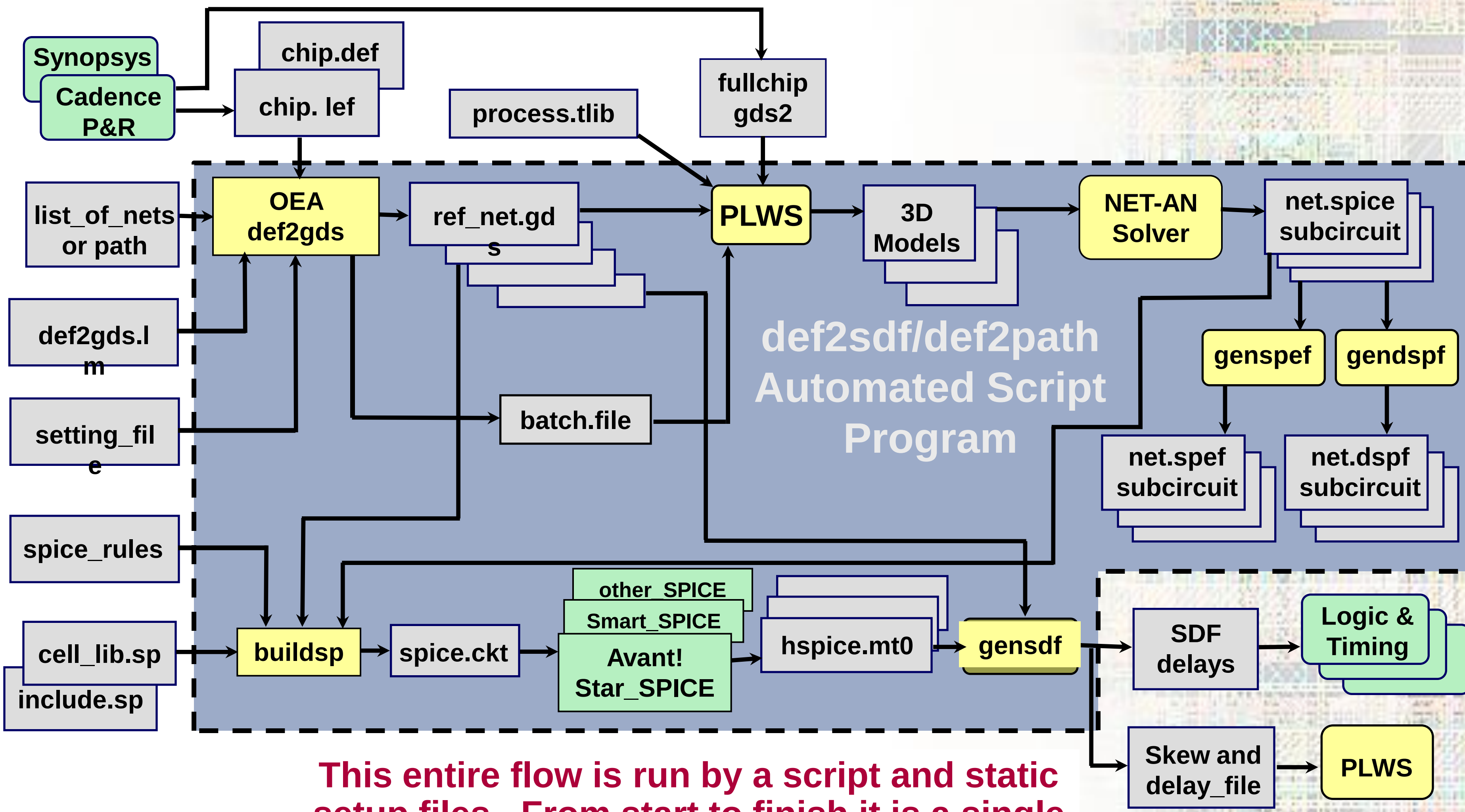
NET-AN

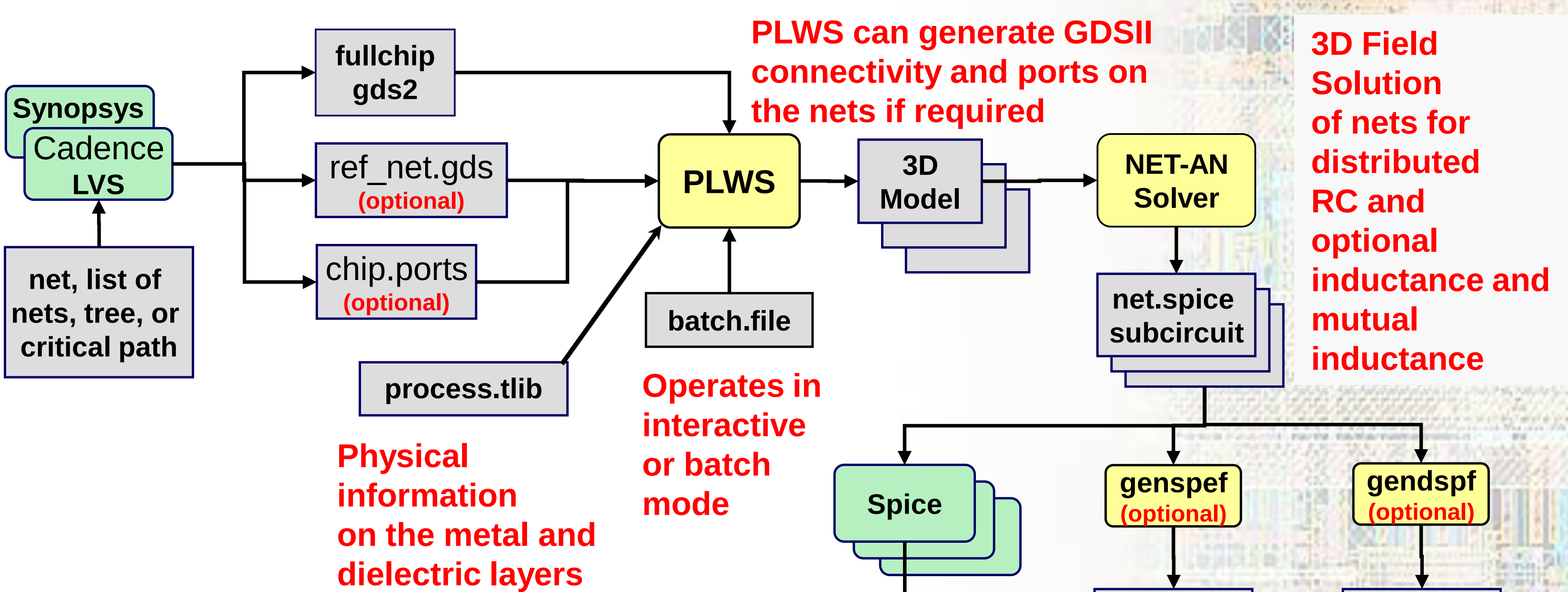
Automatic Critical Net Analysis for P&R Design Flows

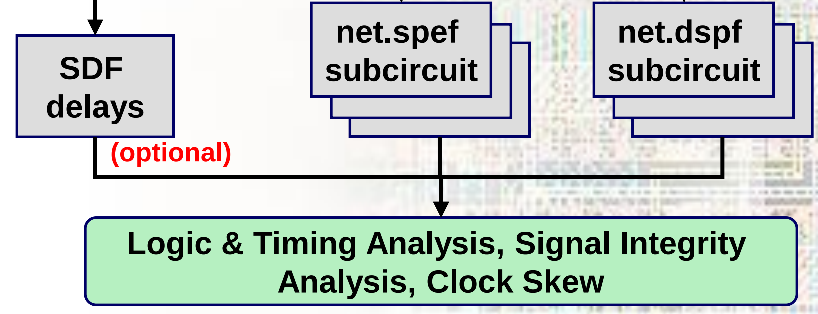


This entire flow is run by a script and static setup files. From start to finish it is a single user command.

NET-AN

Custom Design Flow





The custom design flow can be as automated or as interactive as desired for the application. Automation is made easy through a large number of flow options on input and through the use of industry standard formats.

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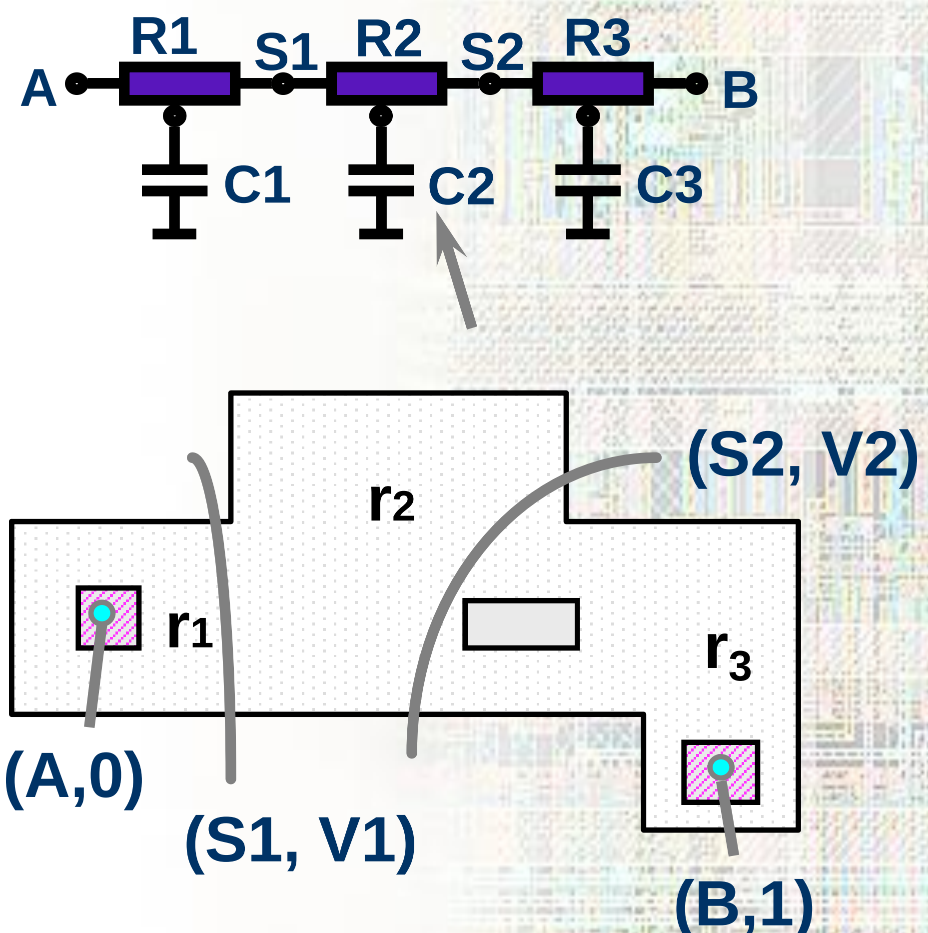
Calculating Resistance
The Right Way!

- Wrong Way
  - Square counting yields errors for irregular conductor shapes
    - No width dependent resistivity support
- Right Way
  - Find equipotential surface
  - Solve for 3D resistance and inductance integrated with capacitance

$$R = V / I$$
$$\nabla \vec{J} = 0$$
$$\vec{J} = \sigma \vec{E}$$
$$\vec{E} = -\nabla V$$
$$\nabla (\sigma \nabla V) = 0$$
$$I = \iint_S \vec{J} * \vec{ds}$$



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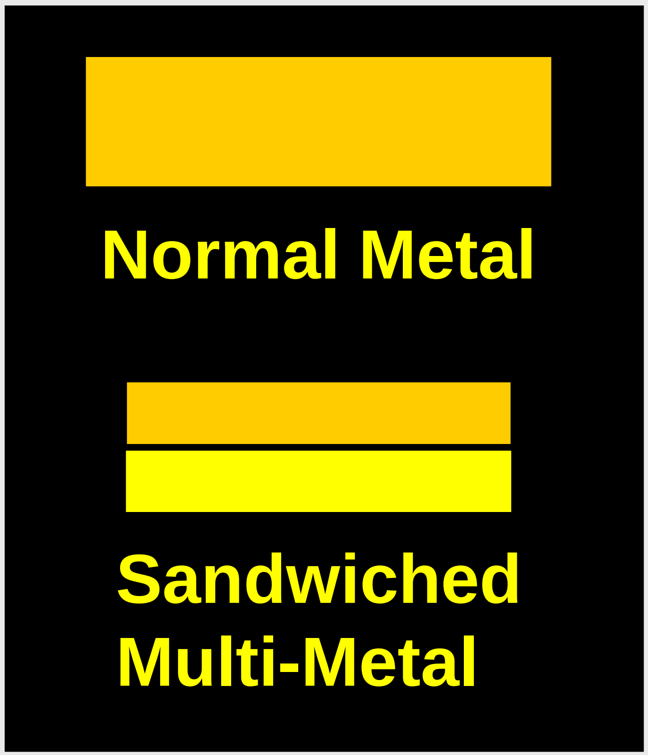
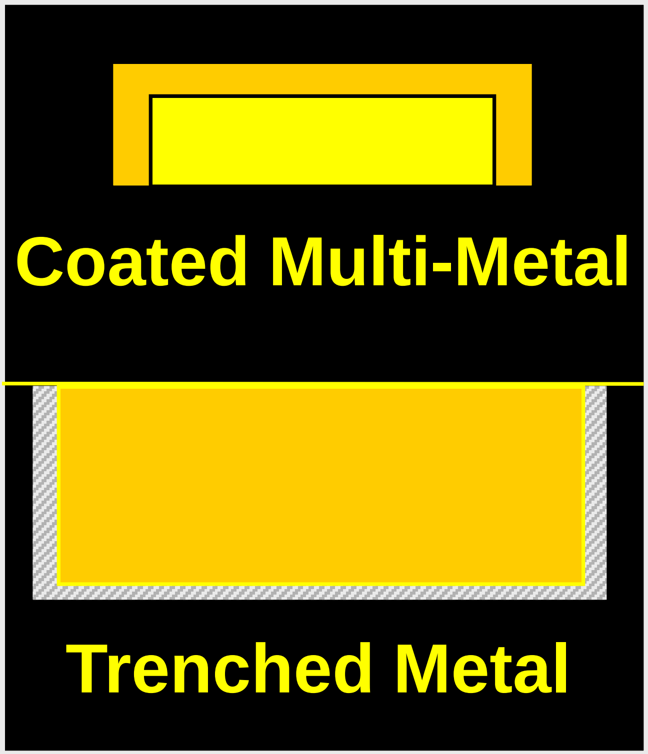
NET-AN

Width Dependent Resistivity Support





- **Coating/trench metals resistivity differ from conductor**
  - **For narrow wires, coating has proportionately larger effect**
- **Wire width sensitivities**
  - **Wider wires experience electron scattering at/near surface**
- **Mechanical polishing induces dishing of wide wires**
  - **Copper processes exceptionally susceptible**

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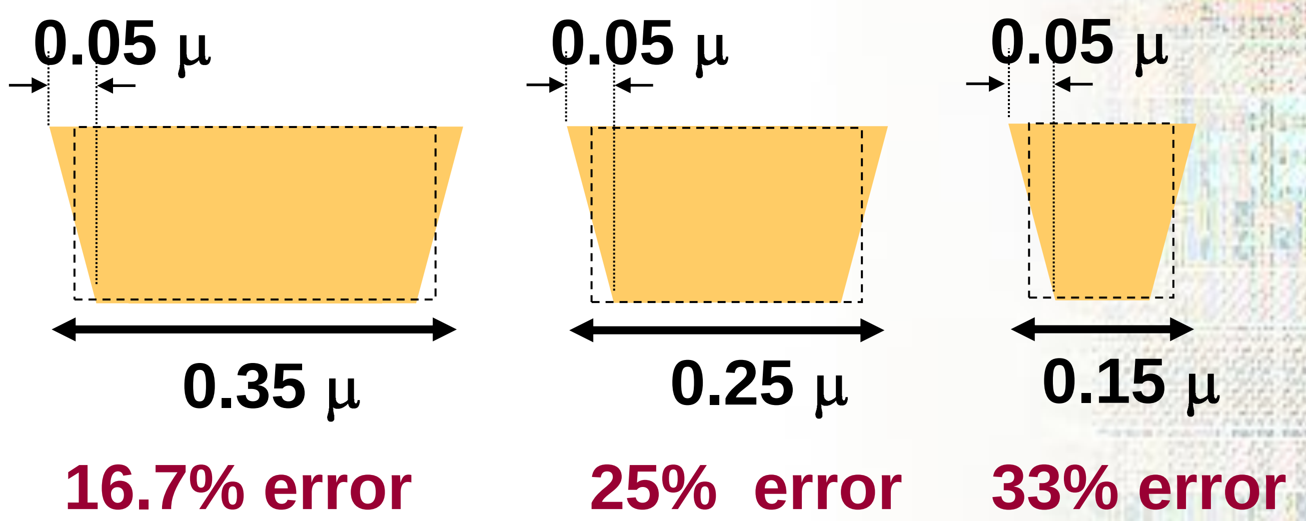
NET-AN

Layer Biasing Support



- Real wires are trapezoids!
  - Trapezoid angle varies based on metal width/spacings
  - True cross sectional area modeled correctly
  - True resistance extracted!

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NET-AN

Full 3D Net Capacitance Extraction

- Full Maxwell field solution!
  - No formula-based equations
  - No reduced order equations

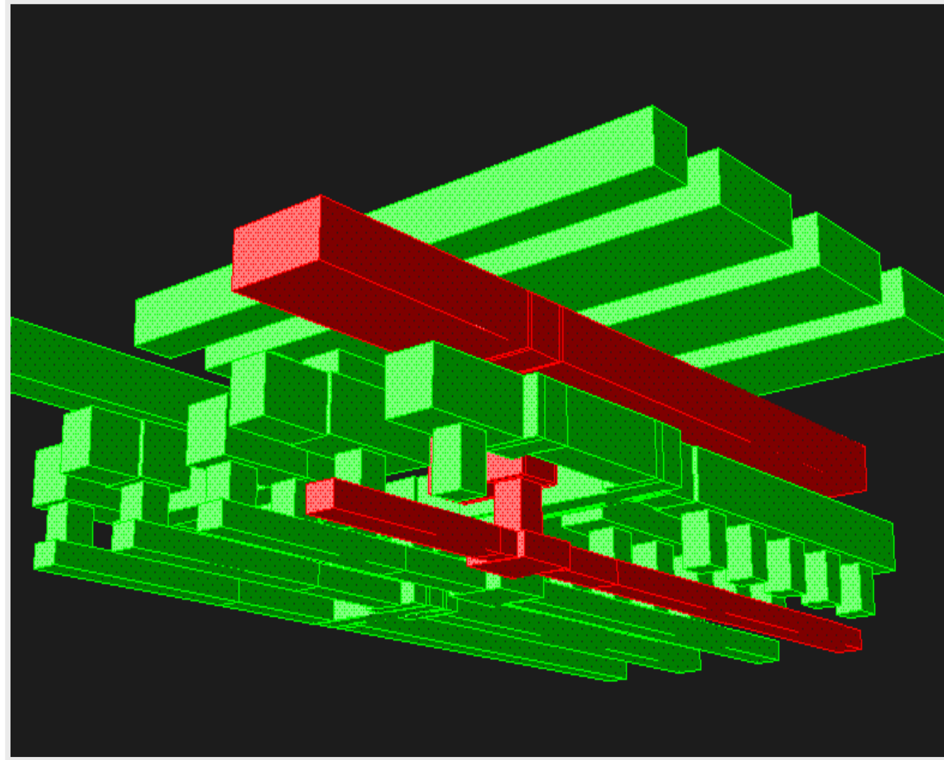
$C = Q / V$

$\vec{D} = \varepsilon \vec{E}$

$\nabla(\varepsilon \nabla V) = \rho$

$Q = \iiint_{\Omega} \rho \, dv = \oiint_{\Gamma} \vec{D} \cdot \vec{ds}$

$\vec{E} = - \nabla V$



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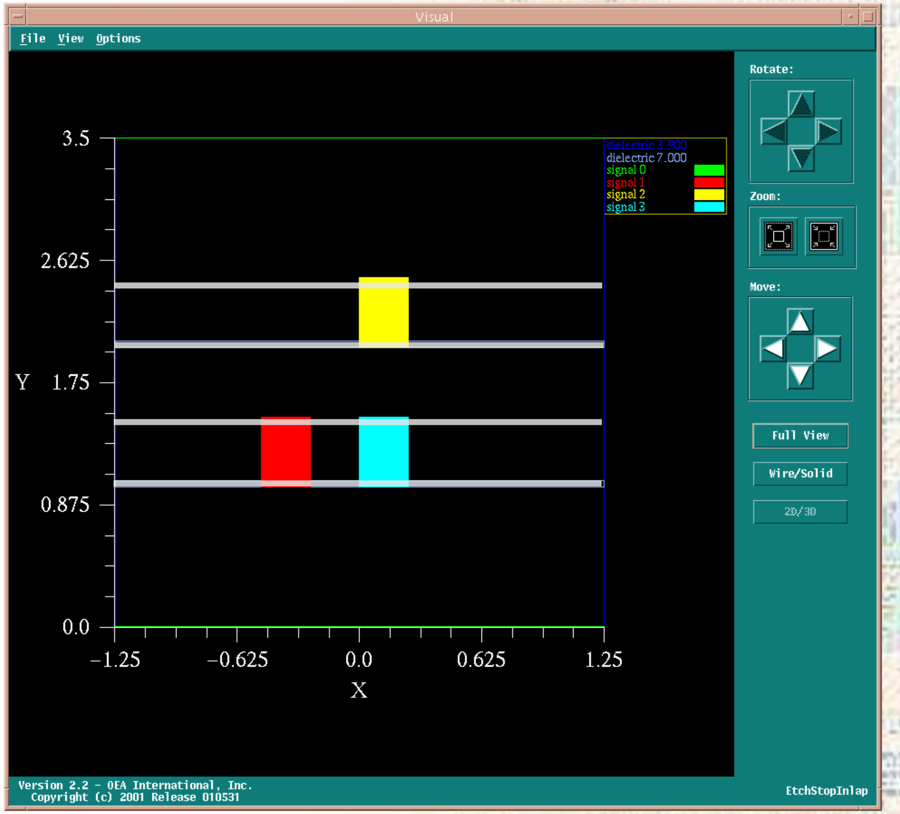
NET-An
Thin Dielectric Layer Support

- **Numerous dielectric layers**
  - **40 distinct layers not uncommon**
  - **Etch-stop layers typically ~ 100 Å**
  - **Layer stack averaging or ignoring leads to errors up to 20%**
- **True electric fields disproportionately affected**
  - **Correct capacitance extraction must include thin dielectric layers**
- **NET-AN accurately models thin dielectric layers!**



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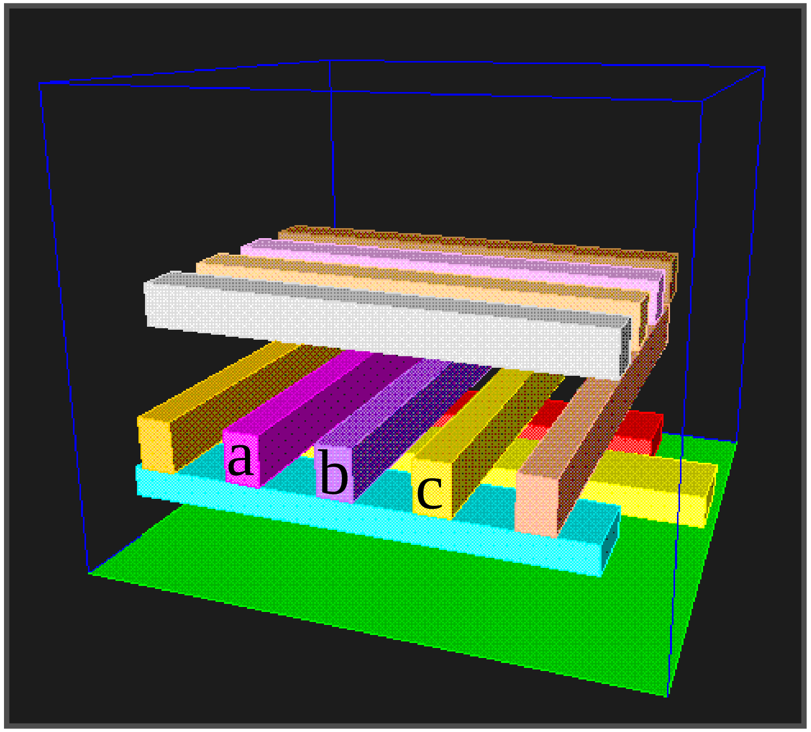
Comparing 3D Extractors
Small Test Case



Layer	OEA	Ansoft Maxwell	%Diff	Rapheal	%Diff
M2 a	2.139	2.24	5%	2.17	1%
M2 b	2.140	2.25	5%	2.16	1%
M2 c	2.139	2.24	5%	2.16	1%

Note: Only center nets are used for comparison since other nets on the simulation border are subject to different boundary condition handling between the solvers.

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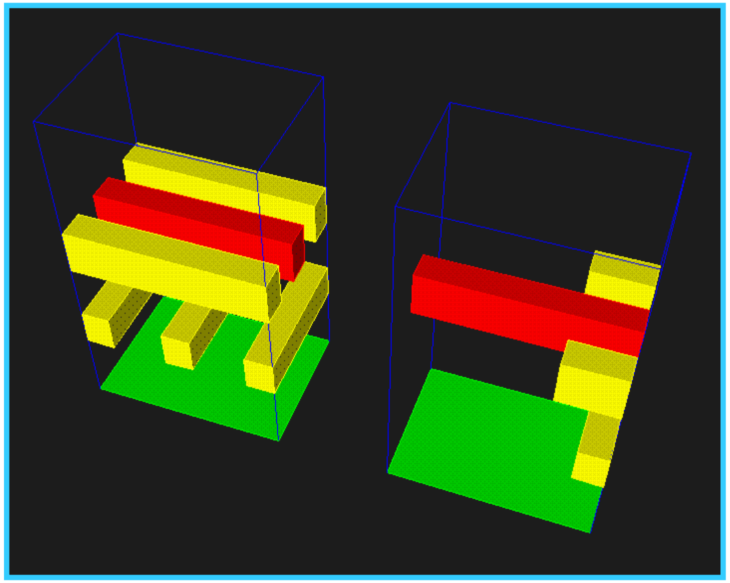
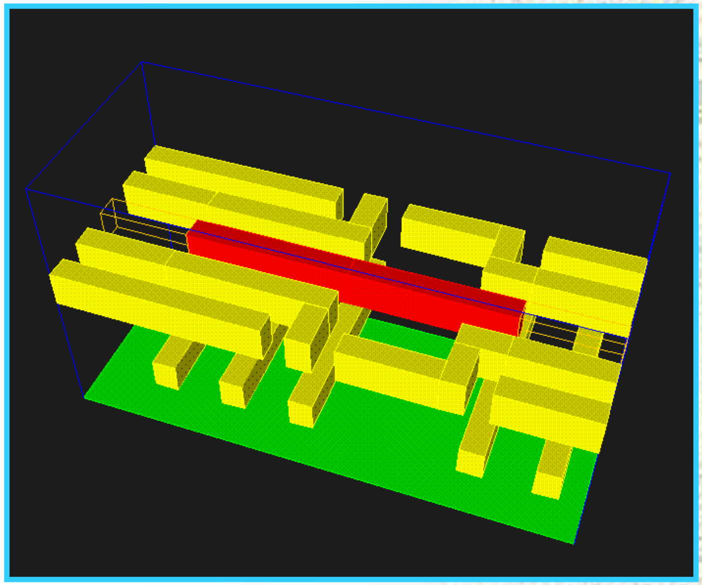
Comparing 3D Extractors

Full 3D vs. 3D Cut & Paste





Cut & Paste Method Cap (fF)				Full 3D Method	Cut & Paste Method	Full 3D Method	Cut & Paste Method
	Sect 1	Sect 2	Both	Cap (fF)	Error	Cap (fF)	Error
Window	1µ	1µ	1µ	1µ		2µ	
C11 Full	0.847	0.443	1.290	1.624	21%	1.725	25%
C12	0.847	0.400	1.247	1.603	22%	1.705	27%
C11 gnd	0.001	0.043	0.044	0.021	109%	0.020	118%

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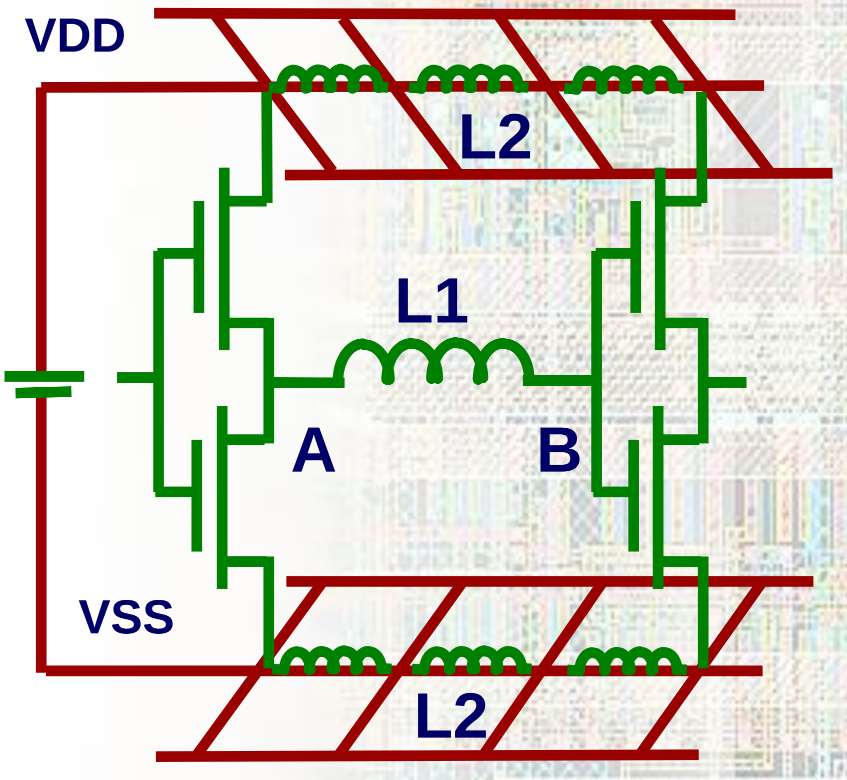
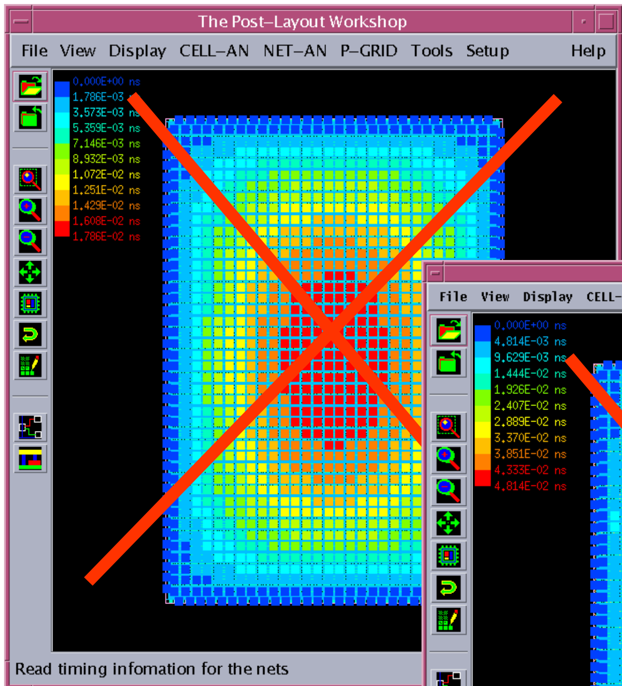
NET-AN
Inductance Support

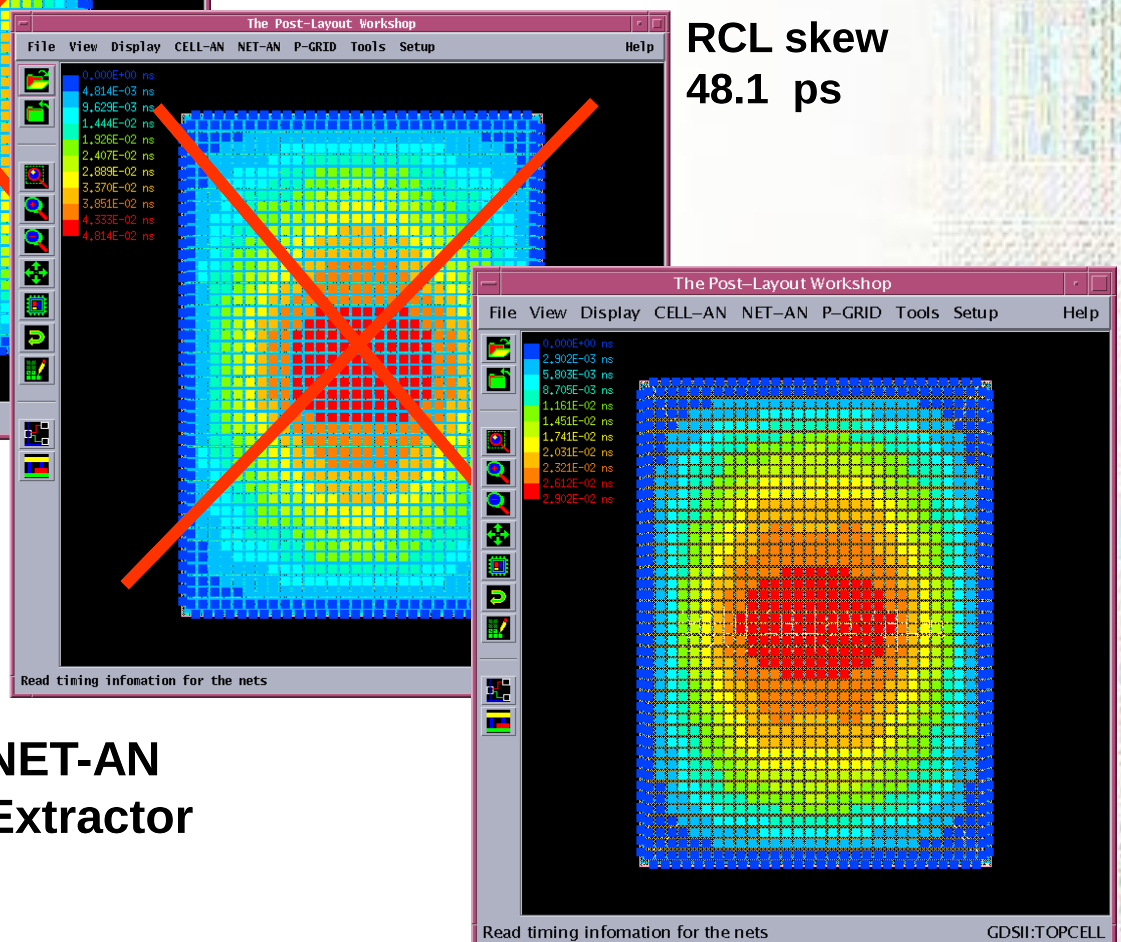
- Partial equivalent element method
  - Self-inductance
    - Low return path inductance
    - Low return path coupling
    - Effective inductance ~ line self-inductance
  - Full Self- and mutual-inductance
    - Shielded nets with known return path
    - High return path coupling
    - Full circuit simulated for highest accuracy



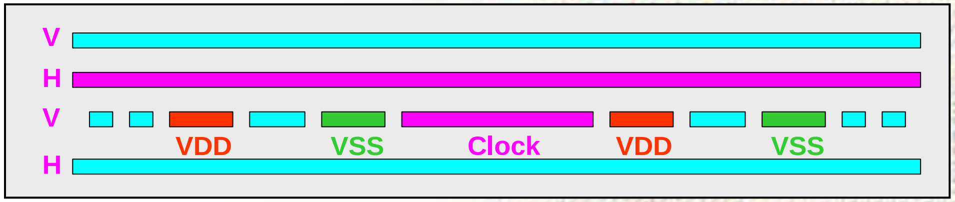
$$L_{LOOP} = L_1 + L_2 - 2\,L_{12}$$

Accurate Inductive Modeling





RC skew
17.9 ps



RCL skew
48.1 ps

RCLM skew
29.0 ps

Simulated With NET-AN
3D Field Solver Extractor

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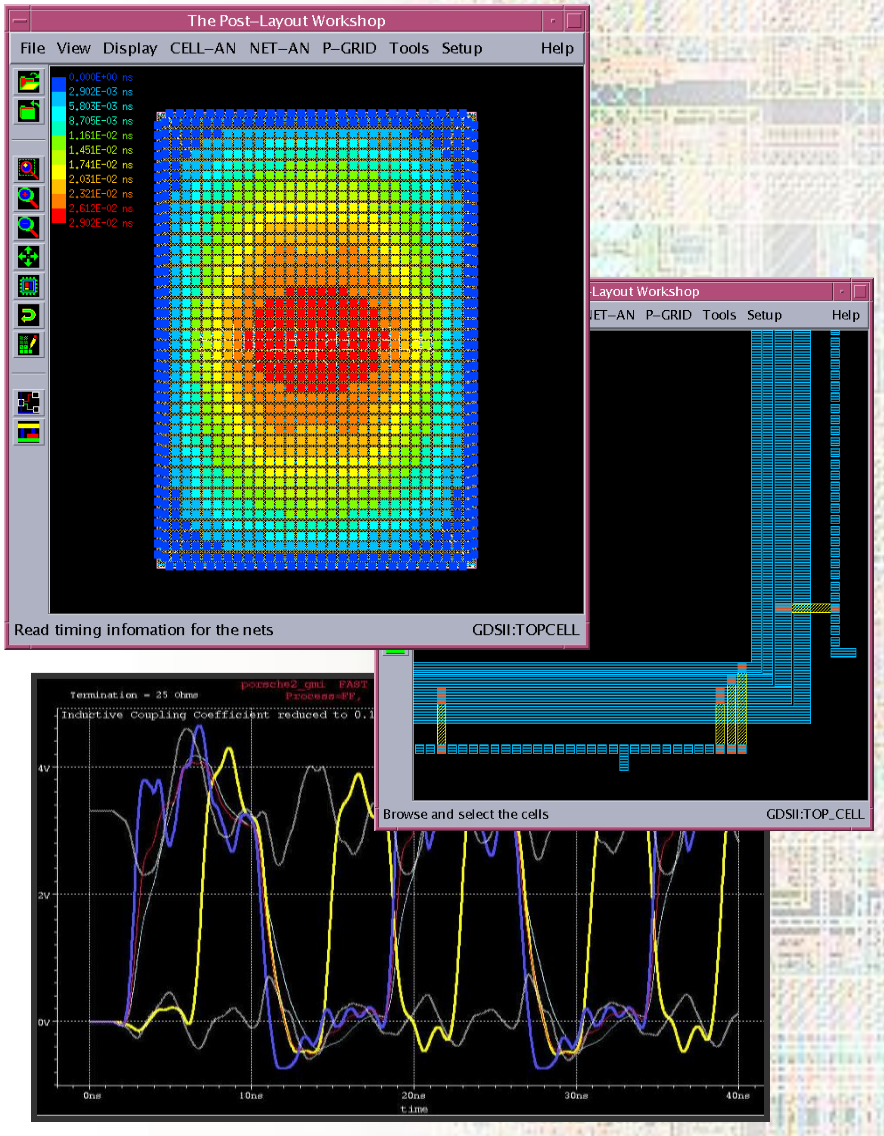
NET-AN
Extraction Engine for Other OEA Products

- CLOCK Designer™
  - 3D Clock Grid Design Planning
  - Fast Cycle Time for Quick What-if Analysis to Optimize Clock Network Width, Spacing, & Buffer Locations
- BUS-AN™
  - Interconnect Design Planning
  - 3D Bus Analysis Including Crosstalk
  - 3D Critical Path Analysis
- RING Designer™
  - IO Ring Analysis for Simultaneous Switching Noise and Ground Bounce Problems



NET-AN Summary

Defacto Industry Standard for Extraction Accuracy

- More accurate then pattern- or formula-based extractors
- Produces accurate and RLC SPICE decks
  - Width dependent resistivity
  - Full Maxwell 3D resistance and capacitance solution
  - Only solution to include inductance with return path
- Compact SPICE deck generation speeds up simulation
- Fully automated P&R flow for critical net delay analysis

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