P-GRID™

3D Power Net Analysis Design Tool

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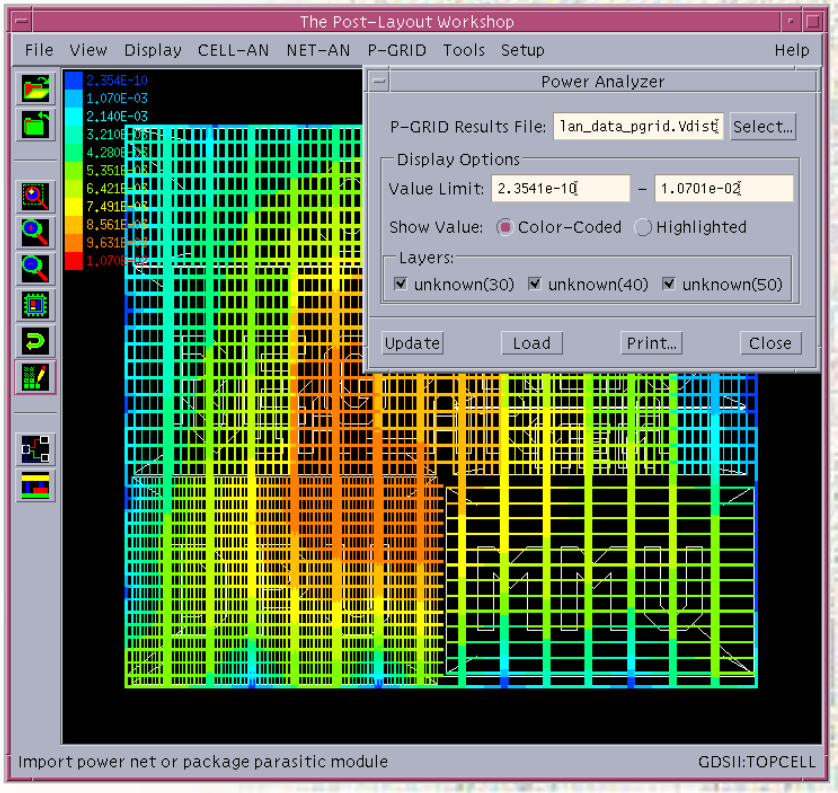
P-GRID Features

- Utilizes full 3D field simulation solver to generate high accuracy distributed network of interconnect current paths
- Flexible voltage source definition as point sources or automatically assigned at defined edges or block routing
- Flexible current source definition by area with automatic node pickup or with user specified point sources
- Graphical reporting of violations on layout for easy correction
- Color-coded mapping of current, current density and voltage drop
- Custom formatted violation reports current density and voltage drop



- Optional automatic addition of Phantom metal and vias to represent top layer routing on blocks
- Push-button graphic interface or batch operation

Built-in Utility to Easily Preprocess of Library to Get Cell Currents

.SUBCKT and2
.SUBCKT ram1
.SUBCKT ….

ASIC or Custom Lib

Automatically links in and runs Spice to get currents

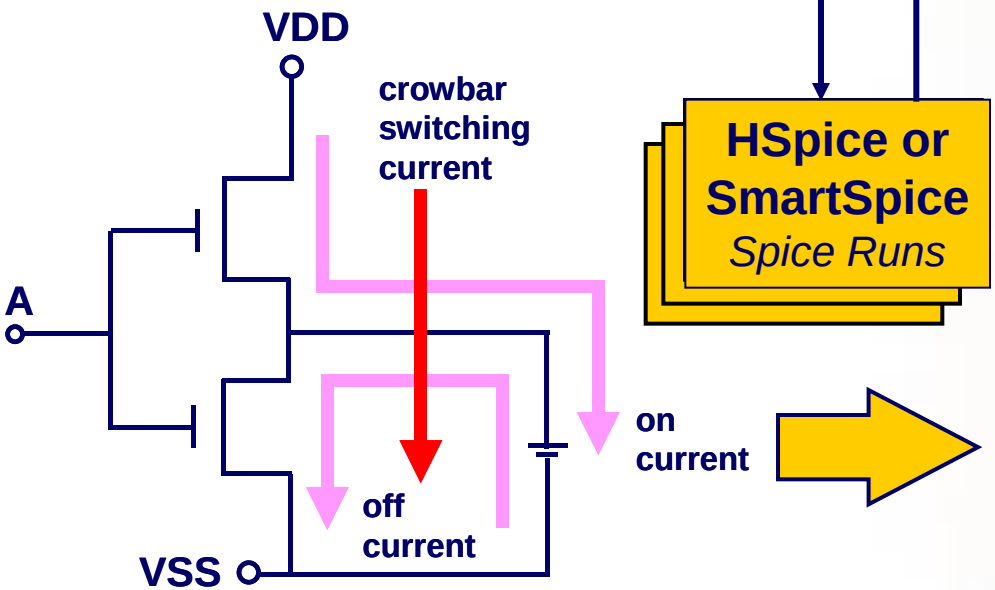
and2 current
ram1 current
AVE VDD
PEAK VDD
RMS VDD
AVE VSS
PEAK VSS
RMS VSS

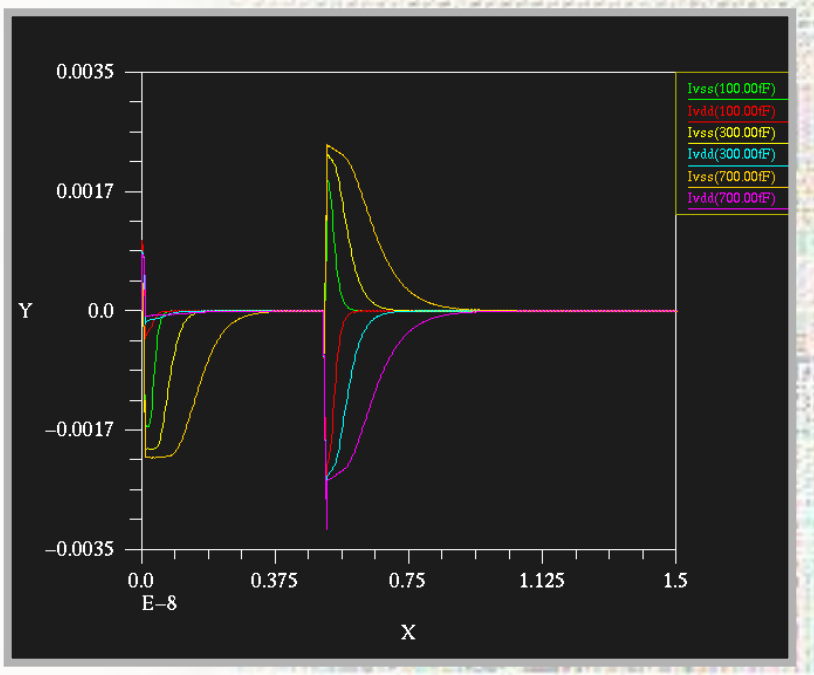
Cell def File

cellcc

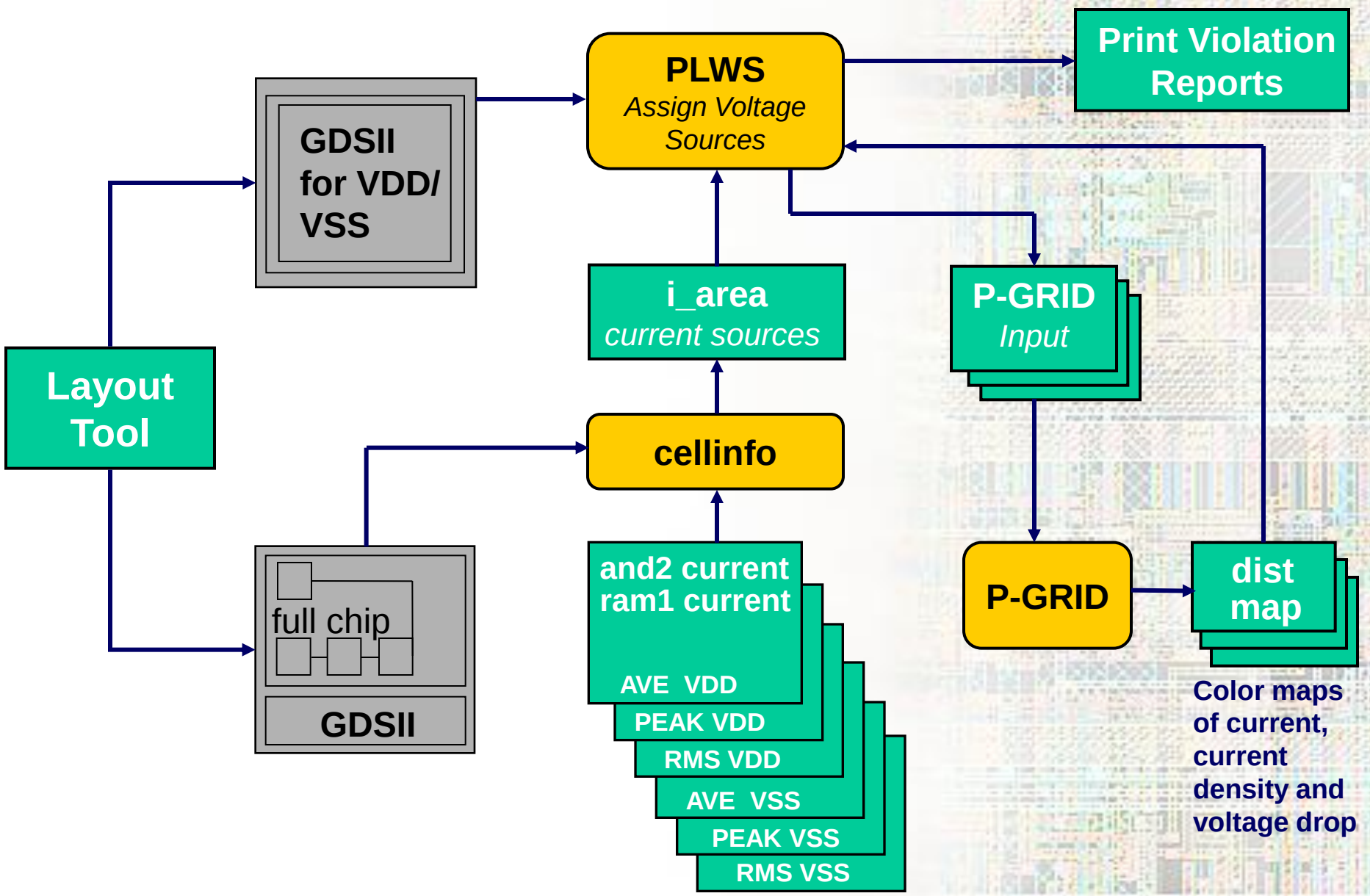
Rules File

HSpice or SmartSpice
Spice Runs





P-GRID Flow

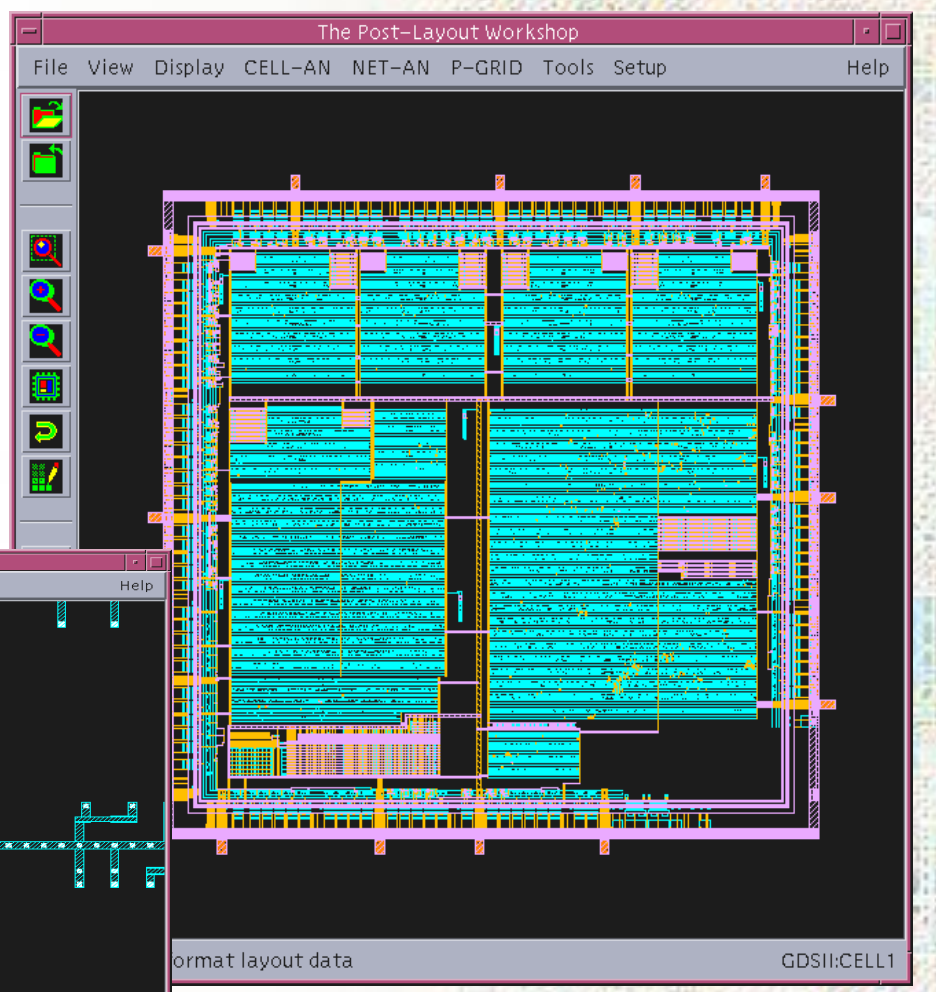

PLWS
Assign Voltage Sources
Print Violation Reports
GDSII for VDD/ VSS
i_area
current sources
P-GRID
Input
Layout Tool
cellinfo
full chip
GDSII
and2 current
ram1 current
AVE VDD
PEAK VDD
RMS VDD
AVE VSS
PEAK VSS
RMS VSS
P-GRID
dist map
Color maps of current, current density and voltage drop

Walkthrough of VDD Static Power Net Analysis

1 million gate ASIC design

Over 800,000 current sources

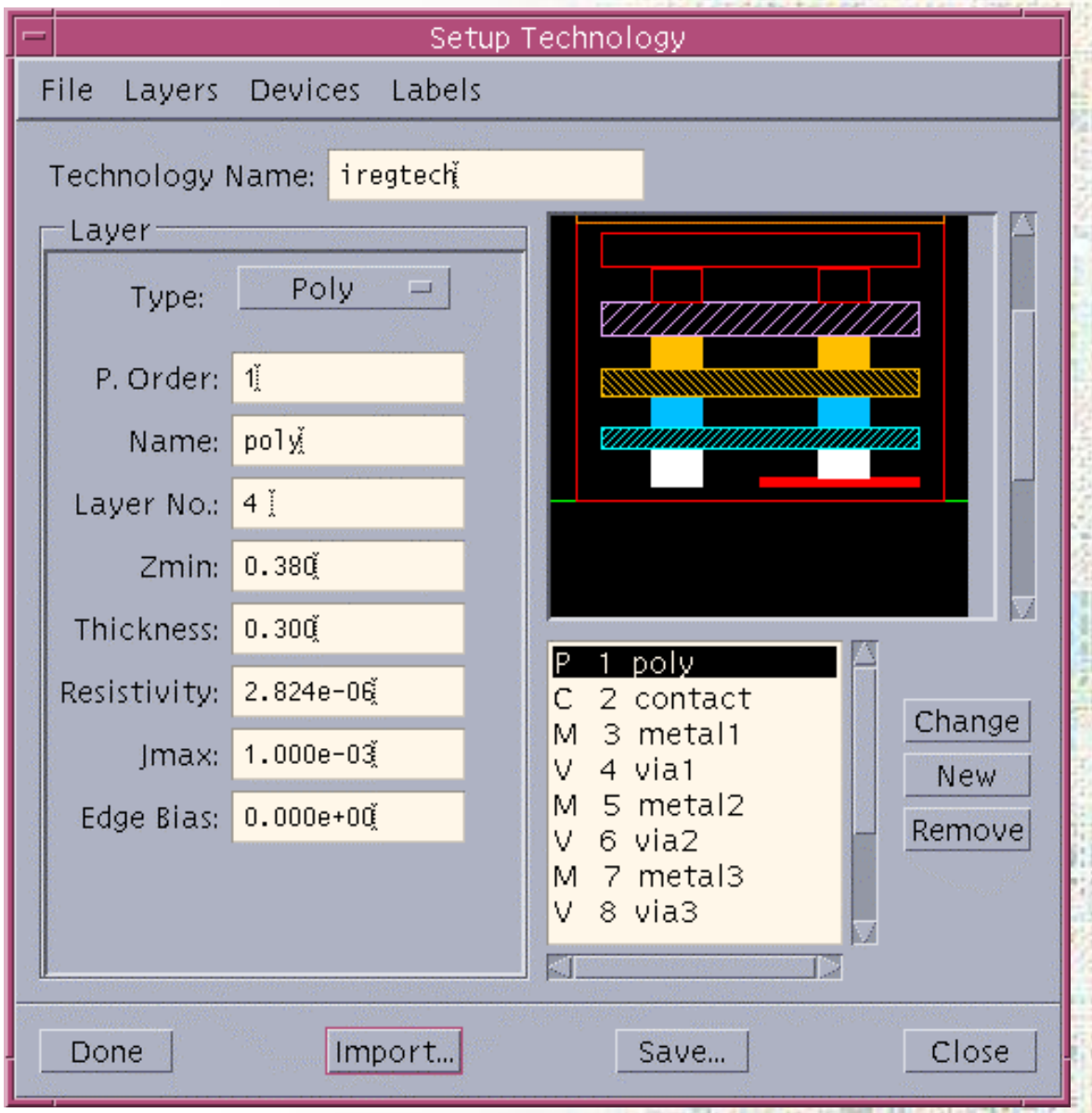
Approx 46 min. Total – extraction and simulation of currents



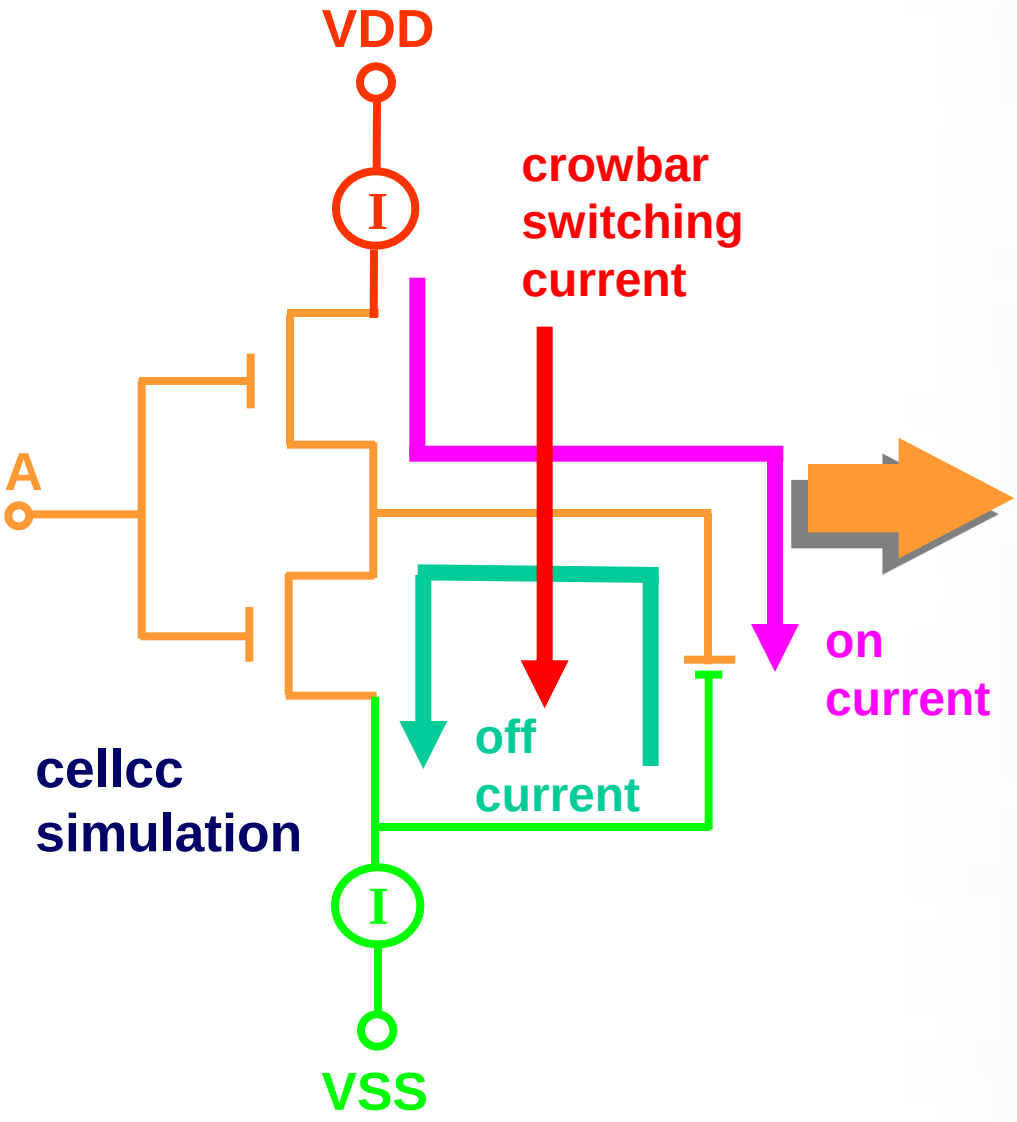
VSS & VDD Net GDSII is generated down to contacts

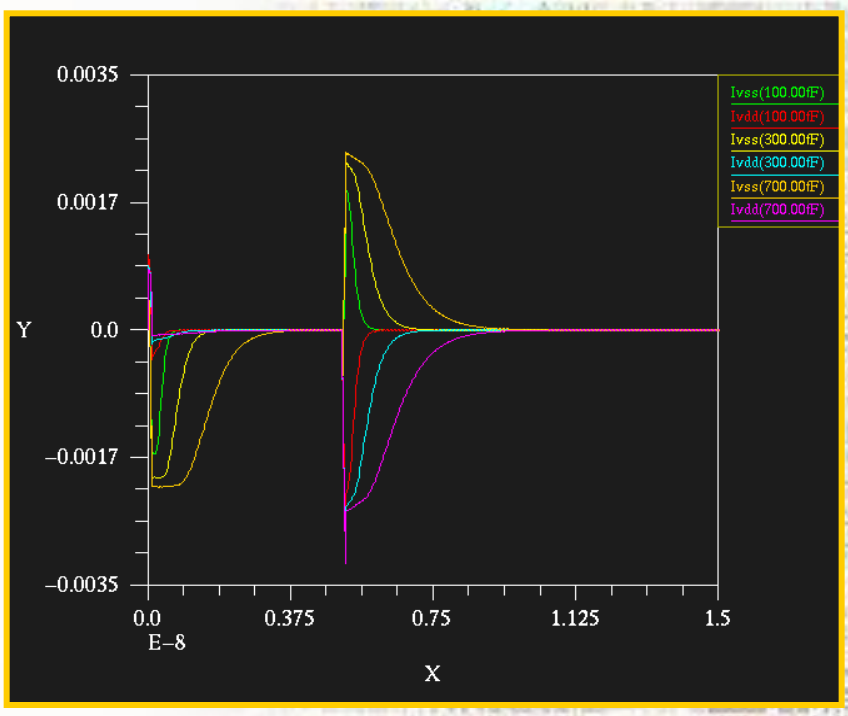
Technology File Setup

- Fast interactive setup
- Easy to enter from process data
- Handles local interconnect, multi-dielectrics, composite metal layers
- Definitions down to transistor contacts



Currents of Switching Gates are Monitored



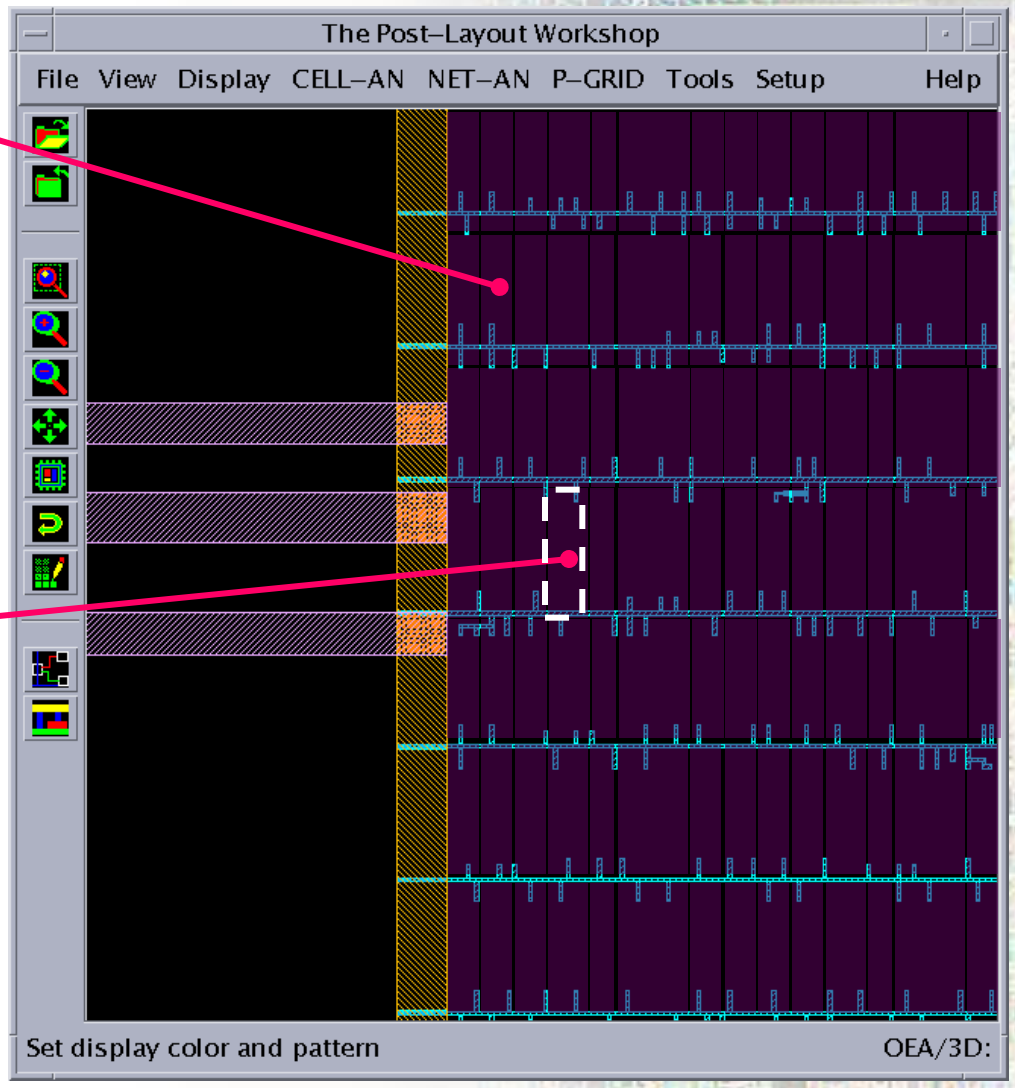


Cells are simulated in Spice and VDD and VSS average, peak, and RMS currents are saved.

Current Sources Are Assigned to Cell Locations

Each gate in the library is pre-characterized and assigned current usages for Ave, Peak and RMS
(i.e. OEA cellcc program)

Gate locations are automatically extracted from full layout.
(i.e. OEA cellinfo program)

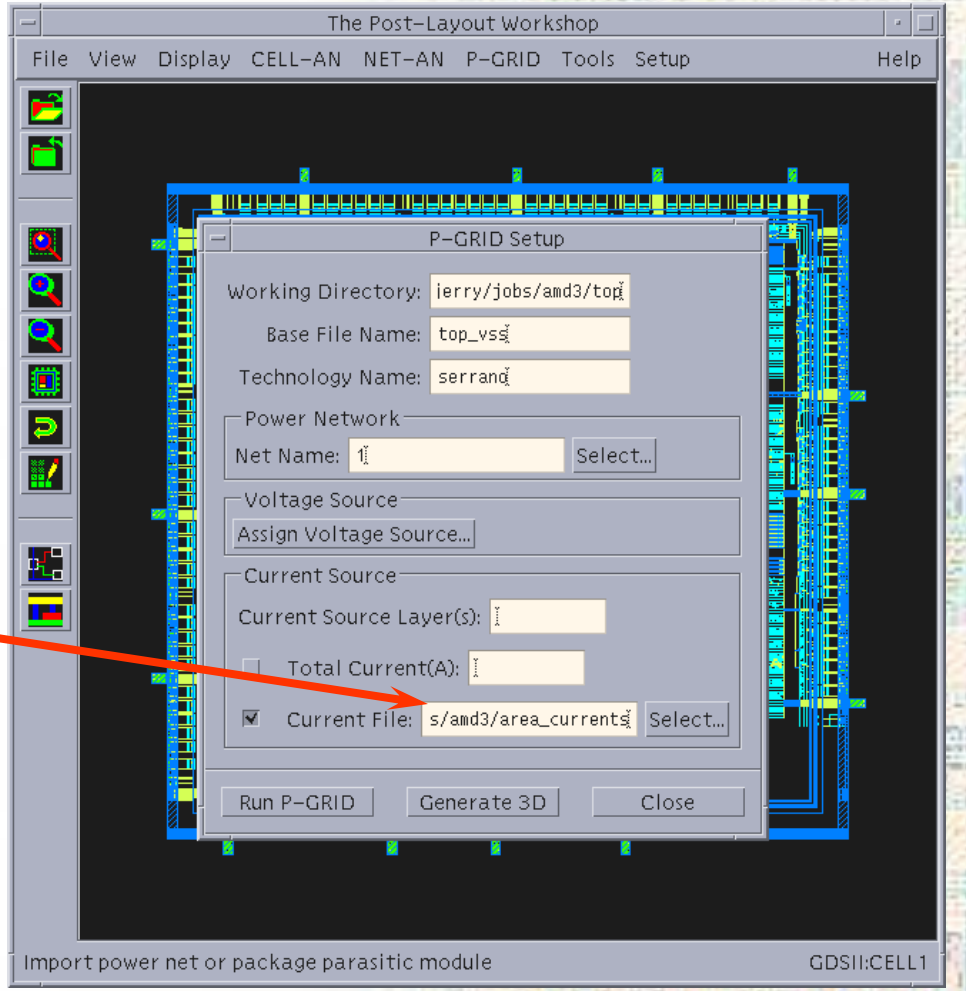


Setting Up Current Sources by Area

- Areas are automatically extracted from full layout
- Areas can be cells, blocks, full chip or any combination
- A utility is provided to automatically assign current to extracted cell boundaries

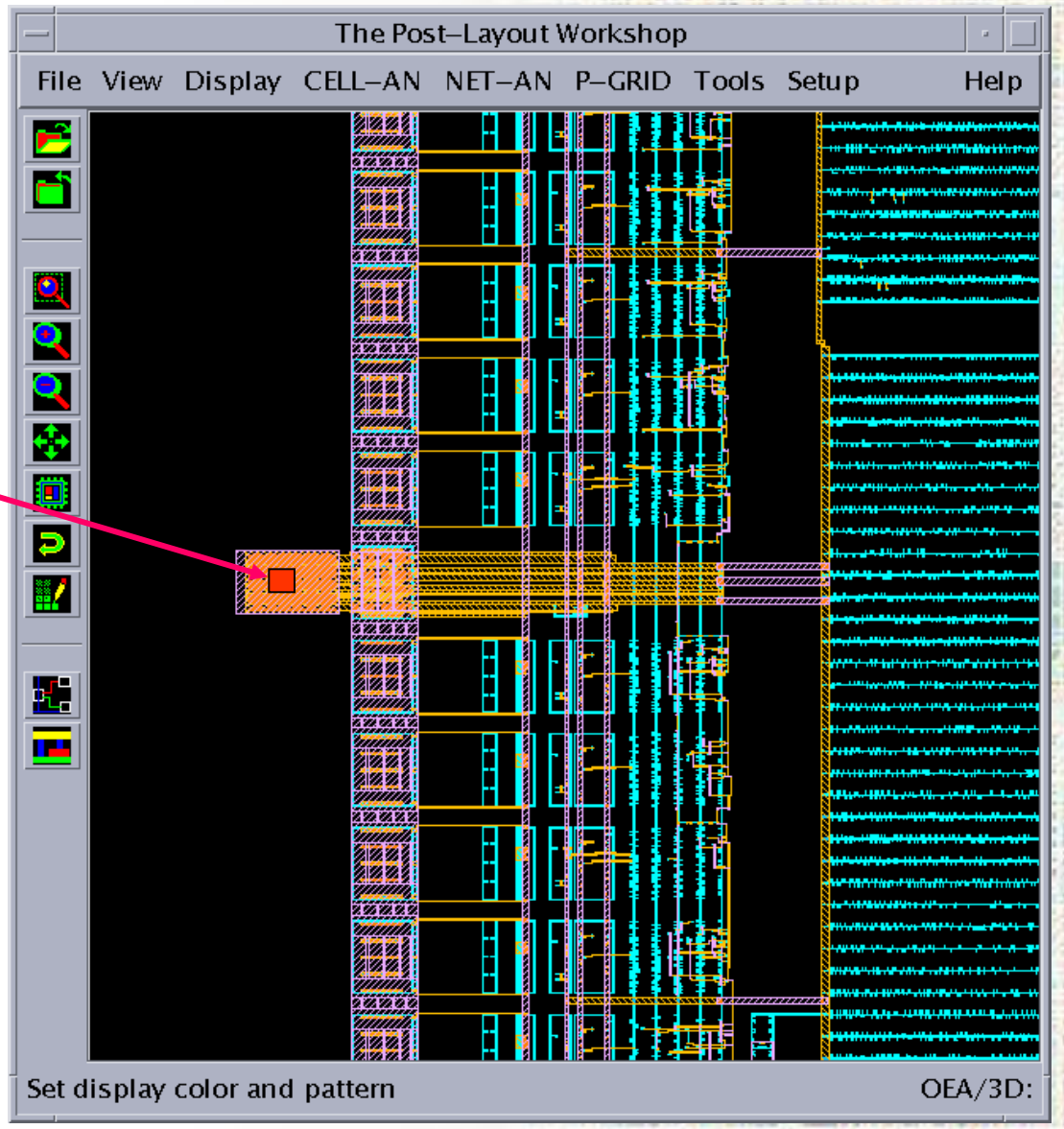
User Provided Block Currents

```
15
   100.00    670.00    400.00   5100.00 0.011    LEFT
   450.00   5400.00     50.00    550.00 0.011    BOTTOM
   450.00   5400.00   4950.00   5450.00 0.011    TOP
  5150.00   5700.00   1000.00   5100.00 0.011    RIGHT
   670.00   1770.00   3750.00   4950.00 0.0183   HDLC_D
  1770.00   2880.00   3750.00   4950.00 0.0183   HDLC_C
  2880.00   4050.00   3750.00   4950.00 0.0183   HDLC_B
  4050.00   5150.00   3750.00   4950.00 0.0183   HDLC_A
   670.00   1290.00   3070.00   3750.00 0.0111   HS_UART
  1290.00   2750.00   3070.00   3750.00 0.0038   UART
   670.00   2750.00   1170.00   3070.00 0.0577   DMA
   670.00   2750.00    550.00   1170.00 0.020    186_?
  2750.00   5150.00   2800.00   3750.00 0.0305   MIB
  2750.00   5150.00   1050.00   2800.00 0.065    USB
  2750.00   3670.00    550.00   1050.00 0.0047   LTB
```



Voltage Sources Are Assigned to Bondwire Locations

Locations for all of the voltage sources are placed where the bondwire will attach to the top level metal.



Extract and Simulate Current Flow

Net GDSII

Cell Current Sources

Voltage Sources

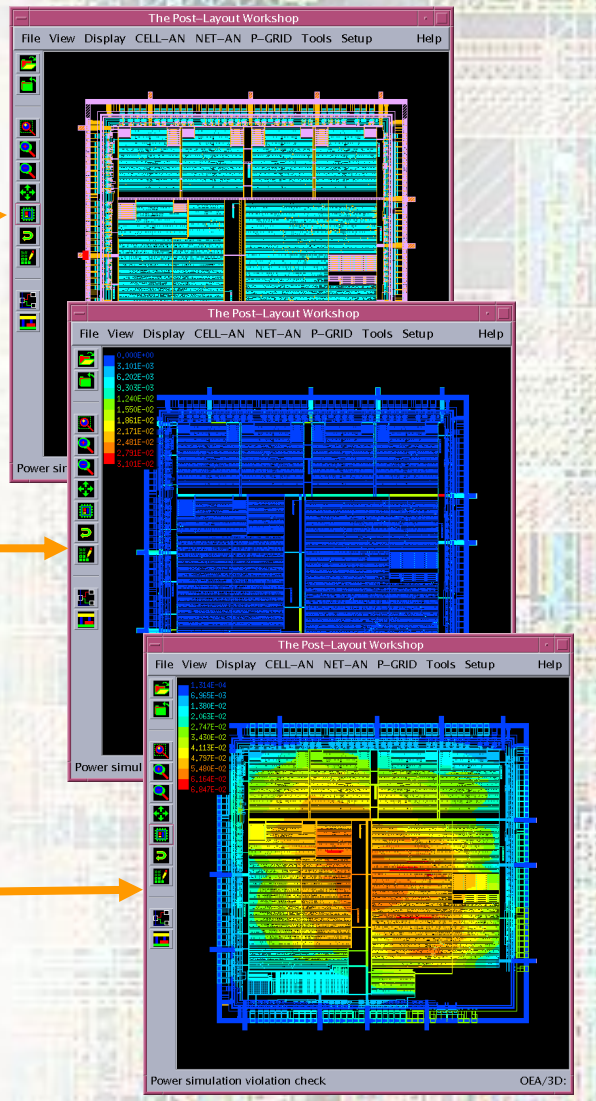
Process Technology

Build 3D Model (OEA PLWS)

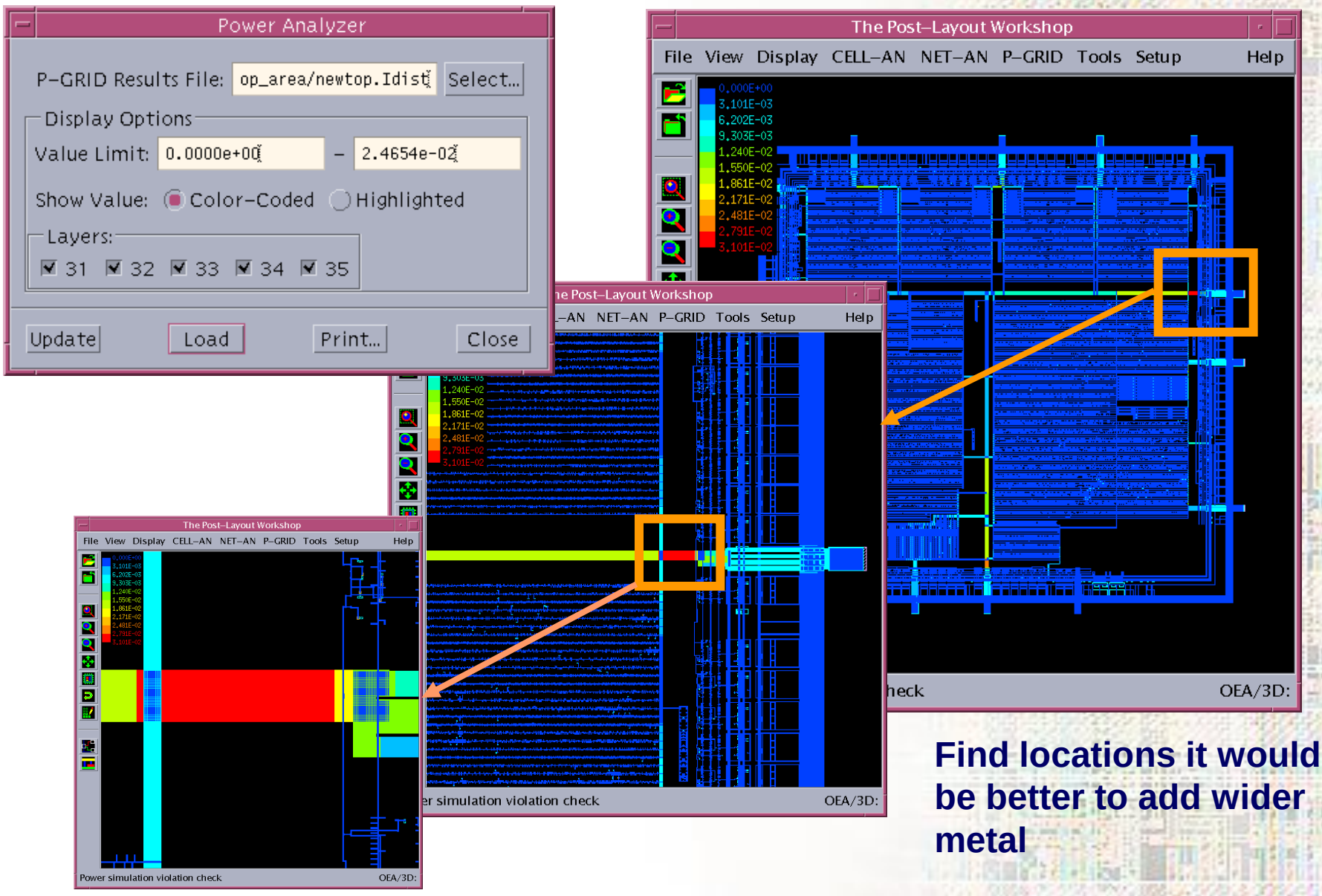
Simulation Input Files

Extract and Simulate (OEA P-GRID)

Output Files



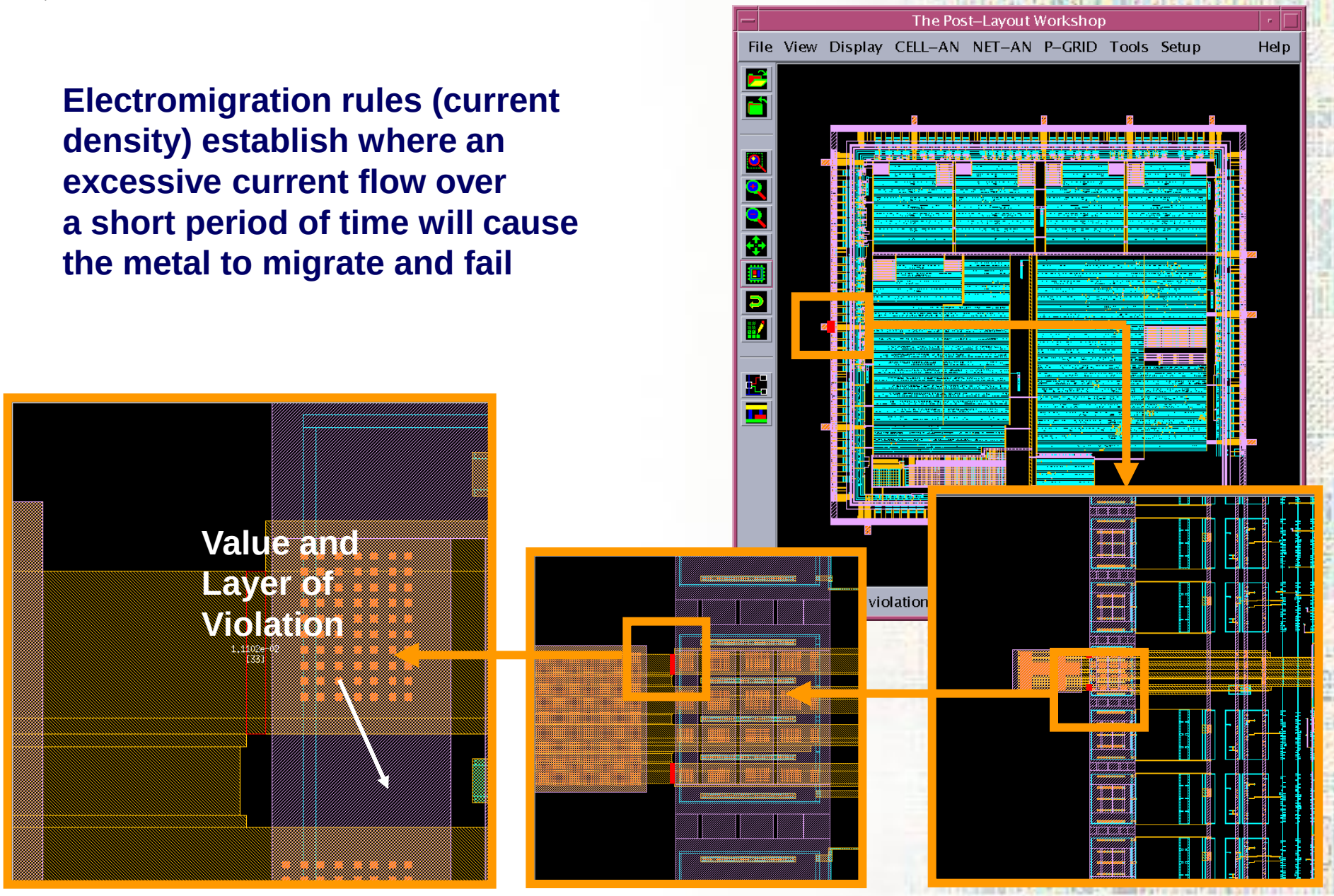
Review Current Distribution in Interconnect



Find locations it would be better to add wider metal

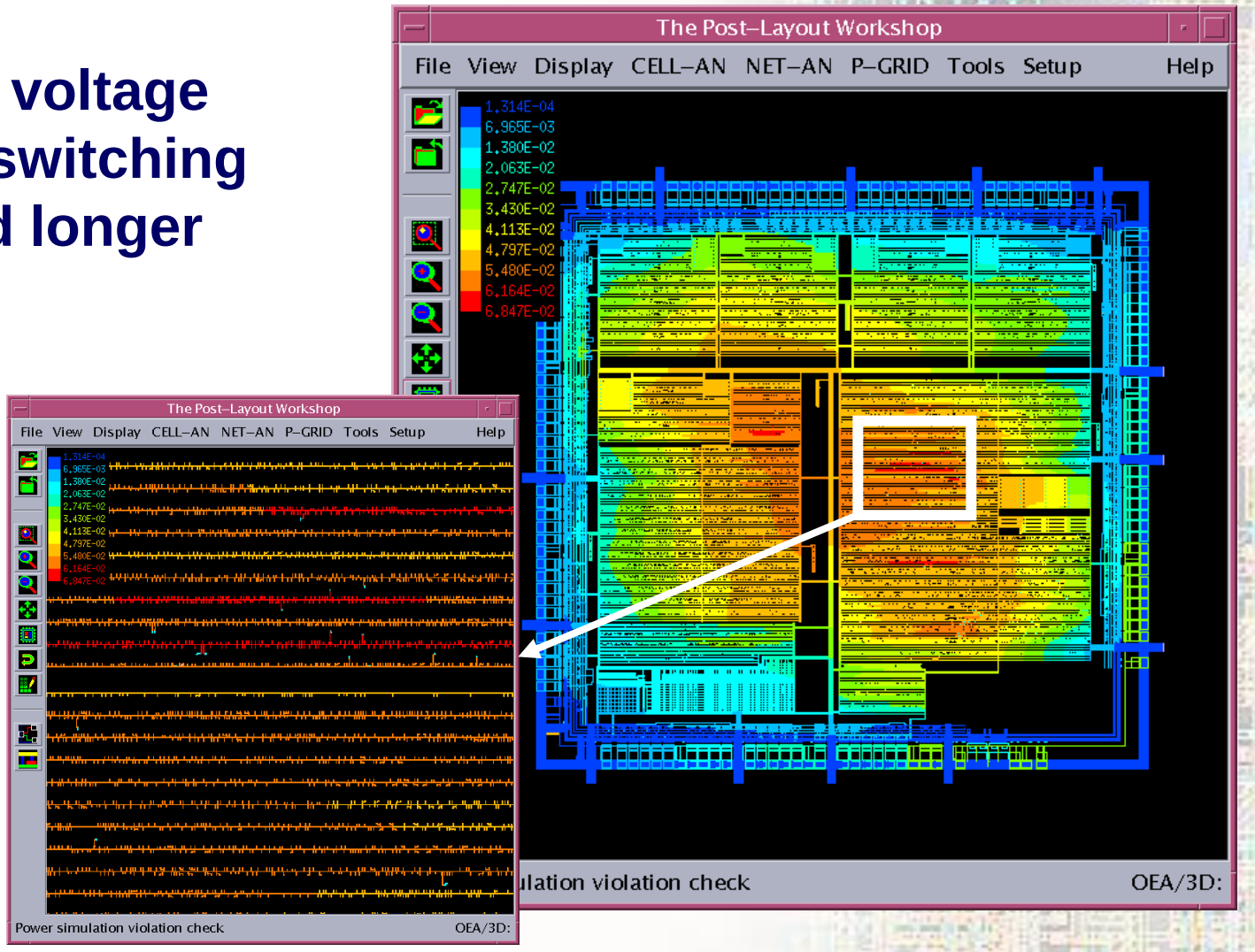
Find Any Current Density Violations

Electromigration rules (current density) establish where an excessive current flow over a short period of time will cause the metal to migrate and fail



Assure Voltage Levels Against Maximum IR Drop Specifications

Inadequate voltage can cause switching failures and longer delays



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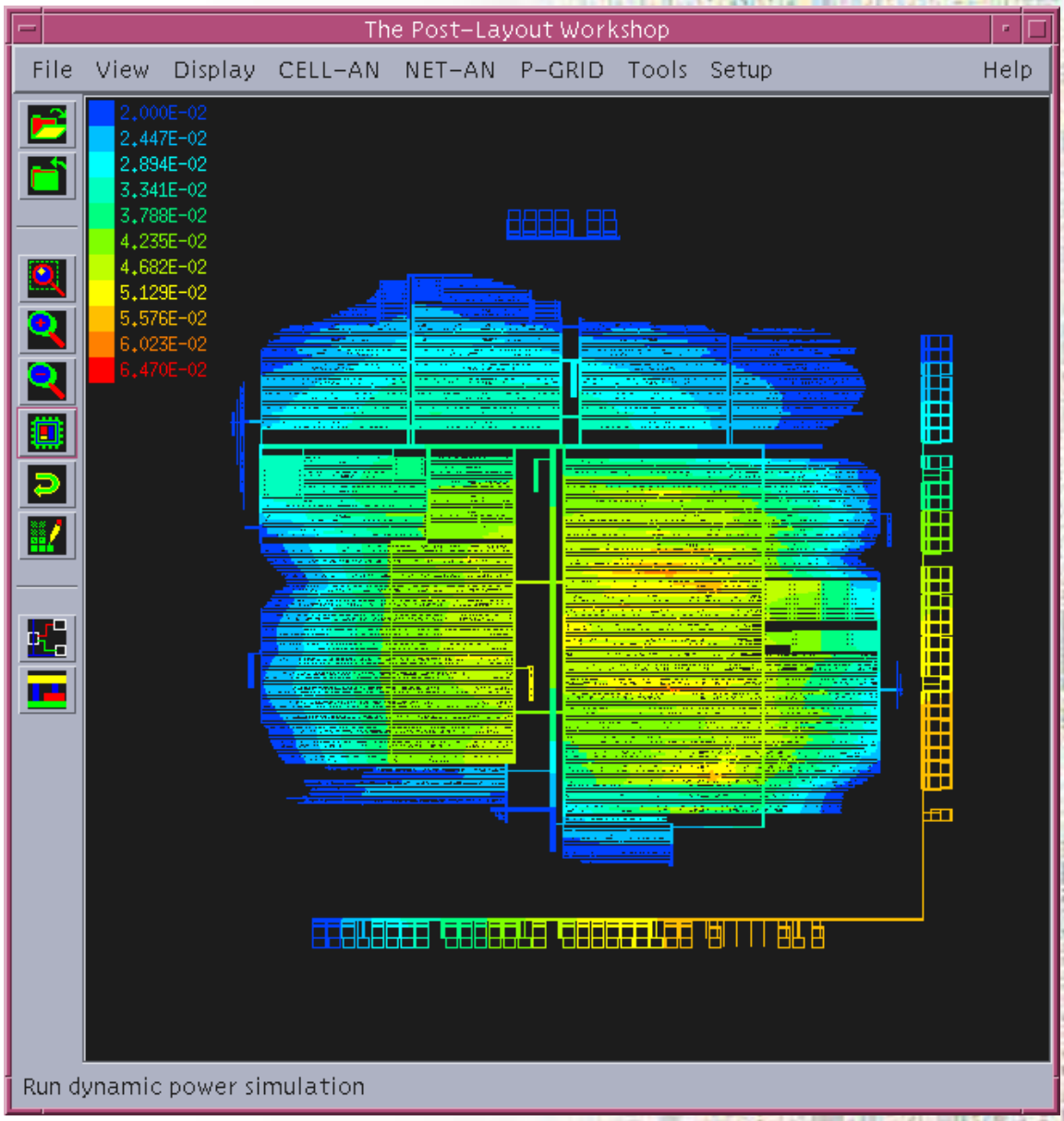
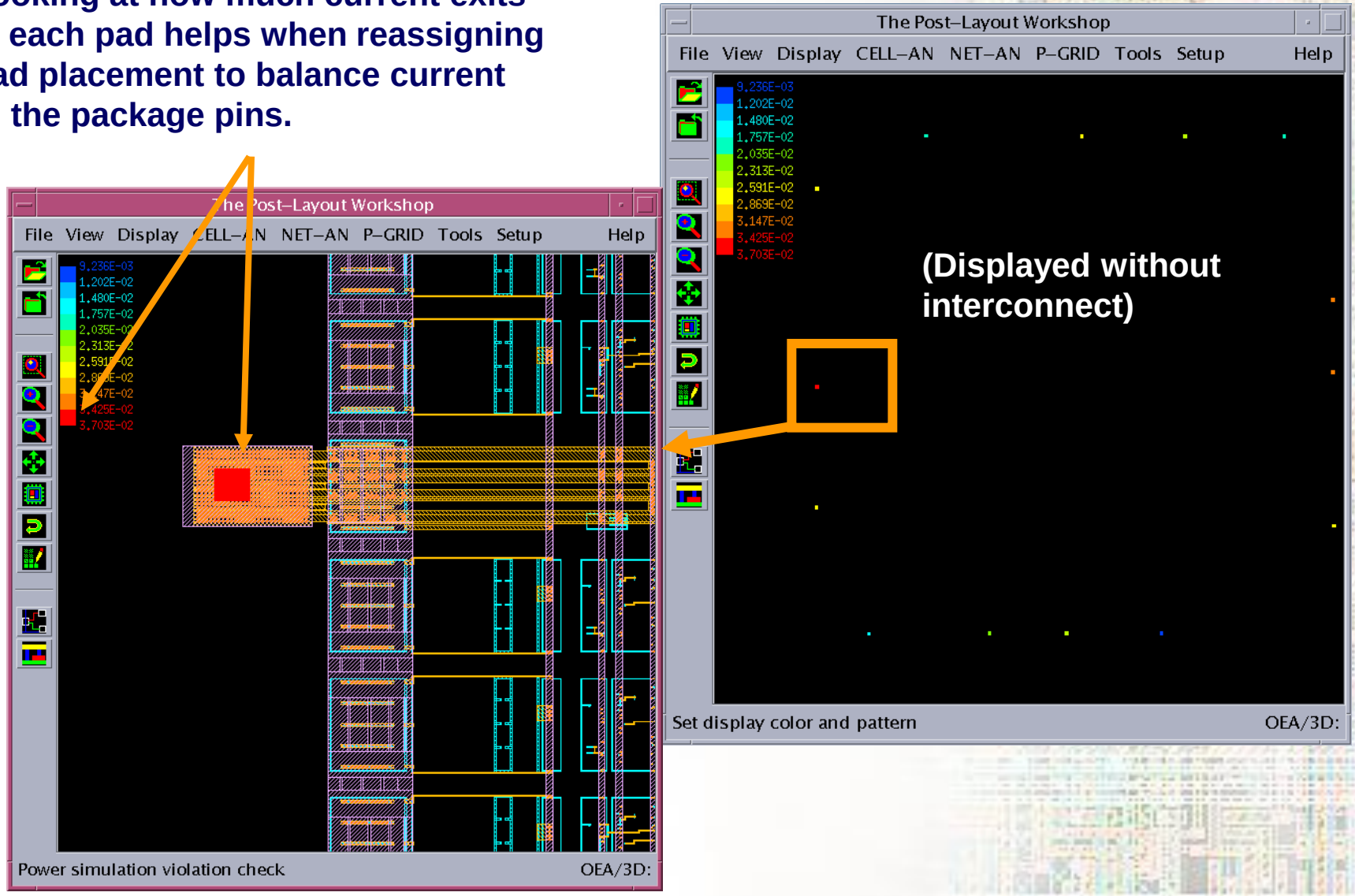
Selected Range Voltage Drop Display

- Easy to find a limited range of values



Examine the Balance of Current Flow to Voltage Input Pads

Looking at how much current exits at each pad helps when reassigning pad placement to balance current to the package pins.



Current Location File for Example Chip

- 806,770 total contact current sources

```
806770
  208.000   208.400   489.600   490.000  31
  208.000   208.400   490.800   491.200  31
  208.000   208.400   492.000   492.400  31
  208.000   208.400   493.200   493.600  31
  208.000   208.400   494.400   494.800  31
  208.000   208.400   495.600   496.000  31
  208.000   208.400   496.800   497.200  31
  208.000   208.400   498.000   498.400  31
  208.000   208.400   499.200   499.600  31
  208.000   208.400   500.400   500.800  31
  208.000   208.400   501.600   502.000  31
  208.000   208.400   502.800   503.200  31
  208.000   208.400   504.000   504.400  31
  208.000   208.400   505.200   505.600  31
  208.000   208.400   506.400   506.800  31
  208.000   208.400   507.600   508.000  31
  208.000   208.400   508.800   509.200  31
  208.000   208.400   510.000   510.400  31
  208.000   208.400   511.200   511.600  31
  208.000   208.400   512.400   512.800  31
  208.000   208.400   513.600   514.000  31
  208.000   208.400   514.800   515.200  31
  208.000   208.400   516.000   516.400  31
  208.000   208.400   517.200   517.600  31
  208.000   208.400   518.400   518.800  31
  208.000   208.400   519.600   520.000  31
  208.000   208.400   520.800   521.200  31
  208.000   208.400   522.000   522.400  31
  208.000   208.400   523.200   523.600  31
  208.000   208.400   524.400   524.800  31
```

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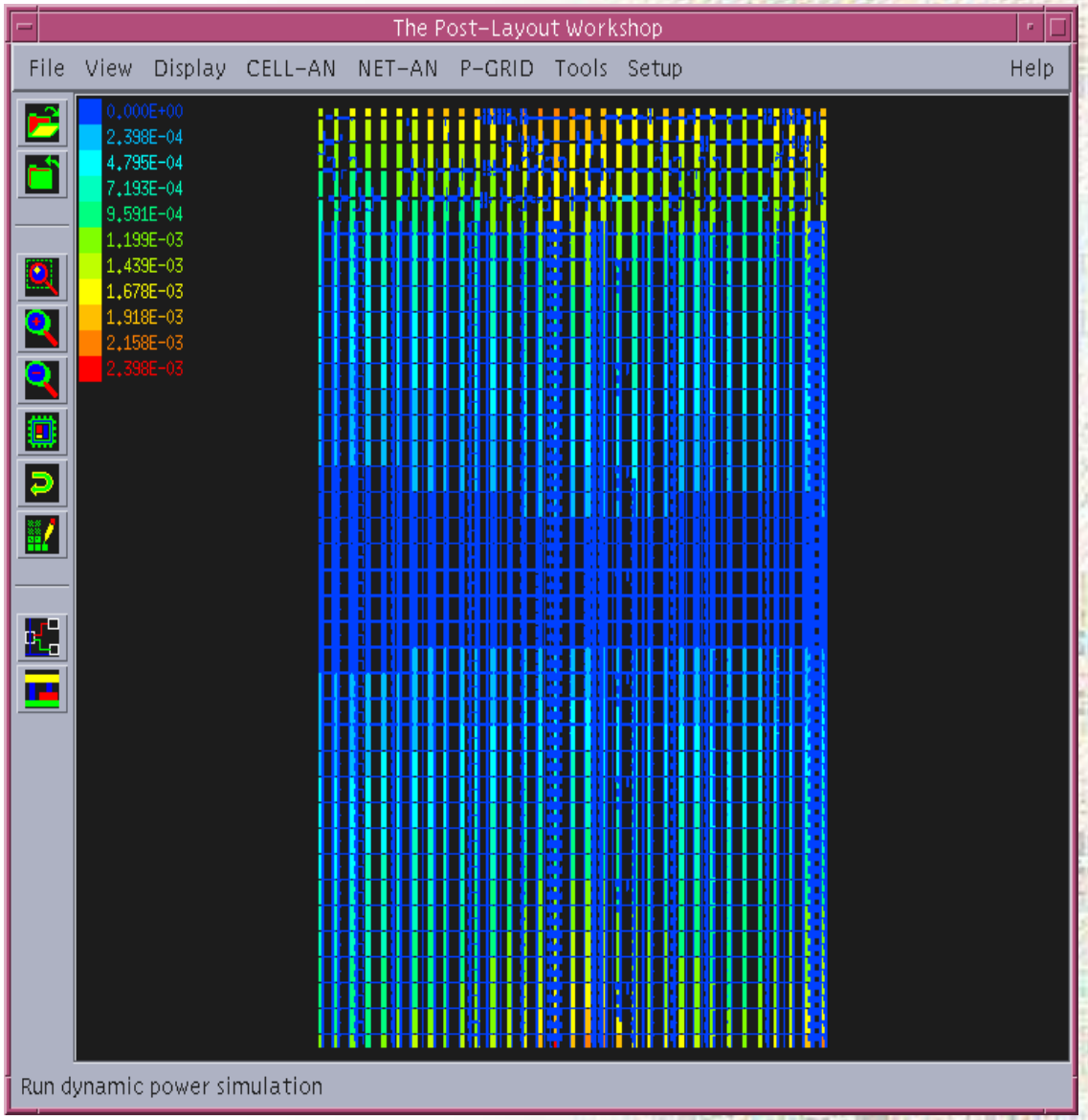
Sample Report for Worst Case Voltage Drop

```
#
# PGRID Violation Report
# Data File: /export/home/jerry/jobs/amd3/top_area/newtop.Vdist
# Violation Range: (6.0000e-02 - 6.4705e-02)
#
# Xmin Xmax Ymin Ymax LayerNo. Value
#
  3650.130   3650.880   1996.130   1996.880 33  -6.4705e-02
  3650.230   3650.770   1995.990   1996.130 33  -6.4705e-02
  3650.230   3650.770   1989.080   1989.210 33  -6.4705e-02
  3650.230   3651.380   1988.430   1989.080 33  -6.4705e-02
  3650.630   3651.380   1988.330   1988.430 33  -6.4705e-02
  3650.230   3650.770   1989.210   1995.990 33  -6.4705e-02
  3694.320   3695.070   1996.130   1996.880 33  -6.4239e-02
  3694.430   3694.980   1995.990   1996.130 33  -6.4239e-02
  3694.430   3694.980   1989.080   1989.210 33  -6.4239e-02
  3694.320   3695.070   1988.330   1989.080 33  -6.4239e-02
  3694.430   3694.980   1989.210   1995.990 33  -6.4239e-02
  3682.630   3683.380   1997.430   1998.180 33  -6.4445e-02
  3682.730   3683.270   1997.290   1997.430 33  -6.4445e-02
```

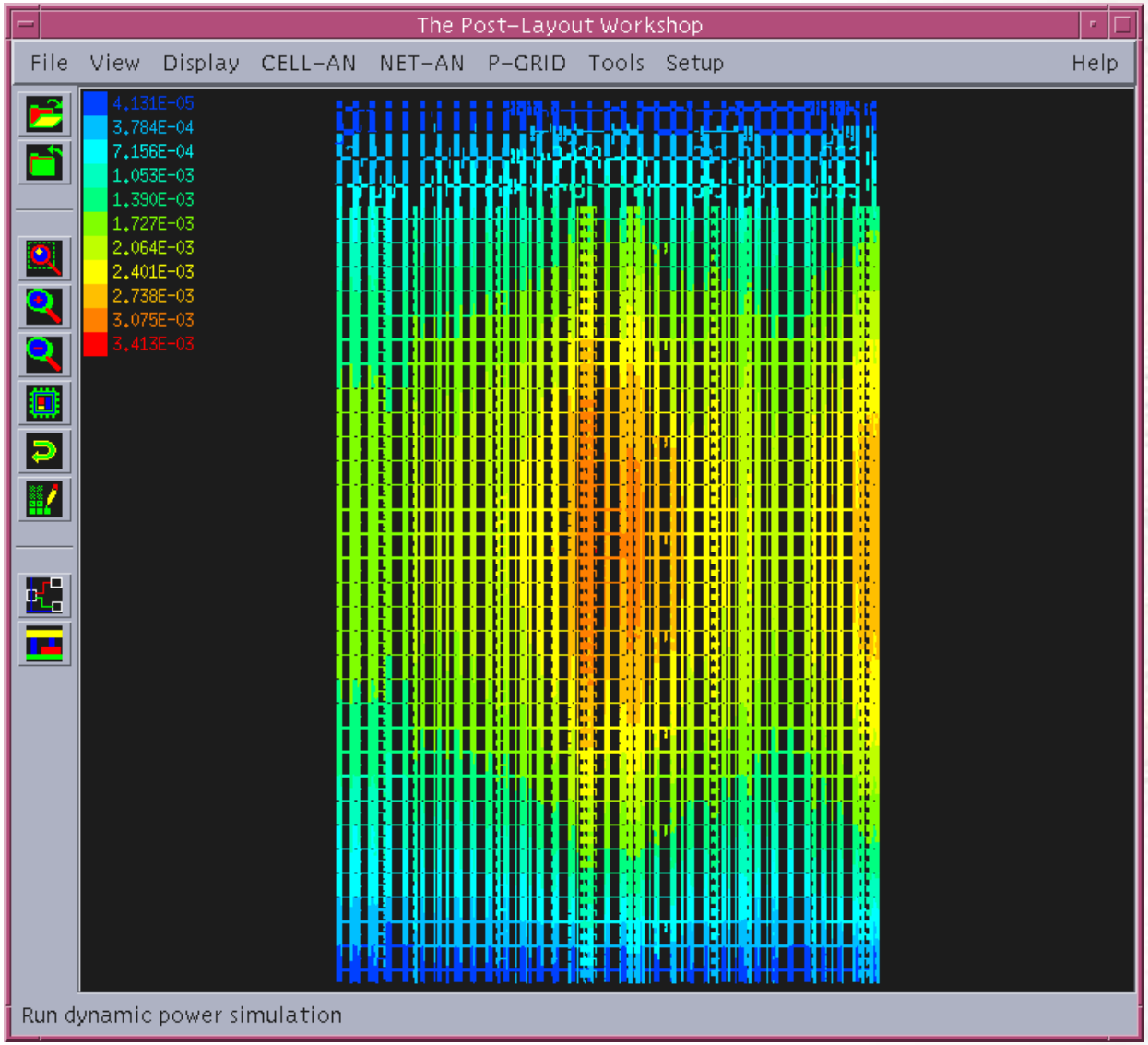
P-GRID Sample Color Coded Output

Block Current Density Display

4 Layers
84,494 Current Sources
10.8 MB GDSII File
0.18 X 0.30 cm



P-GRID Sample Color Coded Output



Block Voltage Drop Display

4 Layers
84,494 Current Sources
10.8 MB GDSII File
.18 X .30cm

Hierarchical Power Distribution Network Analysis