OEA International, Inc.

Parasitic Inductance Impact Study

Final Report

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Submitted December 27, 1999

1. Scope

This report will cover both theory and practical application of inductance concepts. It is the results of OEA's years of research, study, thousands of simulations, and study on inductance modeling and behavior. Frederick W. Grover founded much of the OEA work in the book entitled, "Inductance Calculations, Working Formulas and Tables". This book written in 1946, has become the base line 'Inductance Bible' for almost all technical work and papers since.

This report will focus on on-chip inductance effects and will begin by reviewing the first reported case of measured on-chip inductance effects in 1994. Next, a review of theory as it applies to on-chip interconnect will be presented followed the calculation method known as partial inductance and it's application to on-chip interconnects. Then, a presentation on inductive behaviors in interconnects and the relationship to width, length, and frequency is given. Next, the formulation and theory for mutual inductance is presented with the application and effects on bus structures. An inductance effect on the power distribution network is presented with an example application of simultaneous switching and ground bounce on a VDD/VSS IO ring. In addition, the VDD/VSS inductive return path is reviewed and examples of calculations are reviewed. Finally, conclusions and guidelines are presented.

2. First Reported Case of On-Chip Inductance

Historically, OEA found the first recorded on-chip inductance in 1994 on a SGI T5 microprocessor top-level clock distribution network. The example shown below in Figure 1 is one of 32 of top-level clock nets on the chip. Each net was 7 microns wide and expanded to a relatively large area of approximately 1 cm by 0.75 cm which is approximately one-fourth of the chip. On inspection of the figure, there appears to be a numbers of errors in the plotting, but there is not. The net jogging back on itself is cheating circuitry so there will be equal lengths from the driver to the four buffer locations, numbered one through four.

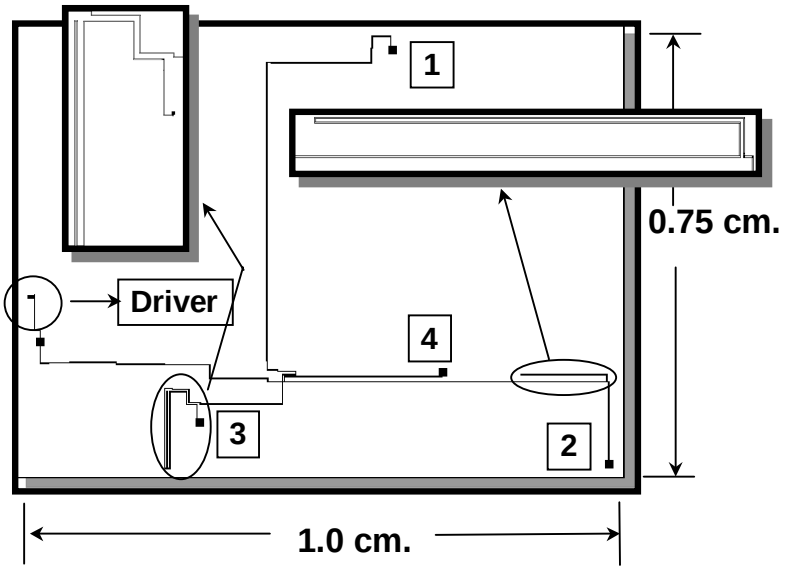


Figure 1: Level 1 Clock Net

Since 1991, OEA has had inductance tools and on-chip inductance extraction capability since 1993, but it was never put to use early on. In 1994, purely by accident on this particular net, we decided to use it and compare it to RC simulation results. Two circuits were generated using the same NET-AN 3D field solver. Both spice deck versions consisted of the same calculated 1401 resistors and 1084 capacitors in a distributed Spice network. Both net circuits were terminated at 16 gate buffer ties with large capacitive loads located equally and representing the large buffer input capacitances. The only difference in the two Spice networks was that one had 1001 inductors calculated in NET-AN and distributed with the resistors in the long lines. The clock buffer was driven with an input clock waveform of a 0.45 nanosecond rise time pulse with a 3.0-volt transition, which is approximately a 144 MHz clock frequency. The comparison at that time was very educational and showed for the first time the effects of on-chip inductance.

Figure 2: Comparison of Waveforms With & Without Inductance

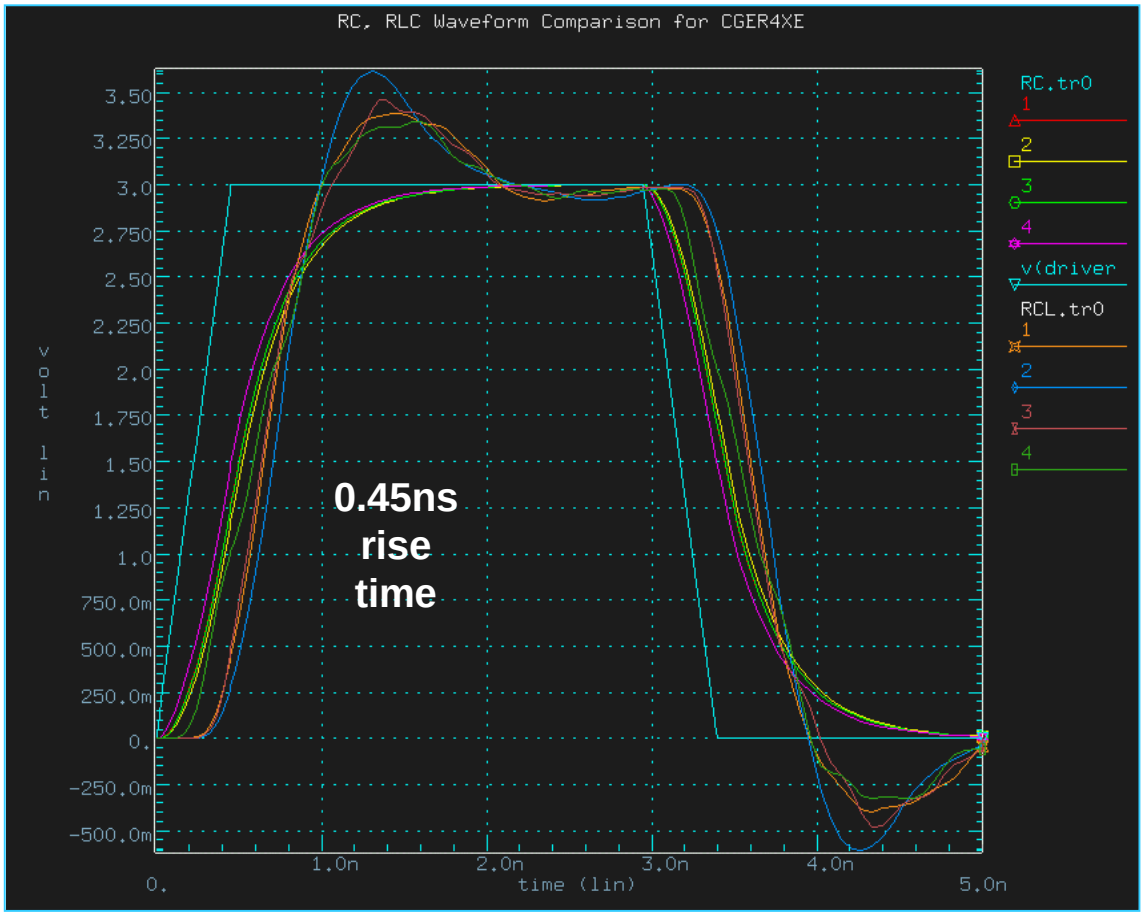


Figure 2 above shows the RC waveforms results versus the RCL waveforms results in these four buffer locations. The RCL model waveforms show an overshoot of a little over 0.5 volts and approximately a 0.5 volts undershoot that is very typical of having inductive elements in the circuit. The effect the designer is concerned about is the delay, since it is a digital circuit clock net. The delay was measured at the switching point (1.5 volts) on the four gate load locations of the RC and RCL lines and put into the table shown in Figure 3 below.

Figure 3: Delay and Skew Comparison for the Level 1 Clock Net

	T_{d1} (ps)	T_{d2} (ps)	T_{d3} (ps)	T_{d4} (ps)	Skew (ps)
RLC	422	479	410	360	119
RC	275	295	276	228	67
C	0	0	0	0	0

As shown in the last entry, resistance is definitely needed to have skew. If there is just a C model, it is a single node and therefore will not have any skew. The RC model is used by most designers and displays 275, 295, 276, 228 pico-seconds of delay for T1, T2, T3, and T4 respectively resulting in 67 pico-seconds of skew. However, if you include the inductance in the model with the same capacitance and the same resistance the delay values go up considerably. For example, T1 goes from 275 to 422 pico-seconds, and T3 goes from 276 to 410 pico-seconds, resulting in a skew of 119 pico-seconds. This is an approximate 2X difference from the RC simulation skew. Assuming this clock had a skew budget of 100 pico-seconds. It would appear to have passed using only RC values, when in reality, by using the full RCL values it would have failed.

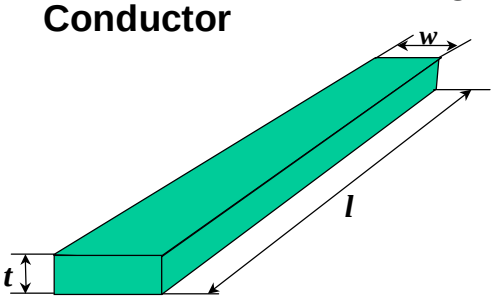
This real life example is just the first of many cases that prove that including inductance for some critical nets was important. The challenge was to find out the reasons why this case was special and how you can predict when inductance will be important to be included and when it can be ignored.

3. Inductance Calculation Theory and Calculation Methodology

As every engineer has learned, Michael Faraday discovered inductance, or more appropriately electromagnetic induction, when experimenting with a conductor passing through a magnetic field. He discovered when a magnetic field is passed near a conductor, or visa versa, there is a current flow in the conductor. By reversing the process, it stands to reason that whenever a current passes through a conductor, there is a change in the electromagnetic field (emf) around the conductor. The set of equations commonly used to calculate this emf and current relationship is the Maxwell's set of equations, Gauss's Law, Faraday's Law and Ampere's Law. When considering inductance for on-chip interconnects, one needs to understand the formulations for inductance as they apply to rectangular conductors.

In earlier OEA work, OEA experimented with many circuits and did not find a strong inductive behavior in many of them although they were a lot longer and larger nets than the one discussed in Section 2. Most of the other nets were much more heavily loaded. For this study, OEA focused on figuring out the basic reason why some circuits exhibit a very strong difference between RC and RCL levels and others did not. The study started with the basic mathematics of finding the partial inductance of rectangular conductor by itself sitting in free space. Assuming a conductor has a length of L, width of W and a thickness of T, the inductance in μH is formulated as shown below in Figure 4.

Figure 4: Inductance of a Rectangular Conductor



$$L(\mu H) = 0.002l\,\{\ln[2l/(w+t)] + 0.5 - k\}$$

where $k = f(w\,t)$ *and* $0<k<0.0025$

$$R(\Omega) = \delta\, l/(w\,t)$$

$$Z(j\omega) = R + j\omega L$$

$$Q = \frac{\mathrm{Im}[Z(j\omega)]}{\mathrm{Re}[Z(j\omega)]} = \frac{L\omega}{R} \qquad \textit{where}\quad \omega = 2\pi f$$

The formula shows that longer lines will be more inductive and wider lines will make smaller inductance. In a way, it behaves like resistance. Resistance is a function of the length divided by the width times the thickness. Inductance is a function of the length divided by the width plus the thickness. Both resistance and inductance increase with length and they are both

inversely proportional to the width and thickness. The big difference is that resistance is a function of the width times thickness (W*T) whereas the inductance is a function of the width plus thickness (W+T). This effect accounts for a large amount of scaling differences in the two parasitics in interconnects. This also shows why wide and long nets are relatively more inductive in terms of the on-chip application.

When you ignore the capacitance, the calculation for the impedance of interconnects between the two endpoints is also shown. In addition, there is a formula for the Q value of the interconnect inductor. The Q value, or quality factor, is the classical definition of the imaginary part of the impedance divided by the real part of the impedance. That can be translated to $L\omega/R$. Whenever this Q value is larger, then the interconnect acts as a better inductor. As the frequency goes higher this Q value varies in proportion to the inductance and therefore you will have a more inductive behavior.

4. Magnitude of Inductance on Interconnect

This section will examine the magnitude of this self-inductance for some typical on-chip circuits.

Assuming a layer of one micron thickness, we have plotted the length versus the inductance values for various widths of 0.25 micron to128 micron. Lengths are shown ranging from zero to all the way to 2cm, which represents the typical chip size today. See Figure 5 below.

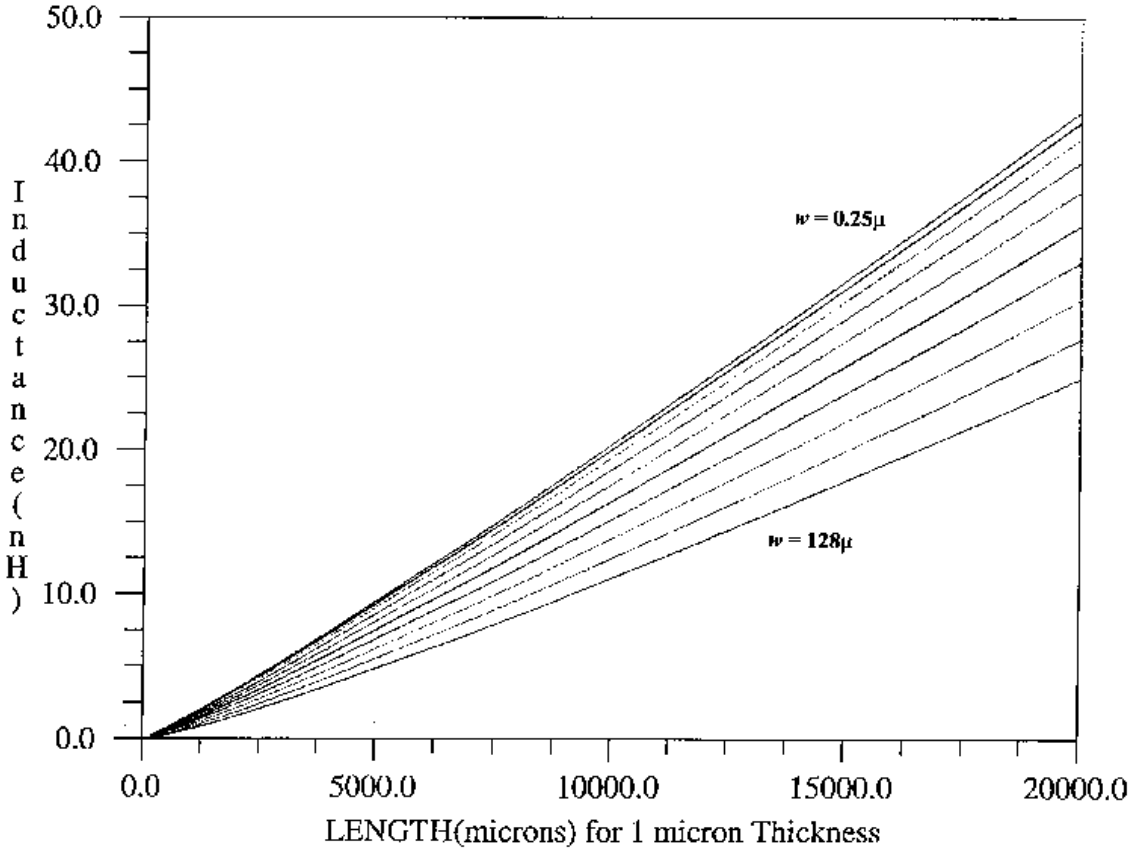


FIGURE 5: Inductance versus Length for Widths of 0.25, 0.5, 1.0, 2.0, 4.0, 8.0, 16.0, 32.0, 64.0 and 128.0

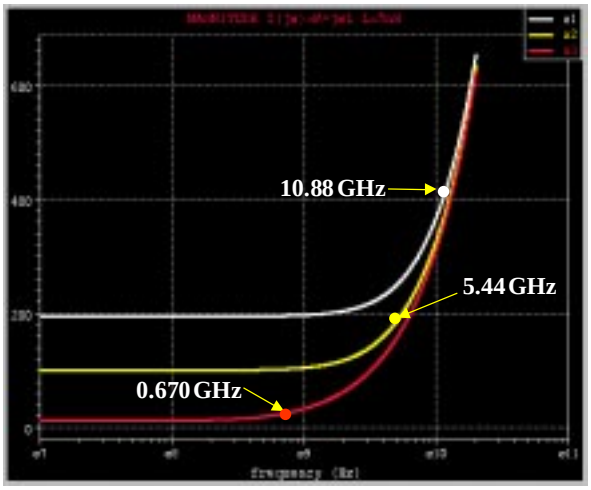
An example of a 1cm chip with 128 micron wide line exhibits approximately 10 nH of inductance which is very large even though it is a very wide line. But, if reduce the line width to 0.25 micron wide the inductance value will approach 20 nH. As you can see, 500X increase in width only increases inductance by a factor of 2X. With resistance, the increase in resistance from 128 microns wide to 0.25 microns wide would be 500X. This illustrates the major difference between the resistance behavior and inductance behavior by function of width.

When you look at these values, it is apparent that they are relatively large numbers. With a length of 2 cm, there will be about 25 nH of inductance for 128 micron line width. For a length of 2 cm and a 0.25 micron line width there will be approximately 45nH of inductance. If you had only inductance on these lines, they would be very noisy. Luckily, (remember the formula for inductance of a rectangular conductor) a line does not have inductance by itself it also has a resistance with it. The important value relating to the behavior of the interconnect then is really the impedance.

$$\delta = 3.24 \cdot 10^{-6} \Omega\ cm$$

$$t = 1\mu\ ,\quad L = 5\,nH$$

$w = 0.5\mu$	$l = 3013\mu$	$R = 195.2\Omega$
$w = 1\mu$	$l = 3109\mu$	$R = 100.7\Omega$
$w = 10\mu$	$l = 3821\mu$	$R = 12.38\Omega$



$$f_{pass} = \frac{R}{2\pi L} = \frac{\delta}{0.002w\,t\,[\,ln\left(\frac{2l}{w+t}\right) + 0.5 - k\,]\,2\pi}$$

Figure 6: Pass Frequency of 5 nH Inductor with 0.5, 1, and 10 μ Width

Figure 6 above shows some typical impedance curves. Assuming for this figure, the desired inductance value is 5nH made by using various widths of 0.5, 1 and 10 microns and using a resistivity (δ) equal to 3.24 * 10^{-6} Ω cm. If the width is 0.5 microns, a length of 3,013 microns with a one micron thickness is required to produce a 5nH inductance. The resulting is resistance is 195.2Ω. If the width increases to 1 micron wide, the length increases from 3,013 microns to 3,109 microns. A longer line is required to achieve the 5nH goal and the resistance will go down to 100.7Ω, almost half of the previous value. Finally, if the width increases to 10 microns wide, then the length must increase to 3,821 microns long and decreasing the resistance to 12.38Ω. As can be seen, there is a very significant reduction in the resistance value versus a relatively insignificant increase in the length to achieve 5nH.

Looking at the impedance curves for the 0.5, 1, and 10 μ widths as a function of frequency, the Fpass, or Pass Frequencies, at the corner points of this curve is where the line starts to exhibit a strong inductive behavior. As the width increases, the frequency where it starts to behave inductively starts going lower and lower. The corner frequency shown for the 10

micron width is 670MHz. This means if there is a line in a design that is 10 microns wide, 3,821 microns long and 1 micron thick, inductance needs to be included in simulations for frequencies above 670MHz. Now this pass frequency shifts up to 5.44GHz for a one micron wide line and up to 10.88GHz for 0.5 micron wide line. This illustrates that as the width gets wider, the inductive behavior of the interconnect starts at lower frequencies. This is completely contrary to what one might think. As the widths become narrower, the inductance value increases but the resistance values increase much faster than the inductance. Therefore, inductance for narrow lines is not important; one needs to be watchful of the wider lines.

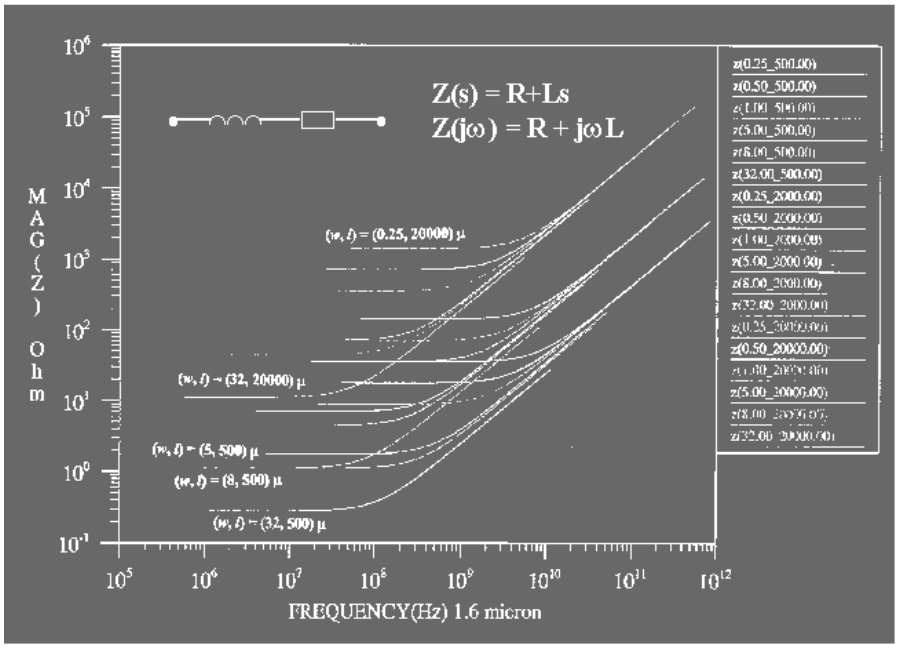
Again, reviewing the formulas below for the Q of an inductor and the pass frequency it shows clearly by looking at the width and length factors that the wider the width, the better the inductor. The higher the Q value, the better the inductive behavior of interconnect and wider lines have a higher Q. The wider the interconnect, the lower the band pass frequency where it starts acting more inductive than resistive.

$$Q = \frac{0.002w\,t\,[\,ln\left(\frac{2l}{w+t}\right) + 0.5 - k\,]\,\omega}{\delta}$$

$$f_{pass} = \frac{R}{2\pi L} = \frac{\delta}{0.002w\,t\,[\,ln\left(\frac{2l}{w+t}\right) + 0.5 - k\,]\,2\pi}$$

Figure 7 shows a log /log plot of the magnitude of the impedance as a function of frequency. In this Figure you can view the corner frequencies for various lengths and widths, but it is difficult to see these relationships clearly.

Figure 7: Magnitude of the Impedance as a Function of Frequency for Different Width and Length of Metal



The figure above clearly shows the length for the pass frequency is not a major factor in the inductive behavior of interconnect. Once the interconnect passes around 1,000 microns, the effect of length for various widths is relatively flat. The width however is shown to be a major factor with the 128 micron width remaining at a relatively low pass frequency with relation to the 0.25 micron wide interconnect pass frequency. This shows that the main problem is width not length.

Figure 8: Pass Frequency as a Function of Length for Different Widths (1μ Thick Metal)

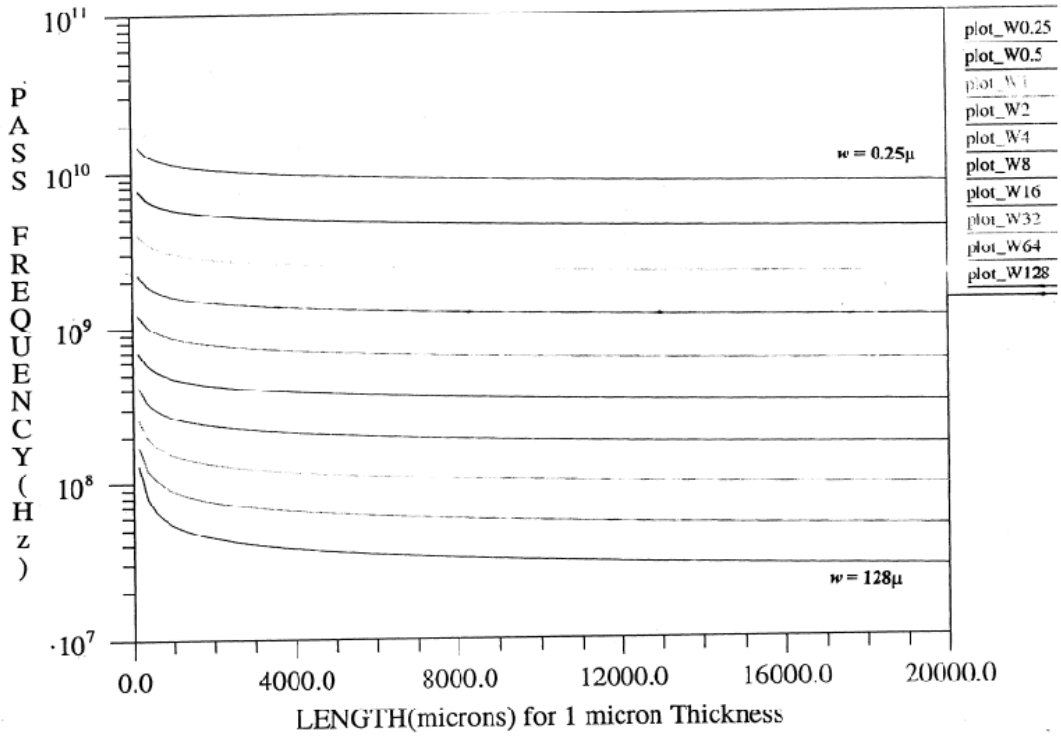
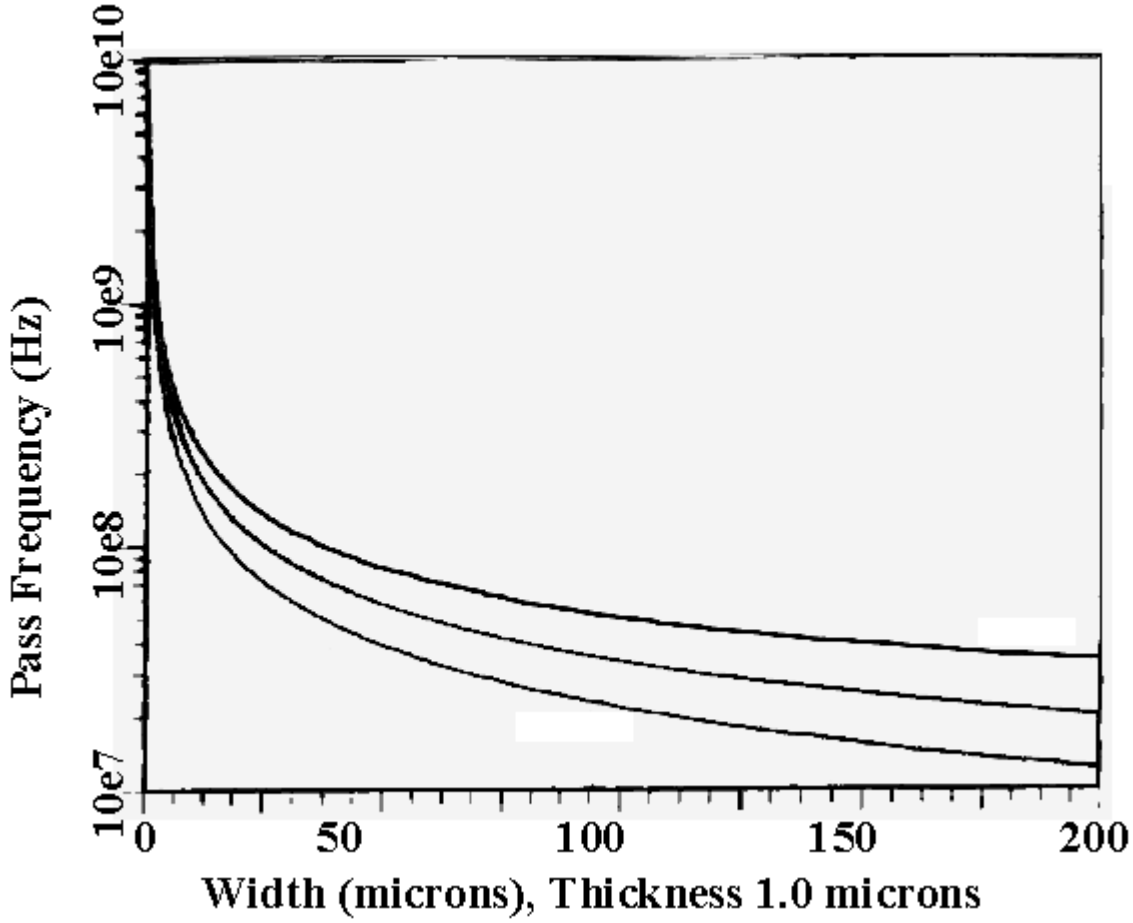


Figure 9: Pass Frequency as a Function of Widths for Different Lengths (1.0µ Thick Metal)



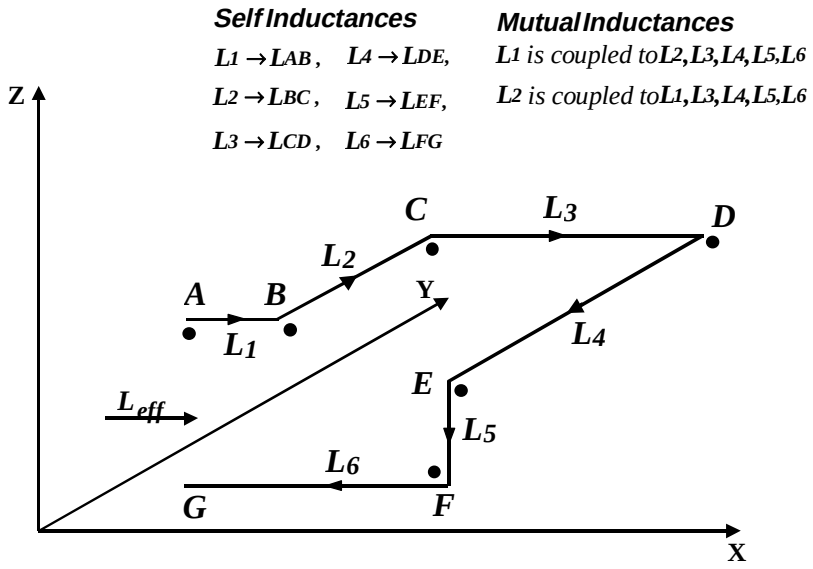
In Figure 9, we see the same plot as in Figure 8 but with a different axis. Here the pass frequency is plotted with relation to width of the conductor. Here we can observe a strong relationship of width to inductive behavior.

For example, with a 10 micron wide line, inductance becomes a factor at around 200MHz. For 5 micron wide line, which is a typical clock line, inductance becomes a factor at about 500MHZ. In other words, after 500MHz you need to include inductance in the Spice simulation to correctly model the circuit performance for 5 micron wide line. Below 500MHz inductance is not that important.

5. The Partial Inductance Concept

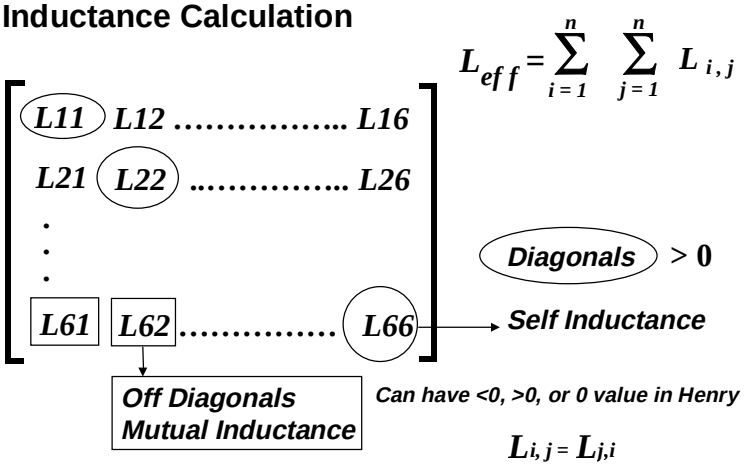
A more complicated circuit, a circuit made up of a number of elements, is shown in Figure 10. The arrows on the segments indicate how the currents flow in this particular circuit illustration. You may ask, 'how can we calculate the inductance of this particular structure?' The easy answer is to use the partial inductance concept, which calculates the self-inductance of each segment and sums all of the mutual inductances between every segment.

Figure 10: The Partial Inductance Concept



This calculation can be clearly shown in a matrix representation shown in Figure 11 below. The diagonal terms represent the self-inductances and off diagonal terms represent the mutual inductances of each segment. Diagonal terms must always be positive. Off diagonal terms can be negative, positive or zero. If the line segments are 90 degrees to each other, the off diagonal terms or mutual inductances would be zero. This matrix is always a symmetric so Lij's will be equal to Lji's. To calculate inductance of the entire structure, one needs to add all the terms objectively to get effective inductance or loop inductance to the structure seen in the above illustration.

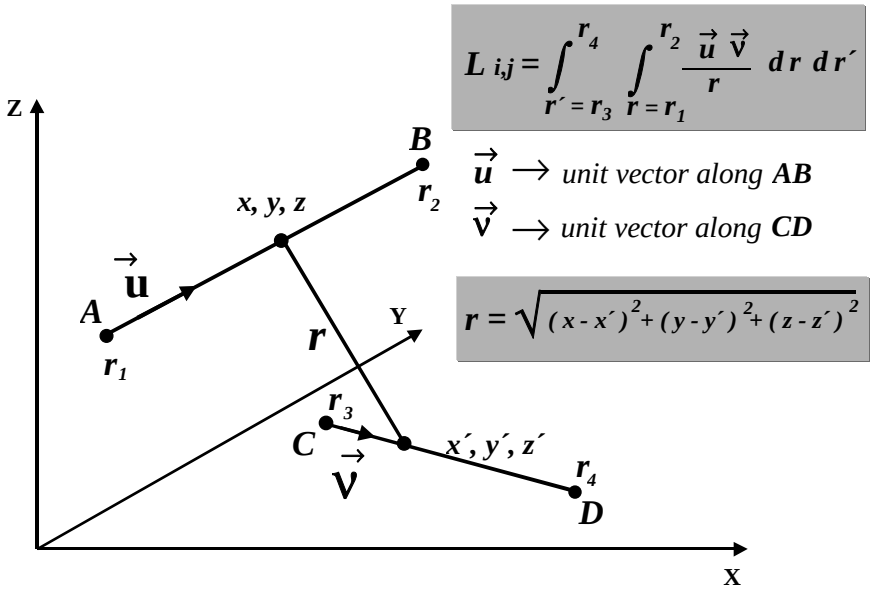
Figure 11: Matrix Representation of the Partial Inductance Calculation



6. Formulation of Mutual Inductance

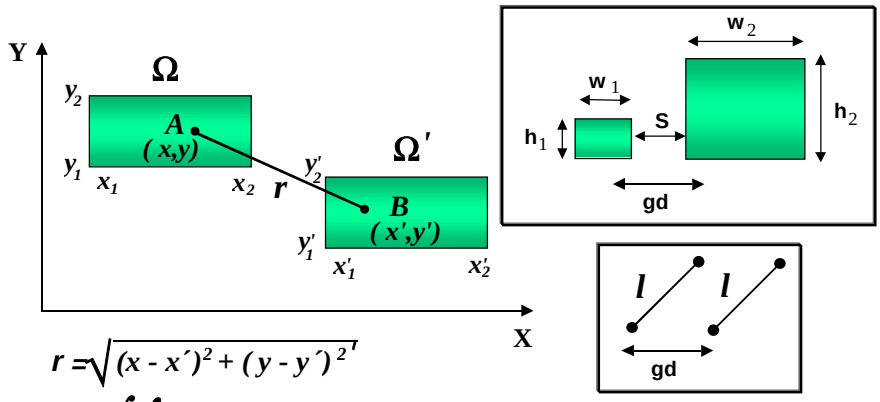
The Figure 12 below illustrates two line segments, A-B and C-D with vectors u and v. Assuming for now these line segments are infinitely thin and act as filaments. The Neumann formulation calculates the mutual inductance between any two line segments modeled as filaments such as these. As can be seen the Neumann formula is a double integral of the vectors u and v divided by the geometric distance, r times the distances of r and r'. This integral is not an easy one to calculate, but when solved may be applied very generally and universally to any mutual inductance solution. This introduces a new concept known as the 'geometric distance'.

Figure 12: The Neumann Formulation of Mutual Inductance



In order to apply the Neumann formula to interconnects, one must find the equivalent filament points or the geometric distance between the objects or in this case line segments. The formula shown in Figure 13 below may be used to calculate the mutual inductance between any objects or line segments. As can be seen, finding the geometric distance requires a quadruple integral calculation but in solving this, we simplify the mutual inductance equation by allowing a simpler solution. The validity of using this method can be proven by solving the full six integral solution and comparing results.

Figure 13: The Geometric Distance Between Objects

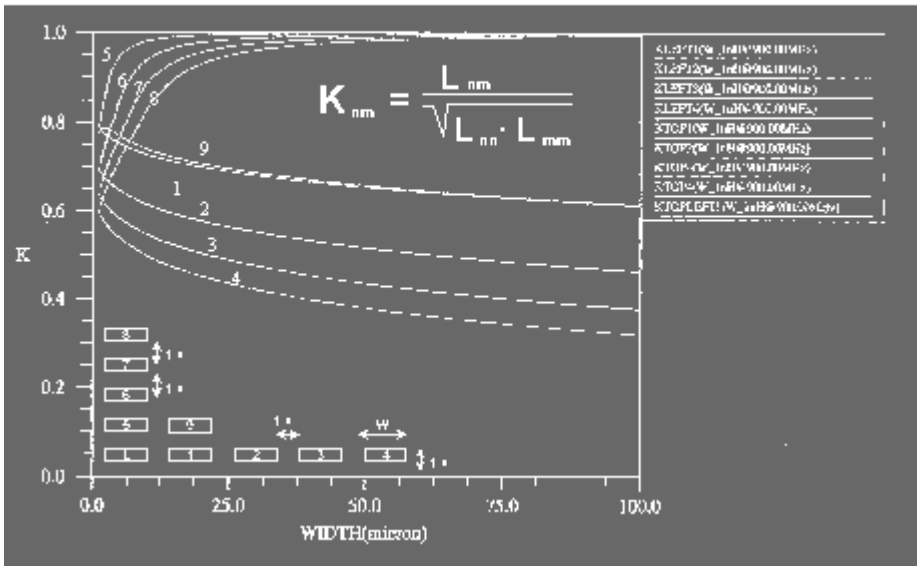


$$r = \sqrt{(x - x')^2 + (y - y')^2}$$

$$gd = \int_{\Omega'} \int_{\Omega} \ln(r)\, d\Omega\, d\Omega'$$

$$gd = \int_{y'=y_1'}^{y_2'} \int_{y=y_1}^{y_2} \int_{x'=x_1'}^{x_2'} \int_{x=x_1}^{x_2} \ln\sqrt{(x - x')^2 + (y - y')^2}\; dx\, dx'\, dy\, dy'$$

Figure 14: Mutual Inductance Coupling Coefficient K as a Function of Width



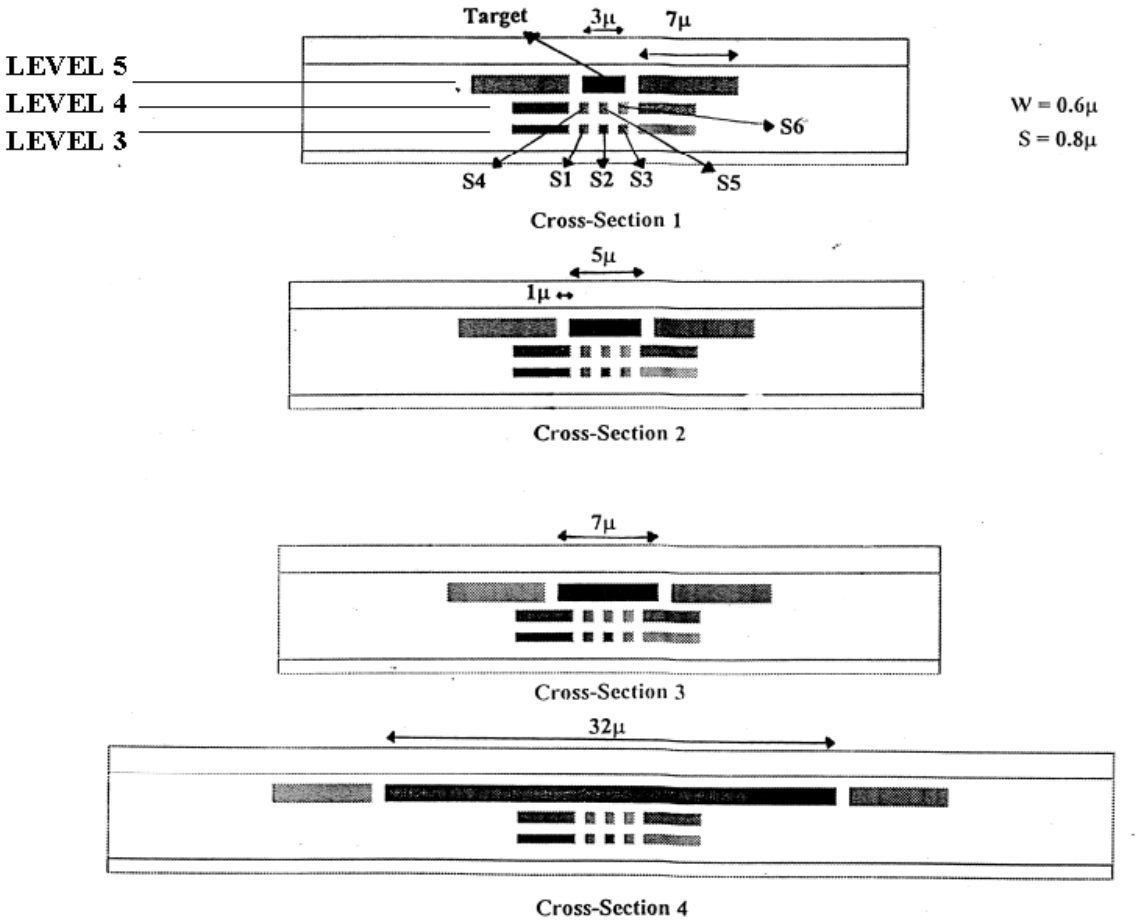
In Figure 14, the calculated mutual inductance coupling coefficient (K) is explored as a function of width for lines that are adjacent on the same layer (lines 1-4), coplanar and above on different layers (lines 5-8), and adjacent on a higher layer (line 9). Remember that earlier, we postulated that the wider the lines the more problem with inductance. In this example, we are exploring mutual inductance as a function of width. For the simulations, we are using a constant line spacing and layer spacing of one micron. The width varies from 0.25 to 100 microns. As can be seen, the mutual inductance of adjacent lines on the same layer starts out high at a K of 0.8 for the next line over (line 1) and only drops to a K of 0.6 as the width increases to 100 microns. For a narrow line, where the line is still fairly resistive this may not have any significance, but for wider lines operating at a higher frequency mutual inductance can have a very significant effect. Examples of where mutual inductance may be important would be a wide top-level clock line shielded with wide VDD/VSS lines or for VDD/VSS equalization ring lines. The mutual coupling decreases as the line gets farther and farther away but line 4 still exhibits a K value of 0.35 at a distance of more than 300 microns. This shows that mutual inductance is truly a long-range effect and is not shielded as is capacitance coupling. For adjacent lines on a different layer, line 9, approximately the same coupling is observed as if it were on the same layer. This is because the geometric distance as the width increases is approximately the same as line 1. Coupling for coplanar lines directly above the target line, lines 5-8, have a K value which ranges from 0.6 to 0.8 at the narrow widths but rapidly increase to above 0.95 at a width greater than 25 microns wide. This indicates that one should be careful of parallel lines on any interconnect layer when using interconnects with wide lines.

7. Analysis of Simple Bus Structures

In this section, a presentation of experiments on simple bus structures is reviewed to analyze crosstalk effects on signals and the effects of the return path on the signal quality.

In the analytical work presented previously, we focused on showing and proving general inductance and mutual inductance behavior and circuit effects. Thus, the capacitance effects and VDD/VSS return path effects were ignored. In the analytical work, it was discovered that wider interconnects and longer interconnects exhibit more inductive effects which influence circuit performance. In order to prove this a much more thorough simulation, based on distributed RCLM models, is required. A fully coupled and distributed RCLM model would be much closer to behavior in the real environment than the behavior in an analytical environment.

Figure 15: Cross-Section of the Simple BUS Structure



One example of simulations performed is shown in the simple bus structure in Figure 15 above. In this example, a target net of 3, 5, 7, and 32 microns wide lines are used. The target

nets on the top layer of routing are shielded with VDD and VSS. Also simulated were lines on lower levels of metal of 0.6 microns wide and using 0.8 microns spacing. These signal lines were in groups of three shielded by VDD and VSS. All combinations with different switching conditions were simulated.

Figure 16: Schematic of the BUS Structure

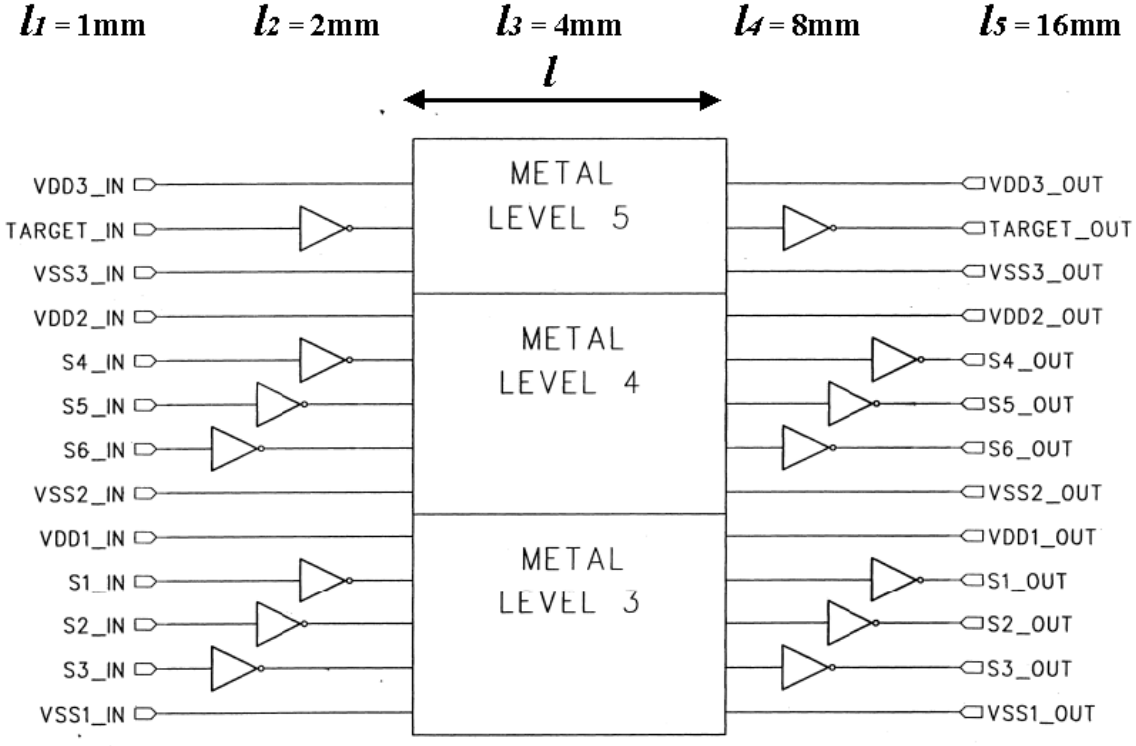


Figure 16 shows a schematic of the example simulated with the metal lines on layers 3, 4 and 5. They were simulated with close to a real circuit environment, meaning with real circuit buffers driving the lines and real terminations that were fairly large depending on the length. Lengths simulated ranged from 1 mm to 16 mm.

Figure 17: Level 5 BUS Circuit

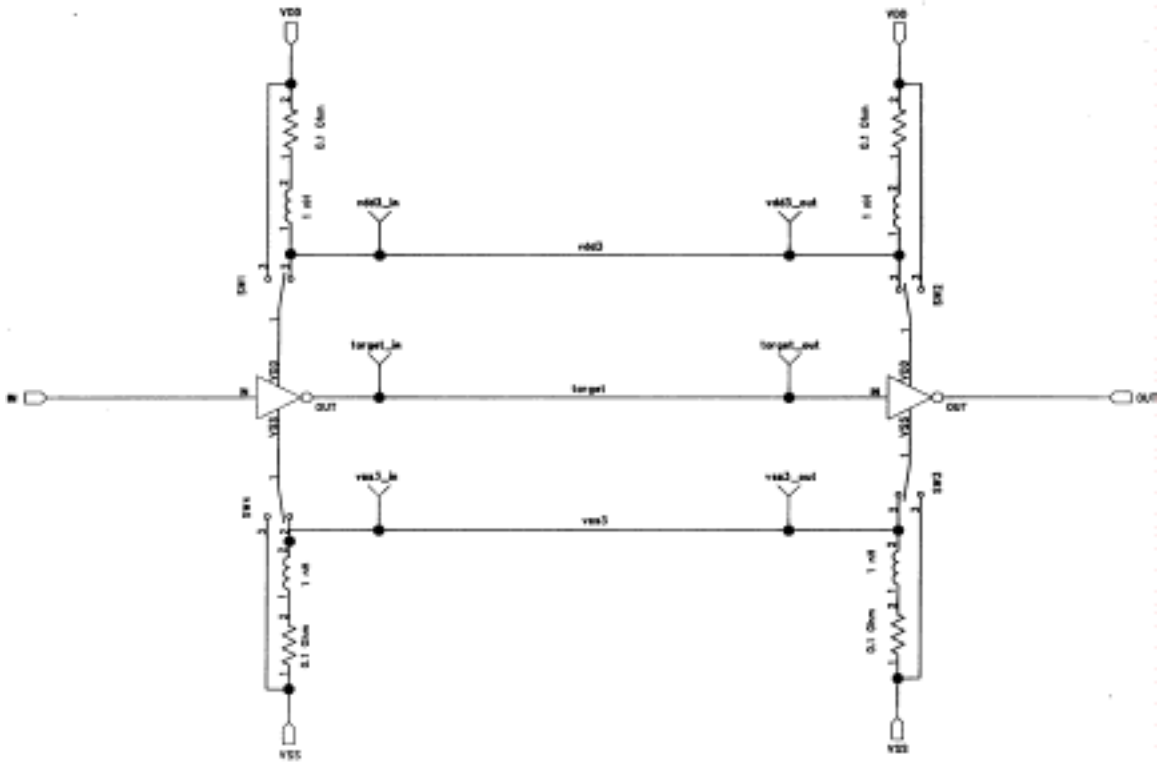


Figure 17 shows the circuit model for metal layer 5 of the example. In the simulation a toggle is provided to switch between using an ideal VDD and VSS or using a non-ideal VDD and VSS, which takes into consideration the return paths. A completely coupled and distributed circuit is used with the target signal line shielded by the VDD and VSS. The target signal is driven by a buffer and terminated by a buffer. The buffers current drive has two options. First, the buffer supplies can be tied to the ideal VDD point and ideal VSS point allowing the current to be drawn without any coupling effects. 99.9% of the simulations commonly done today are done this way. Second, the buffer supplies can be tied to the VDD and VSS through an inductor and resistor which represents the package inductance and resistance combined with the on-chip effective inductance and resistance of the VDD/VSS networks. In the second case, when the buffer is charged, its pulls the current through the package and on-chip inductance and resistance, so the VDD/VSS voltages at the buffer will start to move or bounce and its going to effect the VDD/VSS at the load buffer as well. The buffer speed has a dependency on the voltage supply difference so switching speed or delay of the buffer will be affected. In summary, when you have inductance and resistance in series with the VDD/VSS supplies to the buffers at both ends, the current draw, the di/dt times L, is going to create a voltage drop so the voltage rail at the buffer locations are going to collapse. The performance of the buffer is going to change. It is a complicated coupled mechanism, so you have to determine if your circuit performance is susceptible to return path changes before simulating.

Figure 18: Layout of the VDD, VSS, Signal Nets for the BUS Analysis

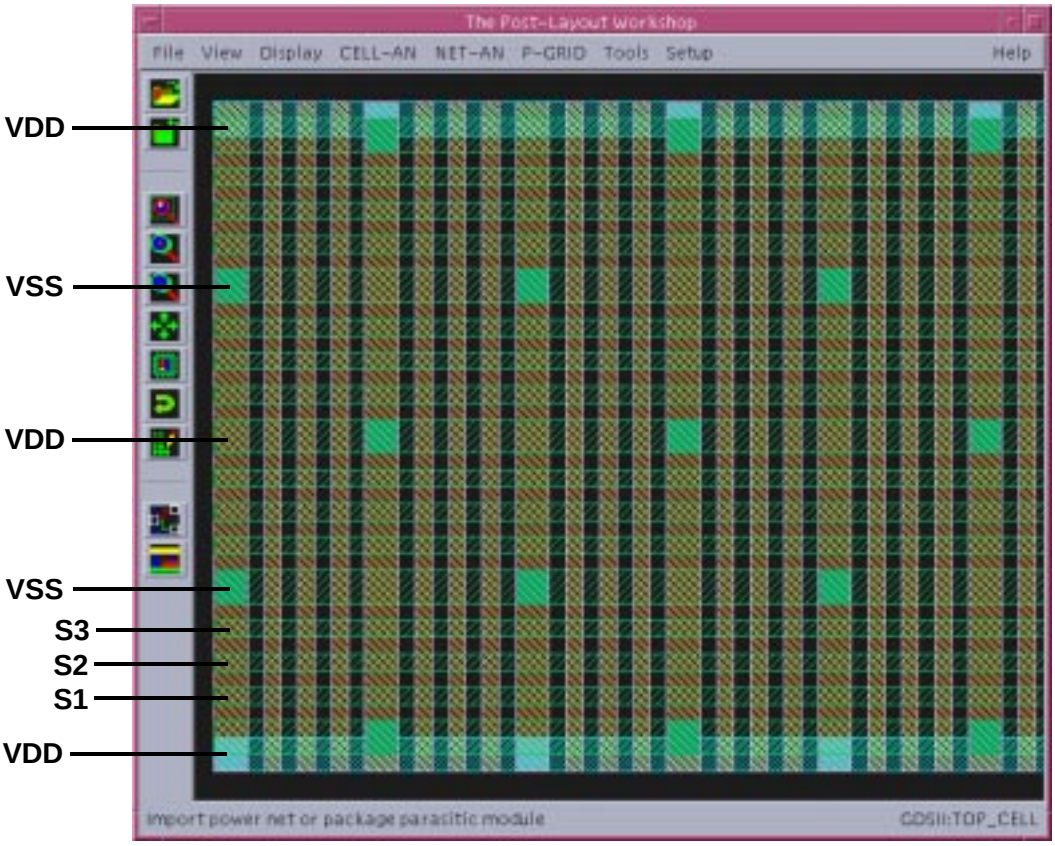


Figure 18 shows an illustration of the actual layout of the VDD, VSS, and signal nets used for the bus analysis. The crisscrossing pattern of VDD-signal-signal-signal-VSS is repeated in alternate directions to simulate the layout in a real chip design. VDD/VSS lines are connected with vias at the crossover points.

Figure 19: VDD, VSS, and Signal Nets in 3D for the BUS Analysis

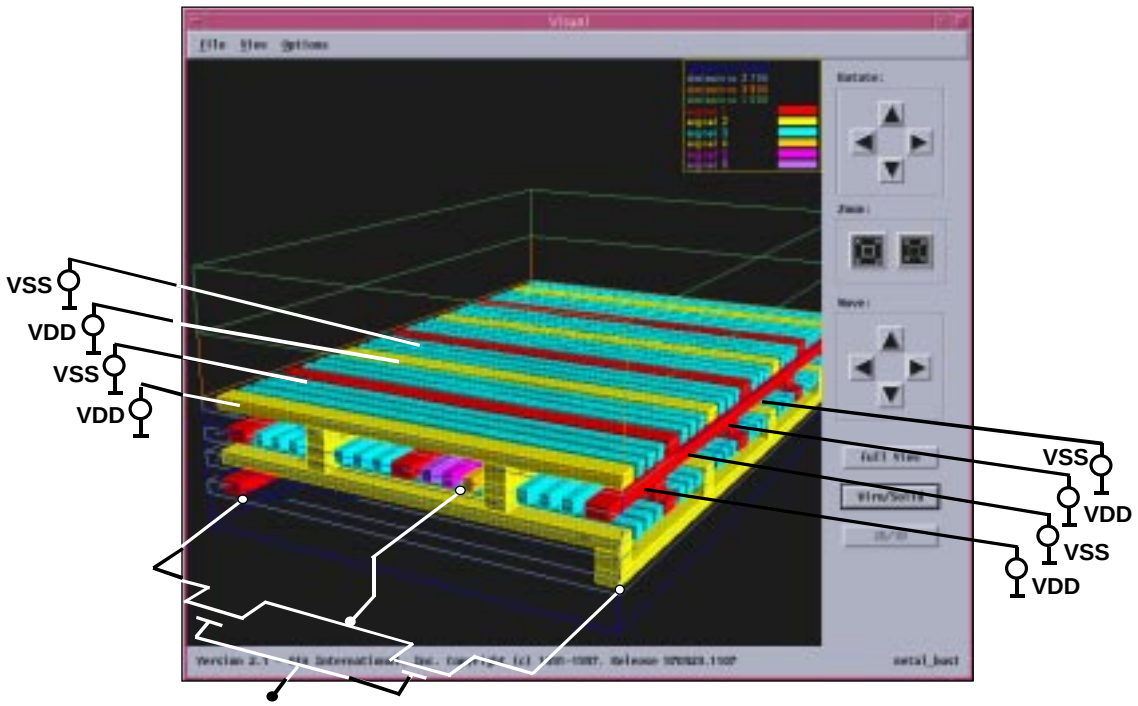


Figure 19 is a 3D view of the same bus structure and shows the complexity of the problem very clearly. As illustrated, the buffer driving the line takes the power from the nearest VDD and VSS points at the ends of the structure. The current is supplied through the complicated four layer metal structure. The red lines represent the VDD network. The yellow lines represent the VSS network. The remaining cyan lines are other signal lines which are not charged and allowed to float, are tied high, or are tied low to tie an ideal VDD/VSS network. The VDD/VSS lines are tied to the ideal sources at the very end of the chip.

Figure 20: Complete Circuit Model for the BUS Structure for Different Models of VDD and VSS Supplies

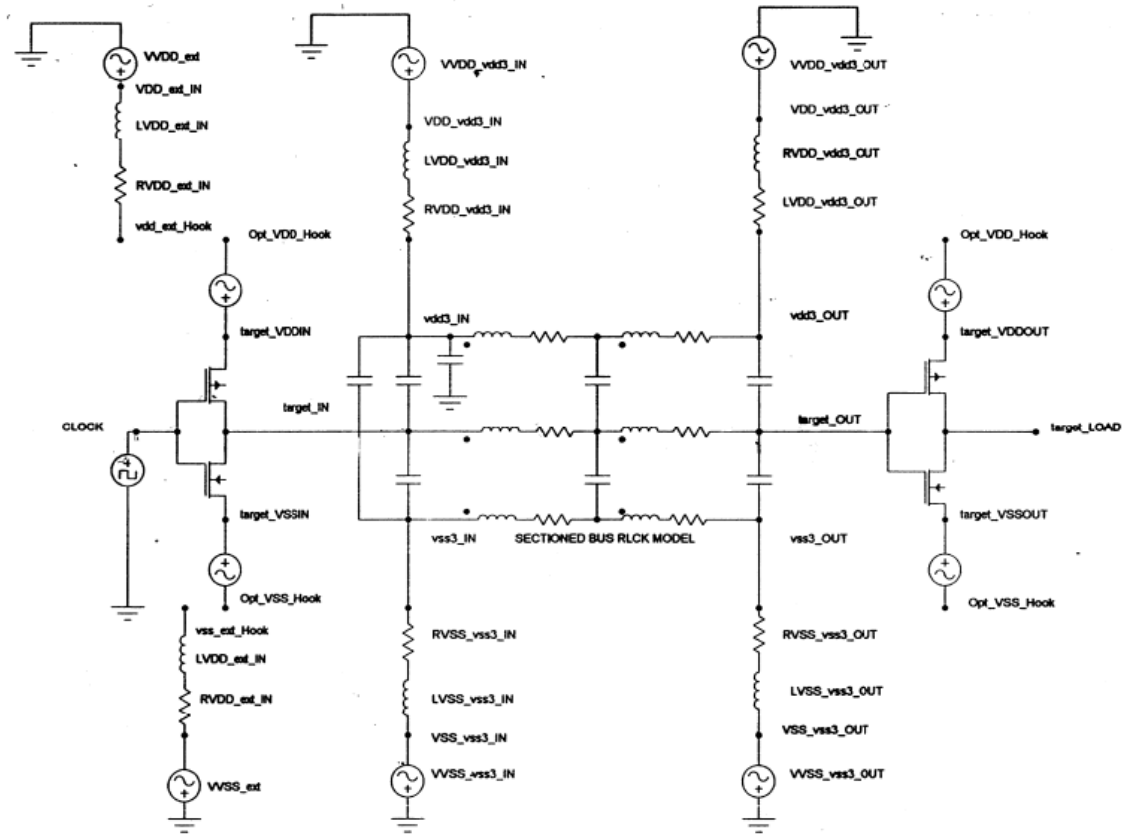


Figure 20 shows the complete circuit model for the bus structure for different models of VDD and VSS Supplies. The model illustrates that between the signal lines we have capacitive coupling and coupling to ground. There are mutual inductances between the signal lines and mutual inductance coupling to VDD/VSS lines as well. It becomes a very complicated fully coupled RCLM model. There are a number of voltage sources to monitor the currents coming from the VDD/VSS network supply points in this complex environment.

Figure 21: Example Power Distribution Grid

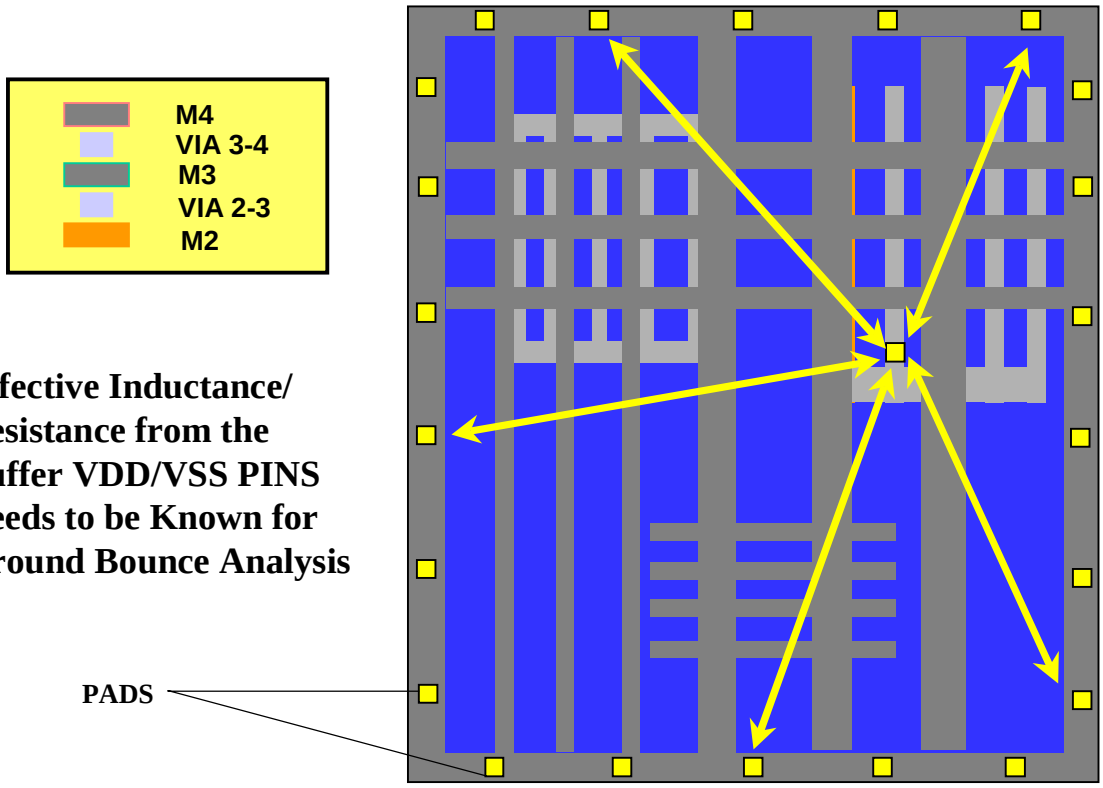


Figure 21 illustrates an example of the power distribution grid used. The lines all emanate from the location of the driver. There are a number of VDD pads and VSS supply pads on the periphery represent the places where the system voltage sources are tied. The OEA tool NET-AN is used to calculate the RLM distributed network and the OEA Simplify tool is used to calculate the effective inductance and resistance from the driver tie location to the voltage source locations. Using this method, an accurate return path resistance and inductance can be calculated for any net in the design. If many nets are to be analyzed, an effective inductance and resistance map can be constructed on the top-level power grid structure.

Figure 22: Target Width 3μ for 16mm Bus Length

"Clean and "Noisy" C, RC and RLCK Bus Models

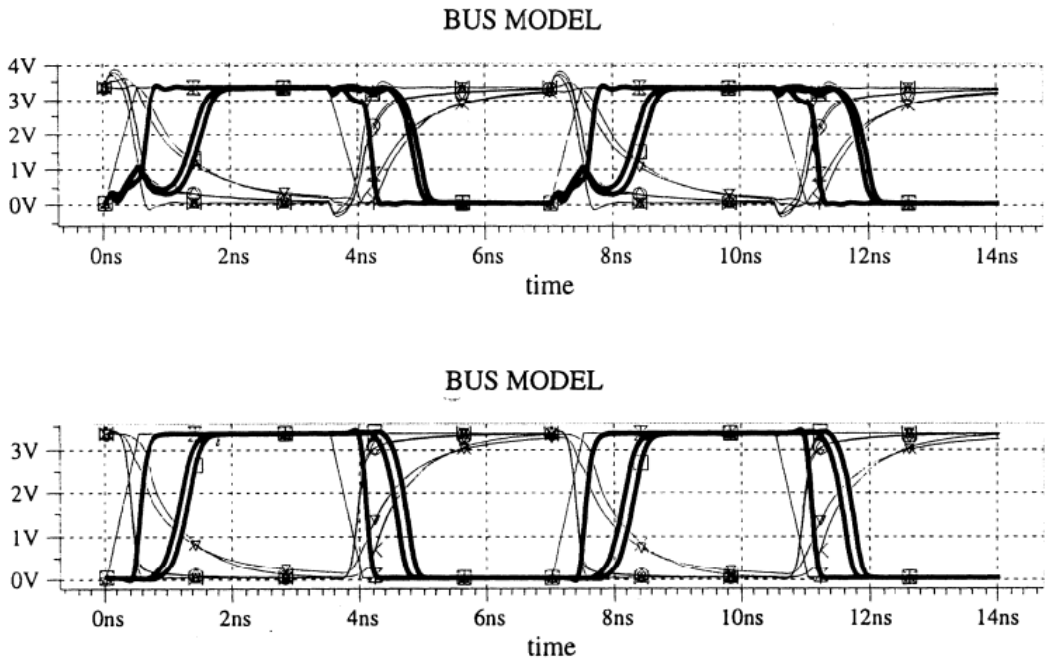
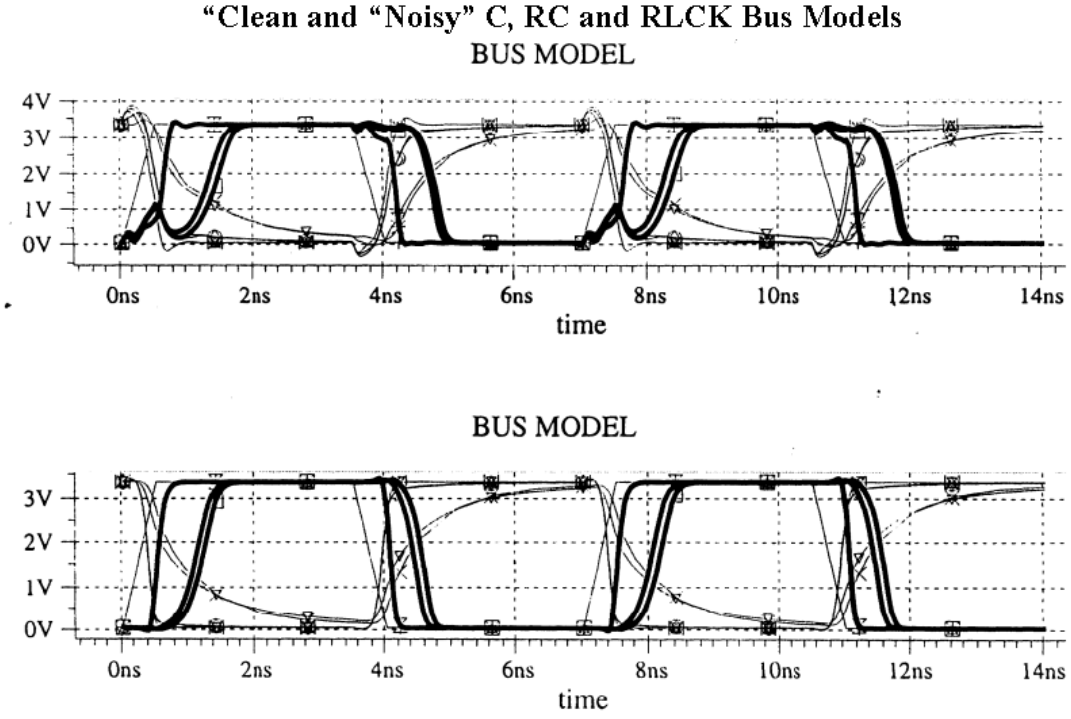


Figure 22 illustrates a simulation of a 3 micron wide net that is 16 mm long. The net is driven with a buffer and terminated at a buffer load as illustrated in the schematics above. Six waveforms in the simulations are bolded. C, RC and RLCM bus models for the noisy simulation are at the top and C, RC and RLCM bus models for the quiet simulations at the bottom. Clean is defined as when VDD/VSS is separated from interaction with the net simulation and the buffer receives the VDD/VSS directly from the ideal system VDD/VSS voltage sources. In the noisy simulation, the buffer receives the VDD/VSS through the power distribution network, which is not ideal and is coupled to this signal line. From left to right in the center range, the bolded lines represent the C model, the RC model, and the RCLM models in both noisy and clean. As can be observed, there is a significant difference between the waveforms. The slowest is the RCLM, including inductance and mutual inductance. There is a slight ringing in the noisy simulation that is due to the inductance in the power supply network. In addition, in the noisy simulation the voltage supply collapse can be observed and therefore the buffer speeds have been reduced. Therefore, the noisy delays are quite a bit slower compared to the clean simulation delays, both at the rising edge and at the falling edge.

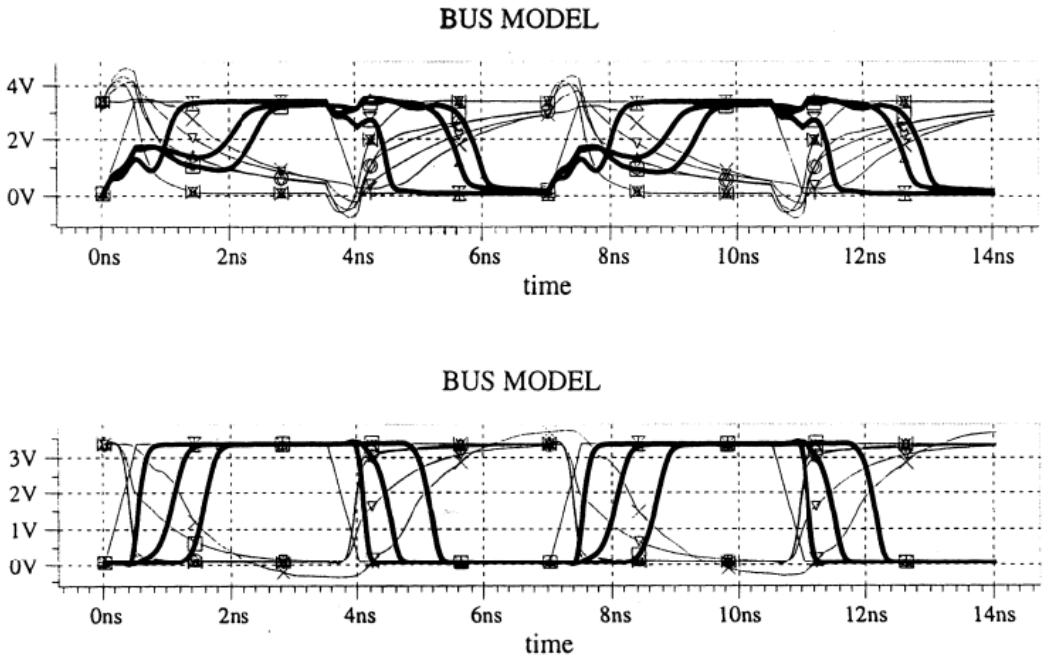
Figure 23: Target Width 5μ for 16mm Bus Length



In Figure 23, a 7 micron width is shown for the same set of simulations as above. Observe how the differences in delay and signal quality from clean to noisy change slightly, the RC and RCLM delays increasing from the 3 micron wide simulation in both the clean and noisy.

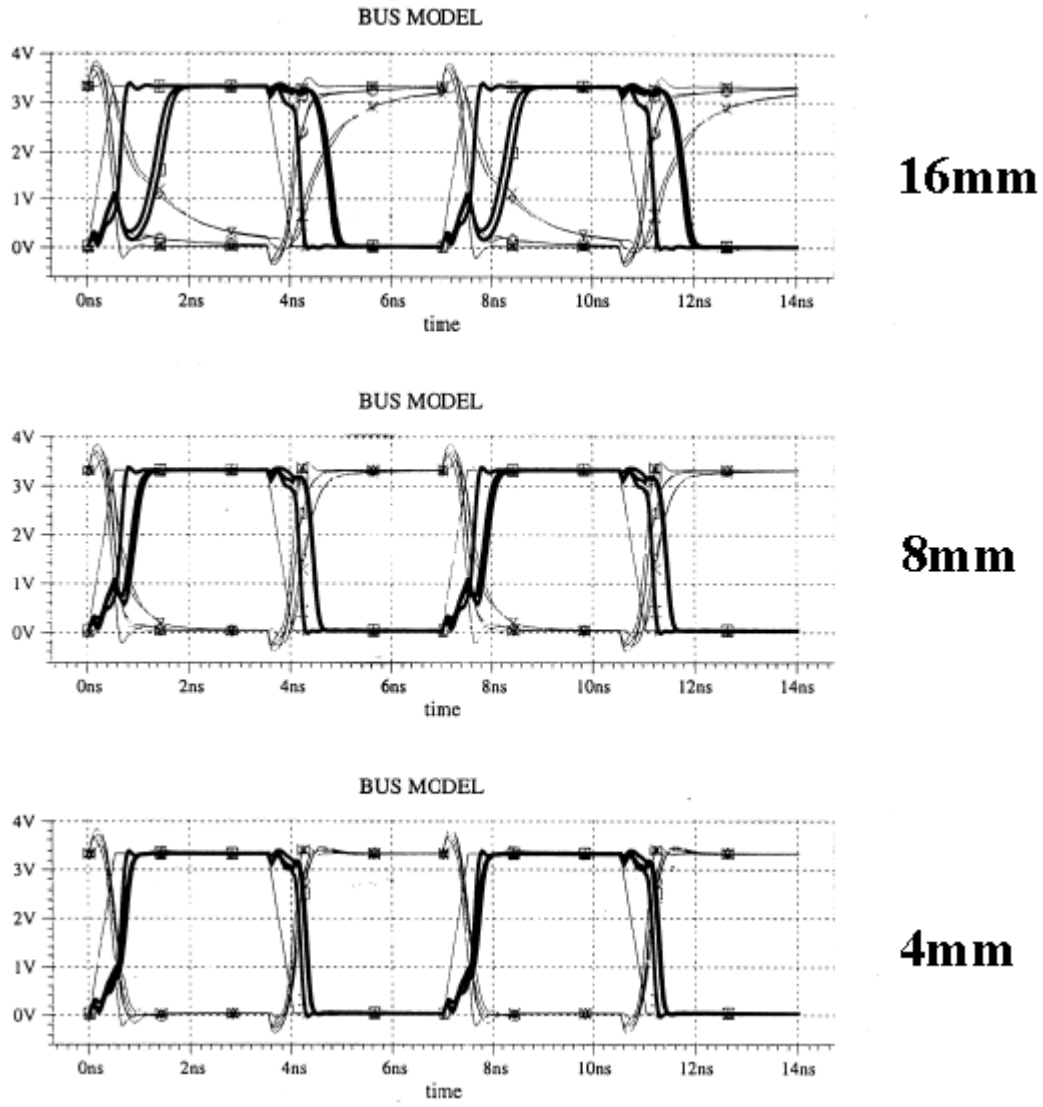
Figure 24: Target Width 32μ for 16mm Bus Length

"Clean and "Noisy" C, RC and RLCK Bus Models



In Figure 24, the width of the target signal is increased to 32 microns wide. As can be easily observed, the signal integrity of the noisy simulation has completely broken down with the delay for the RCLM signal at approximately 2.5 nanoseconds. Even in the clean simulation, the difference in delay between the RC and the RCLM is significantly more pronounced. Therefore, we have confirmed our earlier conclusion that wider interconnects exhibited significantly more inductive effects than narrow interconnects. In addition, we have confirmed that in order to simulate the actual effects of inductance on the signal quality and delay the complete coupled return path must be included in the simulation.

Figure 25: Target Width 3μ for 16, 8 and 4mm Bus Length "Noisy" Simulation C, RC and RLCK Bus Models



The inductance and inductance return path effects on signal quality and delay as related to width have been shown in the Figures 22, 23 and 24. Figure 25 illustrates the effects inductance has on signal quality and delay as related to length. Since previously it was determined that including the complete inductance return path is significant for wide interconnects, the simulations are only shown for the noisy simulations. As observed in the 4 mm, 8 mm, and 16 mm line length results, the signal delay is gets longer as the length increases. What is also apparent is that the delay difference between the C, RC, and RCLM also increases as the length gets longer. In the 16 mm simulations the delay of the RC and RCLM are significantly longer than the delay of the C only model. Obviously showing the resistance component is required for long lines.

Figure 26: Target Width 7μ for 16, 8 and 4mm Bus Length "Noisy" Simulation C, RC and RLCK Bus Models

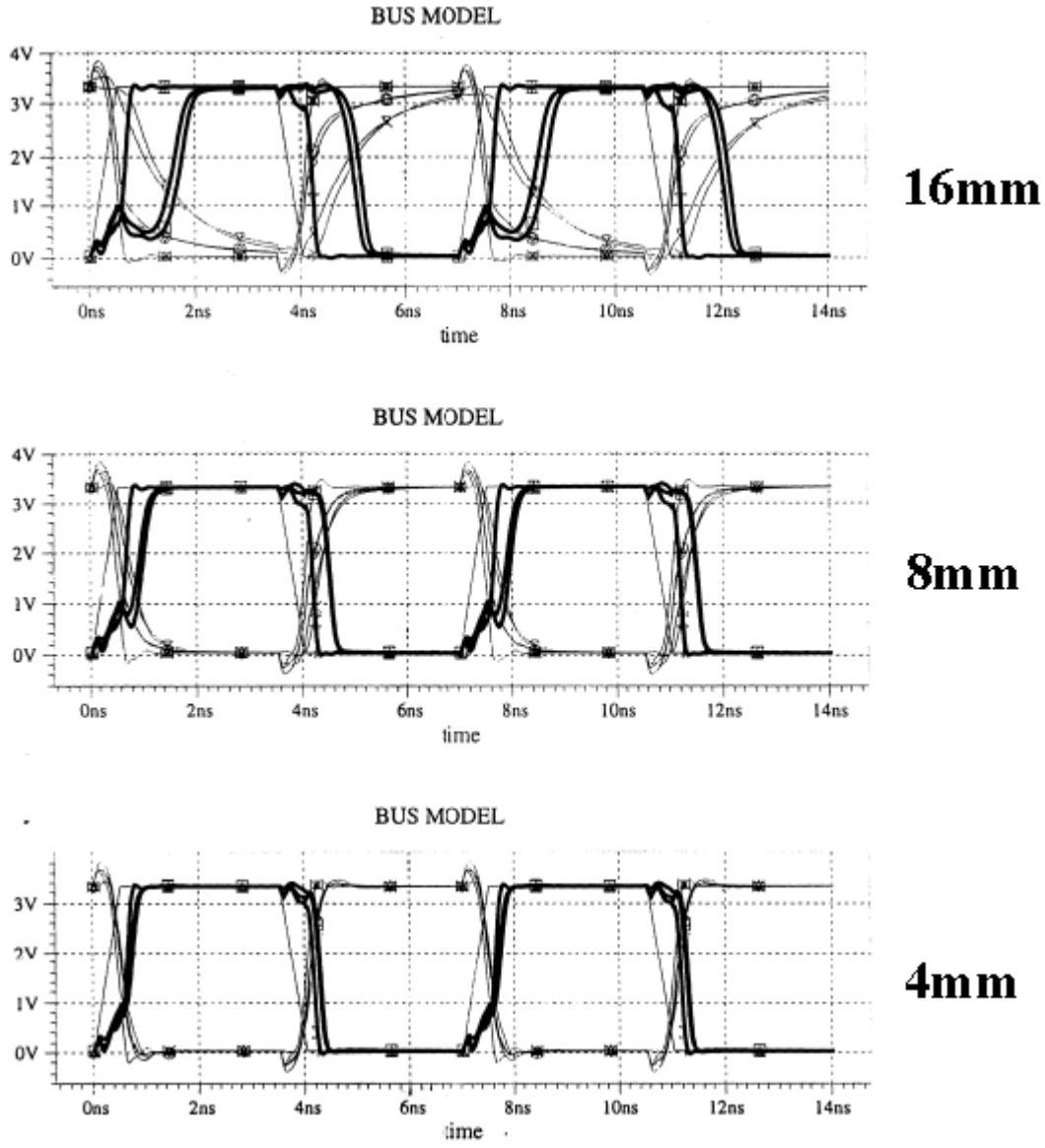


Figure 26 show the same set of simulations as the previous, except that the width has now increased to 7 microns wide. In this simulation the differences in delay in the longer lengths between the C and the RC and RCLM simulations is increased. This is due to the increased effect of the power supply inductance on the buffer, causing a further collapsing of the rails and increased delay in the signal even though the line resistance has decreased. In addition, as expected the difference between the delays of RC versus RCLM is increased.

Figure 27: Target Width 32μ for 16, 8 and 4mm Bus Length "Noisy" Simulation C, RC and RLCK Bus Models

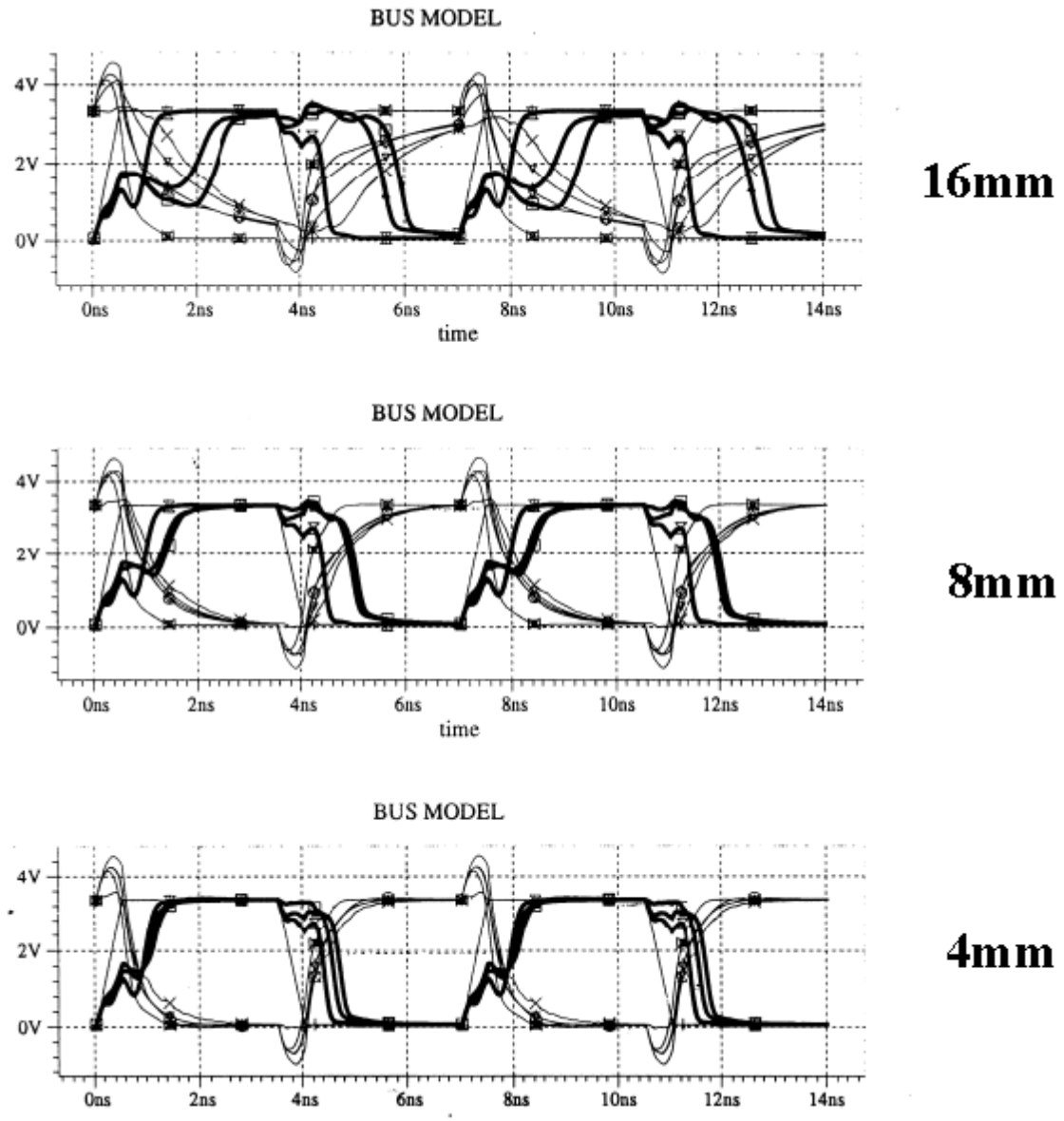
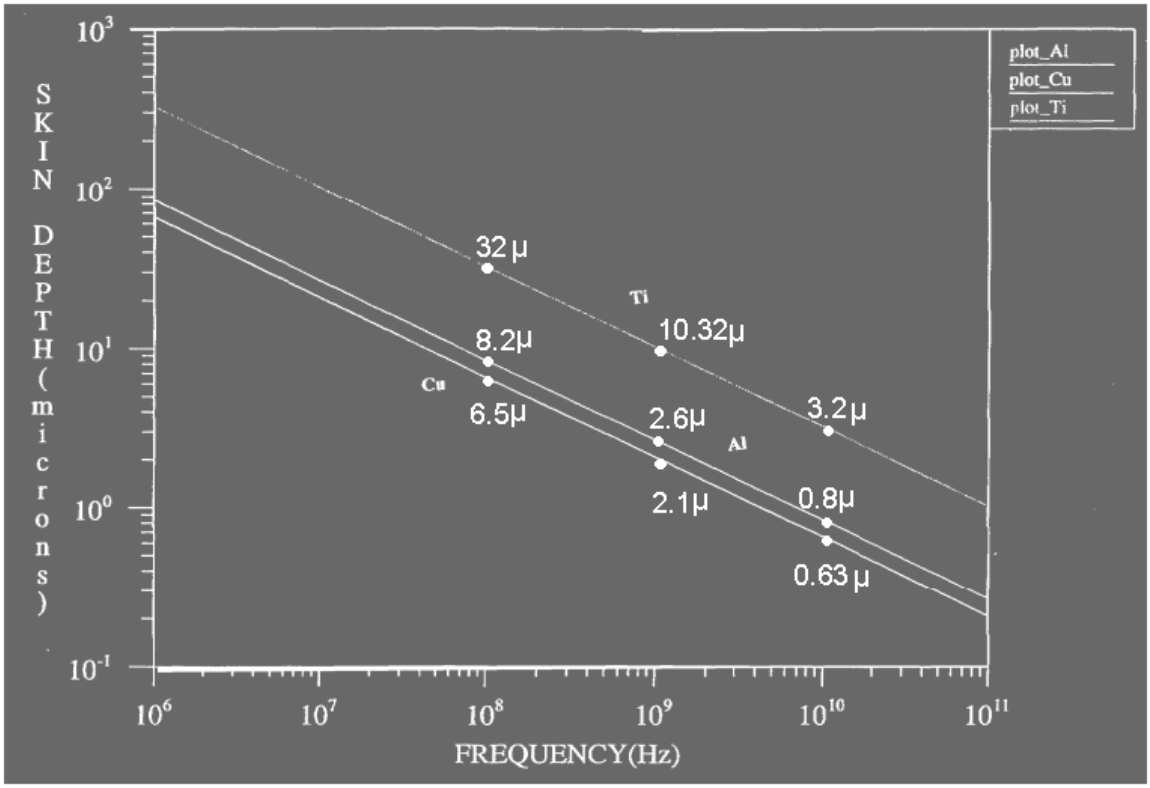


Figure 27 show the same set of simulations as the previous, except that the width has now increased to 32 microns wide. In this simulation the differences in delay in the longer lengths between the C and the RC and RCLM simulations is dramatically increased. In particular, the difference between the delays of RC versus RCLM is dramatically increased. Therefore, we can conclude that length as well as width needs to be considered when evaluating inductive effects for on-chip interconnects.

8. Skin Effects in IC Interconnect

Figure 28: Skin Depth $\delta = \sqrt{\frac{2}{\omega \mu \sigma}}$ as a Function of Frequency for Some IC Metals

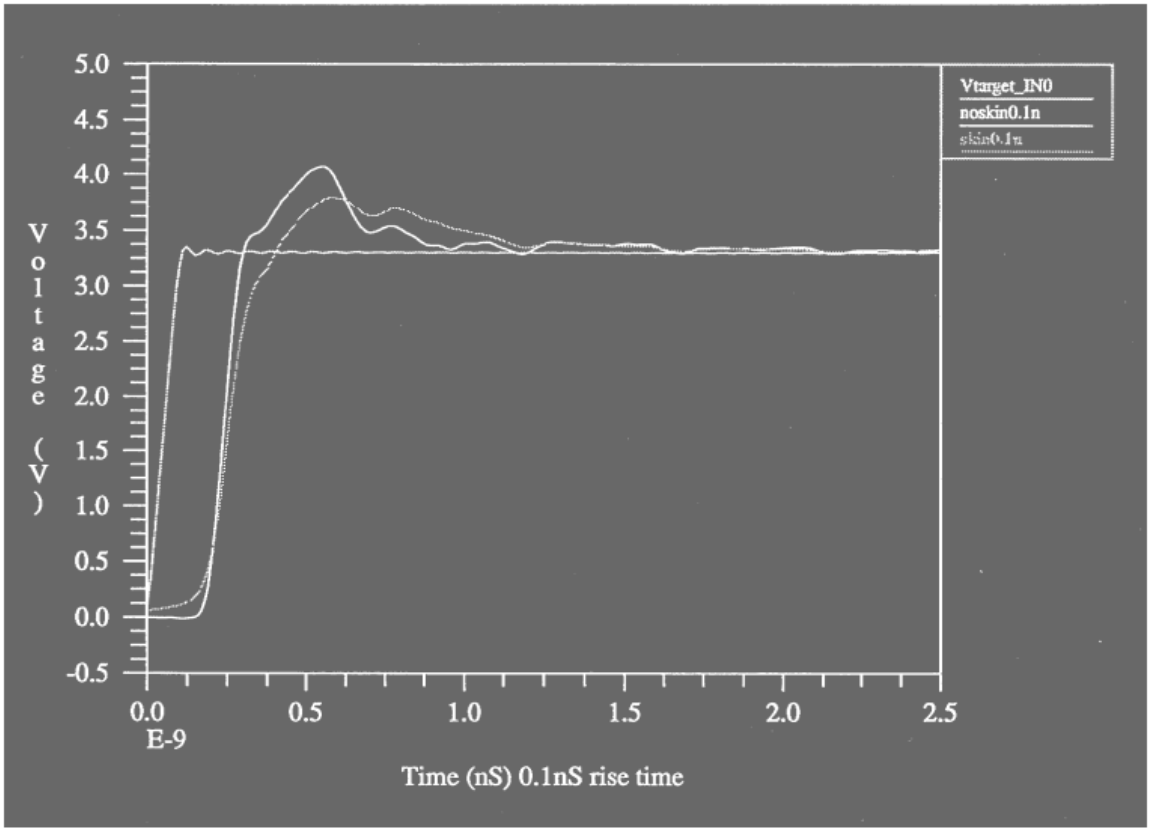


Skin effects are a concern that has been voiced by many engineers. Figure 28 illustrates that it is not a major problem for IC interconnects. Analyzing the formula shown for skin depth (sigma), we see that it is equal to the square root of 2 divided by frequency, magnetic permeability and conductivity. Upon analysis, it can be shown that skin depth is inversely proportional to the square root of the frequency. The analysis shows three typical metals used in silicon IC processes, copper, aluminum and titanium. As can be seen, the skin depths at 100 MHz are large at 6.2 microns for copper, 8.2 microns for aluminum, and 32 microns for titanium. At 1 GHz the values are still large when compared to process thicknesses at 2.1 microns for copper, 2.6 microns for aluminum, and 10.32 microns for titanium. The skin depths do not approach typical process thicknesses until after 5 to 10 GHz. For instance at 10 GHz the skin depth for copper is 0.63 microns, 0.8 microns for aluminum and 3.2 micron for tungsten. One can safely assume no frequency related skin depth problems up until 5 to 10

GHz. Therefore, one needs only to be concerned about frequency related skin effects in the order of 5 to 10 GHz.

Figure 29: Transient Response with and without Skin Effect

Time Domain → Frequency Domain → Time Domain

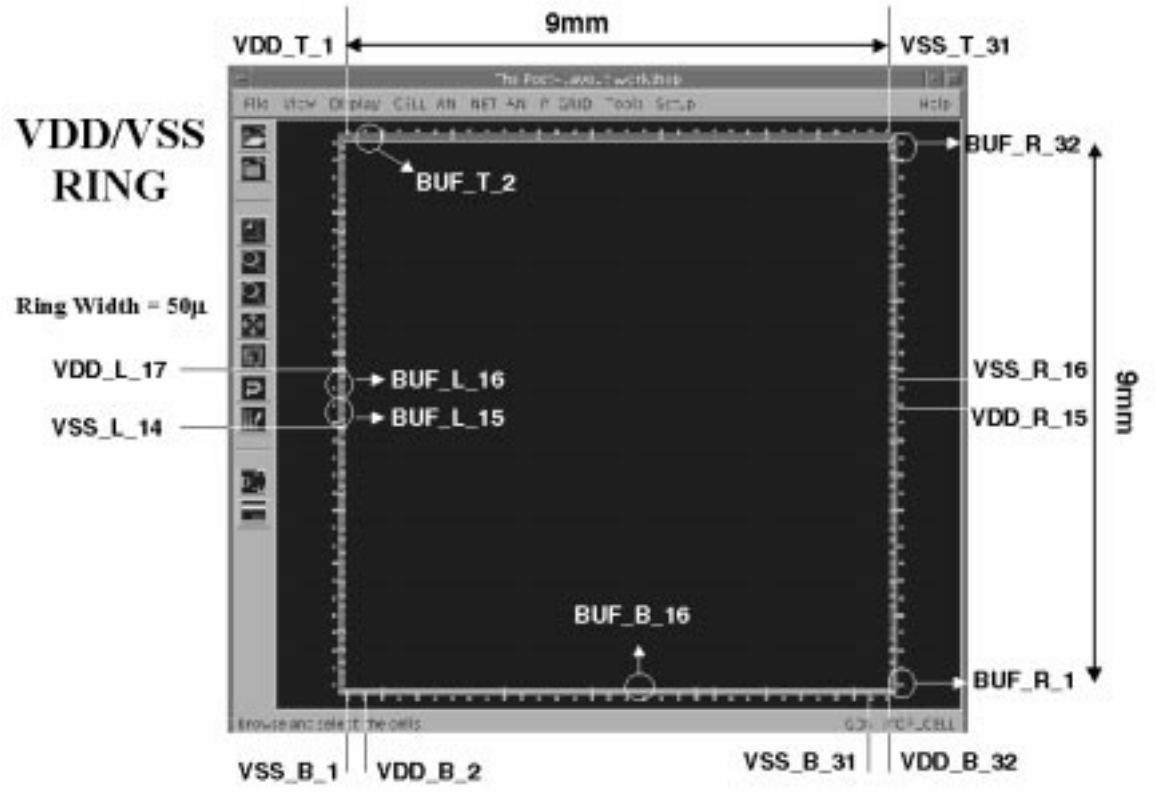


One might argue that it is not just the operating frequency, but the harmonics of the rising edge to be concerned about. To test this theory, in Figure 29 we looked at the transient response of a pulsed signal with and without skin effect considered in the simulation. To accomplish this we used a Fourier analysis that was a time domain converted to frequency domain converted back to time domain simulation. What can be observed was that the waveform without skin effect had a higher overshoot of around 0.3 volts and was significantly faster at the top of the voltage curve. However, at the trigger point of half of the voltage level, it was only slightly faster. Using this observation, it can be concluded that for digital signals including the harmonics in the consideration of frequency effects is not that important.

9. Inductance Effects on the Chip Equalization Ring

Figure 30 shows a typical VDD/VSS I/O equalization ring pair and the numbering scheme used by the OEA RING Designer tool. We have already determined earlier that inductance in wide lines can be a problem. The widest lines on the chip are normally on the VDD/VSS

Figure 30: RING Designer Orientation



equalization ring, which is located at the periphery of the chip. The system power is supplied to some of the connected pads through the package and bond wires that have a relatively high inductance. Many input/output buffers are connected to the ring, many of which may start to switch simultaneously. Problems may arise when the paths from the nearest VDD/VSS voltage supply pad and the input/output buffers gets too large and the rail voltage collapses because of the fast switching speed and the delay caused by inductance in the rail. The main question one might have is how many buffers can you put in between. A different and incorrect result will be obtained if you ignore the inductance effects.

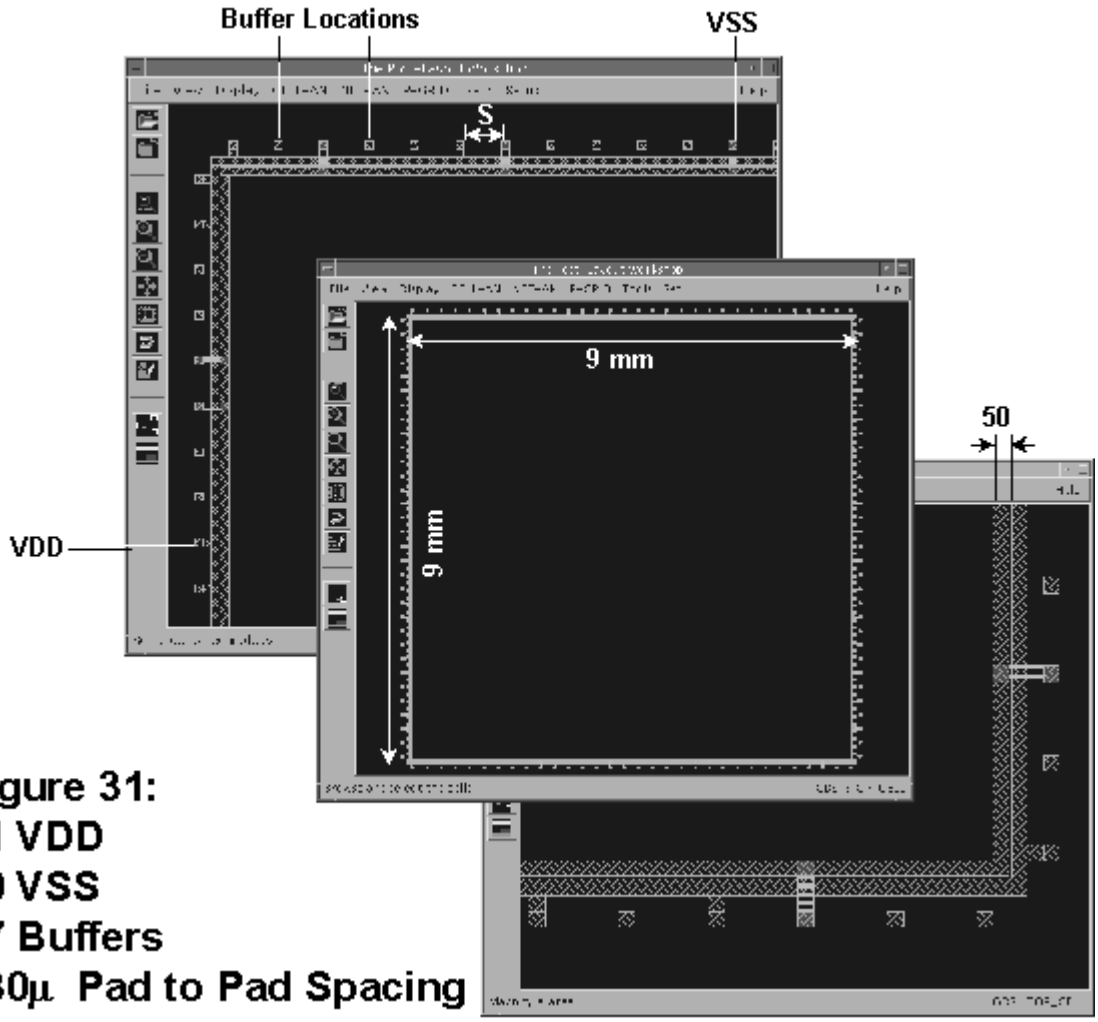


Figure 31:
31 VDD
30 VSS
57 Buffers
230µ Pad to Pad Spacing

To illustrate the potential problems on the I/O ring, the example shown in Figure 31 shows 50 microns wide VDD/VSS equalization rings, on a 9mm chip, with 210 microns of separation between buffers. For system supplied power, 31 VDD and 30 VSS pins are applied to the rings. In addition, 57 buffers are placed on the ring, all of which switch simultaneously. For proof of the ring inductance causing problems, the VDD/VSS pins will be tied directly to the ideal power supply with no bond wire or package inductance.

Figure 32: Buffer Supply Voltages

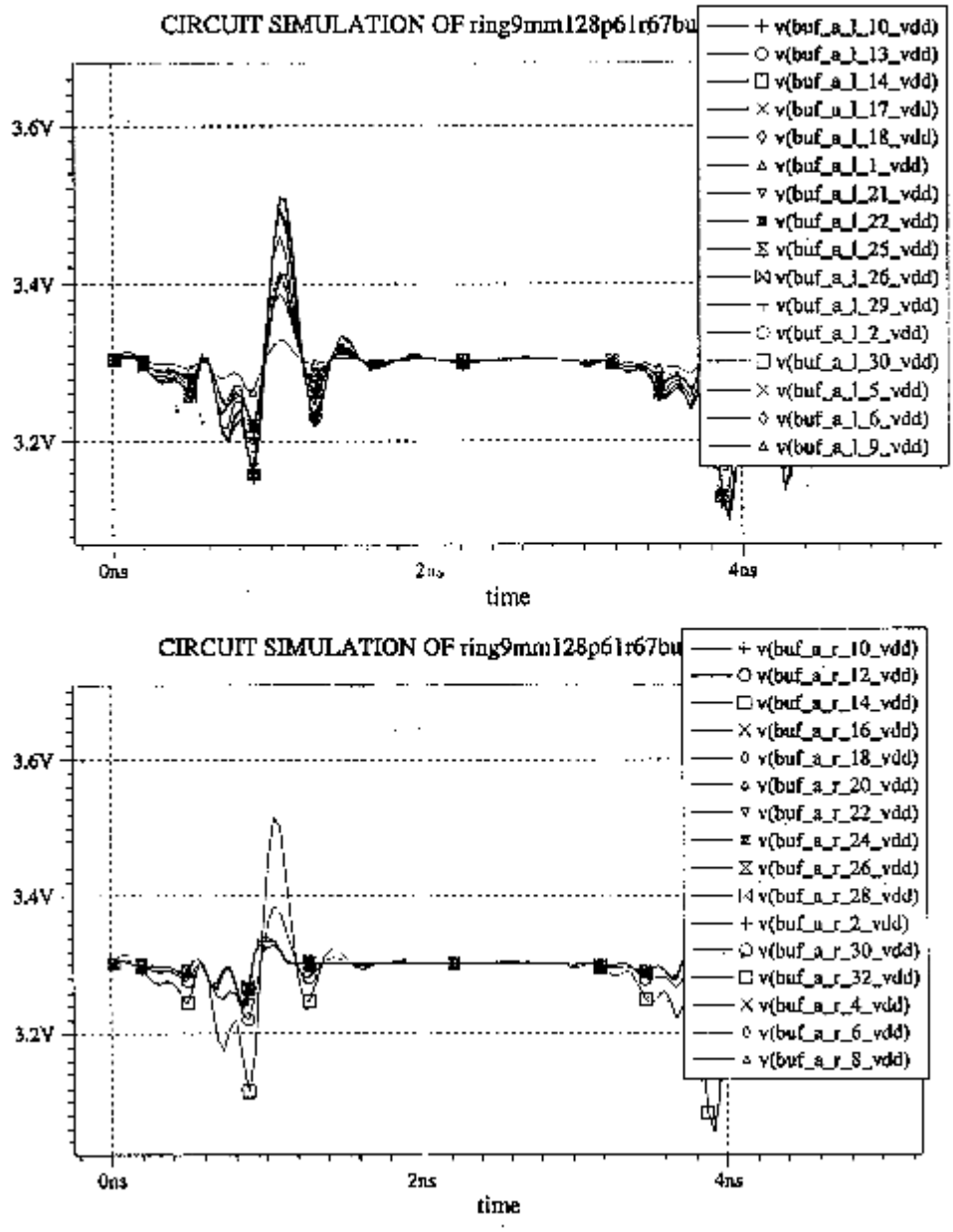


Figure 32 shows the resultant VDD voltage at various buffer locations on the right and left side of the chip when they are all switched simultaneously. The first observation is that there is a ground bounce effect due to the inductance and that they are not all the same. Therefore, the buffer position relative to the voltage supply pins makes a difference. The second observation is the bounce of 0.2V positive and approximately a little bit more on the negative side. This bounce is due to the inductance in the rings and there is not much that you can do about the bounce except add more VDD/VSS pins to decrease the average distance to all the buffers.

Figure 33: Buffer Supply Voltages

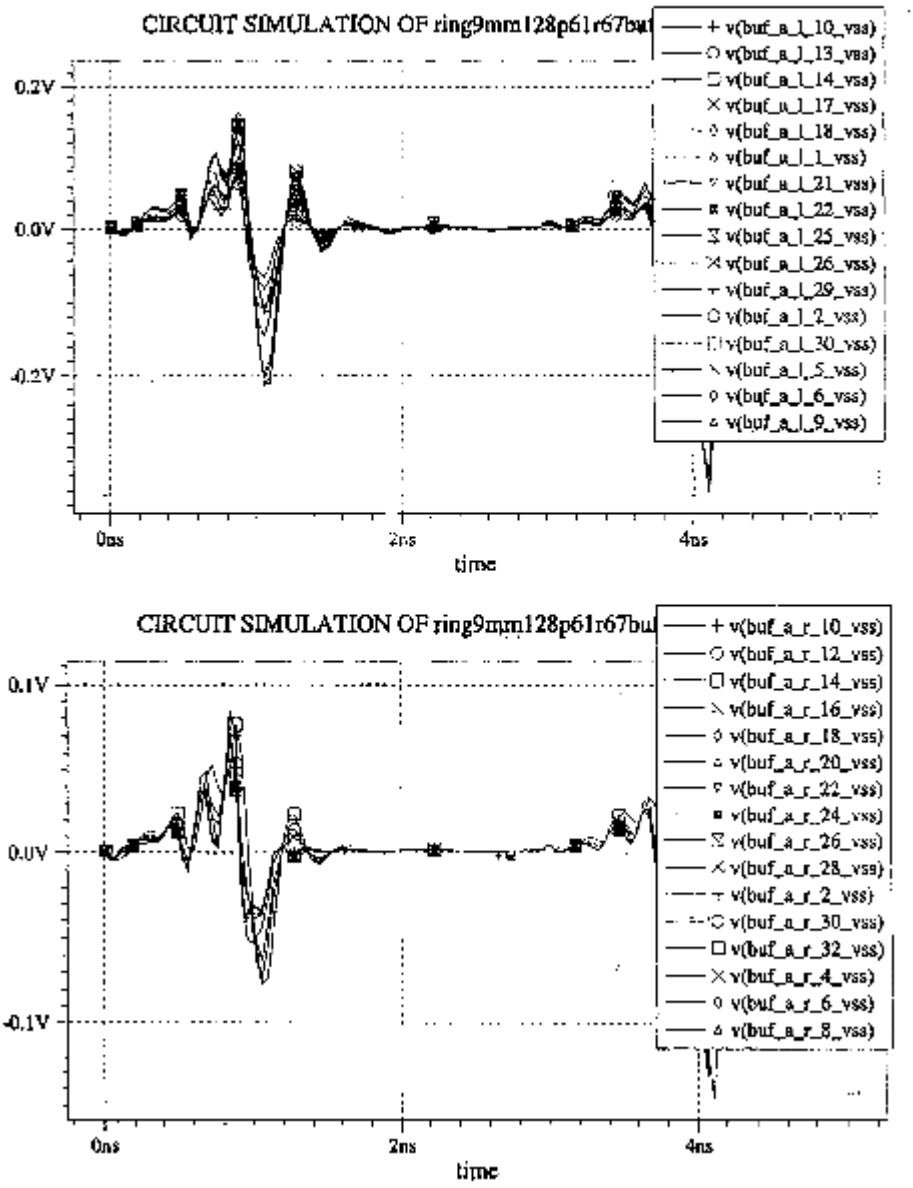


Figure 33 shows the resultant VSS voltage at various buffer locations on the right and left side of the chip when they are all switched simultaneously. Again, a ground bounce of nearly 0.2V is seen due to the inductance effects.

Figure 34: VDD/VSS Pad Currents

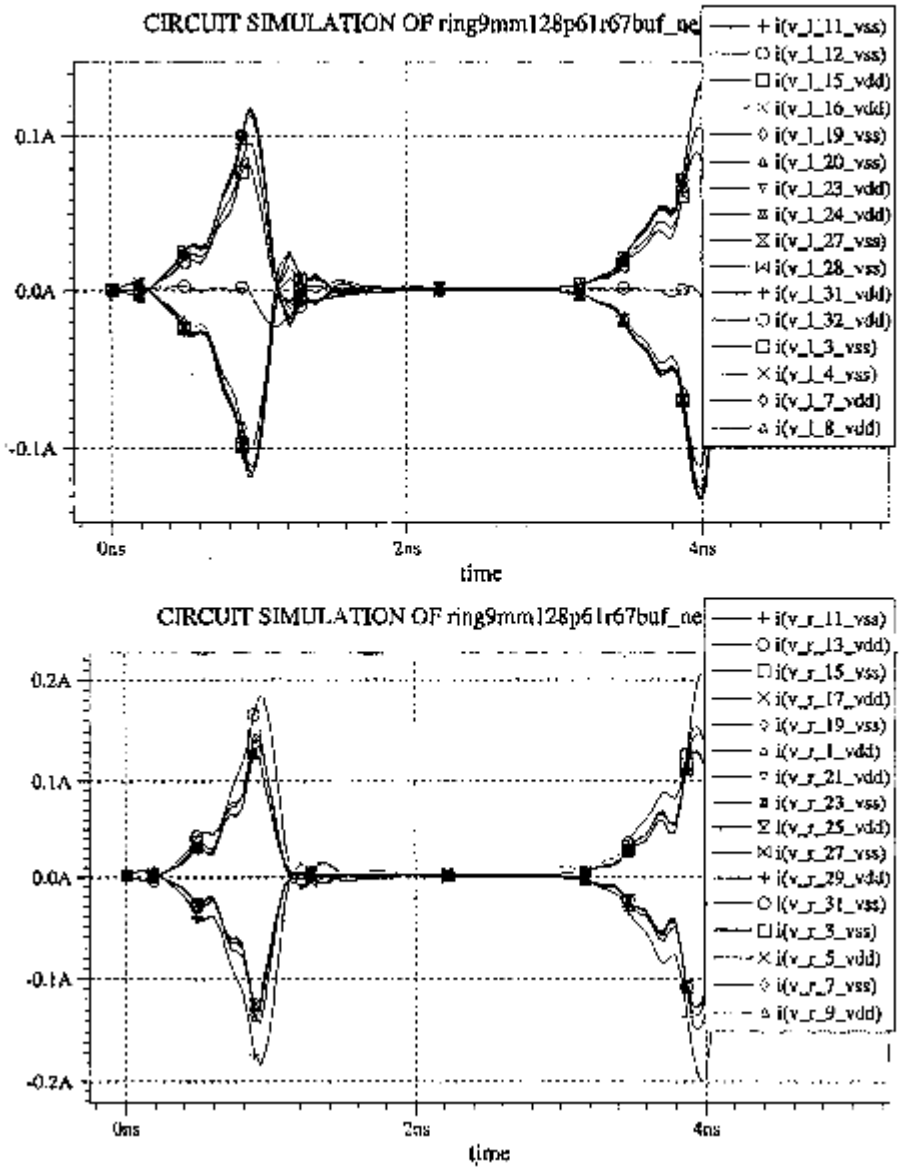
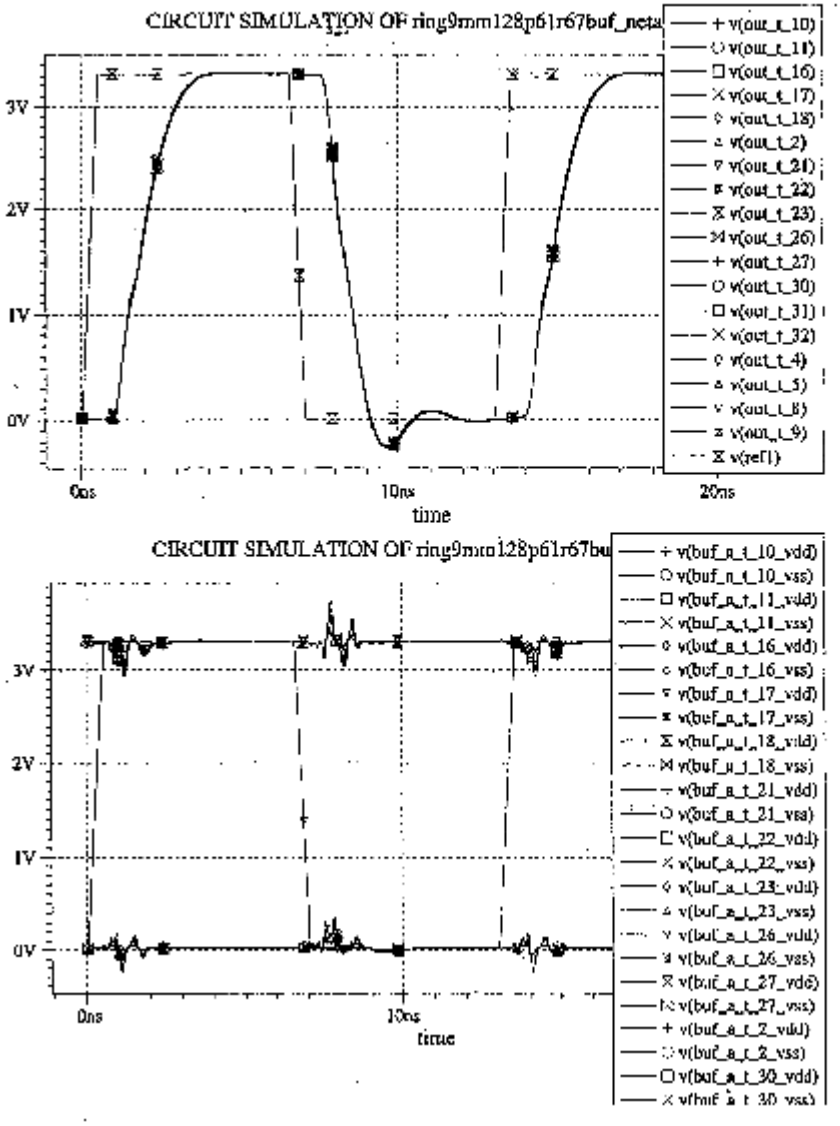


Figure 34 shows you the current at the buffer pad locations, which is the cause of the ground bounce. The current draw typically is approximately 100 to 200 mA at the VDD/VSS pins at the various buffer locations.

Figure 35: Buffer Output Wave-Forms



Driver Size
400X

C_{Load} =50 pF

Figure 35 illustrates the output waveforms for buffers along the top of the example simulation when the buffers are diving a 50 pF load. The delay of the buffer that is driving the current is a function of the capacitance load you are driving. This example shows a 400X driver. The top waveforms show the input signal and the output waveforms. Notice in the lower waveforms, the ringing of the VDD line and VSS line with no package inductance. The ringing is due only due to the on-chip inductance of the VDD/VSS equalization ring.

10. Effective Inductance in the Core Power Distribution Network

Figure 36: 4 Layer Metal, 10 mm x 10 mm, VDD / VSS Core Network

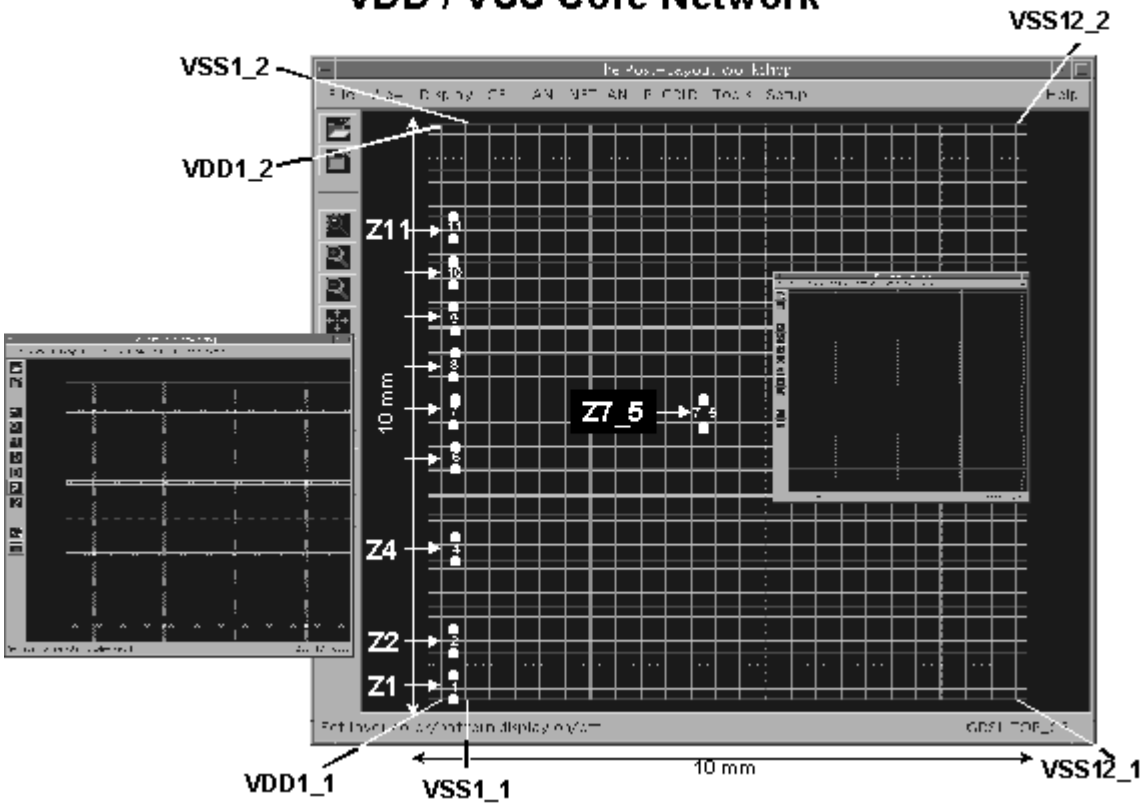


Figure 36 shows a four metal layer, 10 mm x 10 mm, VDD/VSS core power distribution network. The core power distribution network is normally a complicated matrix with alternating VDD and VSS lines in diagonal directions on different layers and tied together with vias at the common intersection points. In the example we have tied the end nodes on the top layer to the ideal system VDD/VSS supplies to eliminate the effects of the bond wire and package inductance on this experiment. Buffers are located at the "Z#" locations at various places on the chip. The example is set-up to show the impedance between these VDD/VSS pins seen by the buffer at various locations of the chip. Once that is determined, the power and ground bounce at the buffer locations can be simulated accurately.

Figure 37: The Distribution of Impedance, Effective Inductance (Leff_M) and Effective Inductance without Mutual Inductance (Leff) at Various Location on the Power Distribution Network.

Values calculated at 100 MHz with 24 VDD and 24 VSS Pads

VDD_NODE	VSS_NODE	Location of buffer X	Y	Z_real	Z_imag	L_eff (nH) with M	L_eff (nH) without M
VDD_Z1	**VSS_Z1**	**490**	**1**	**5.81**	**0.32**	**0.51**	**0.86**
VDD_Z2	VSS_Z2	490	801	5.45	0.49	0.79	
VDD_Z4	VSS_Z4	490	2401	5.62	0.62	0.99	
VDD_Z6	VSS_Z6	490	4001	5.55	0.66	1.06	
VDD_Z7	VSS_Z7	490	4801	5.51	0.67	1.07	1.14
VDD_Z8	**VSS_Z8**	**490**	**5601**	**5.68**	**0.66**	**1.05**	
VDD_Z9	VSS_Z9	490	6401	5.62	0.64	1.01	
VDD_Z10	VSS_Z10	490	7201	5.63	0.62	0.99	
VDD_Z11	VSS_Z11	490	8001	5.86	0.58	0.93	
VDD_Z5_7	**VSS_Z5_7**	**4498**	**4801**	**5.22**	**0.48**	**0.76**	**0.84**

Values calculated at 100 MHz with only one VDD and one VSS pad at opposite corners

VDD_Z1	**VSS_Z1**	**490**	**1**	**8.57**	**2.42**	**3.86**	
VDD_Z5_7	**VSS_Z5_7**	**4498**	**4801**	**7.99**	**2.73**	**4.35**	

Values calculated at 100 MHz with 24 VDD and 24 VSS Pads but with 2X wider metals

VDD_Z8	**VSS_Z8**	**490**	**5601**	**3.11**	**0.60**	**0.95**	

Figure 37 represents a table of various impedances and effective inductances simulated at various locations on the power distribution network shown in Figure 36 and under different conditions. Several of the results were simulated with and without mutual inductances to show you why mutual inductances are important and must be taken into consideration. All values were calculated at 100MHz with the measured locations tied to the bottom level of metal. The 24 VDD and 24 VSS input locations were at the periphery and tied to the top level of metal. The first two columns show the nodes that tie to the VDD/VSS network. The second two columns are the X and Y coordinates for which there is calculated impedance. The impedance is shown in both the real and imaginary parts.

At point Z1, we have 5.81 Ohms of real impedance and 0.32 Ohms of imaginary impedance and an effective inductance of 0.51 nH. If the mutual inductance effects were ignored, the 0.5nH of effective inductance would jump to 0.86nH of effective inductance. That is nearly a 70% increase in this case. Therefore, when calculating effective inductance on the on-chip, you need to include mutual inductance in the simulation.

Notice that points Z1 through Z11 show a symmetric behavior due to the increased distance away from the VDD/VSS pins. The value depends on the way currents flow and the length of the return path. As the pin location gets closer to the center, it is getting far away from the VDD/VSS pins, and therefore the inductance increases above 1nH in the center. Again, for Z7 at the center of the chip, if mutual inductance is ignored, the value jumps from 1.07nH to

1.14nH. This 6.5% jump is significantly less than the nearly 70% jump in location Z1. This illustrates that it all depends where the pin is and how the current distributes itself as a return path. If you observe at the Z7_5 location, there is an effective inductance of 0.75nH when you include mutual inductance and an effective inductance of 0.84nH when you do not include mutual inductance. In this case, there is a 12% difference, yielding further validity to the location theory.

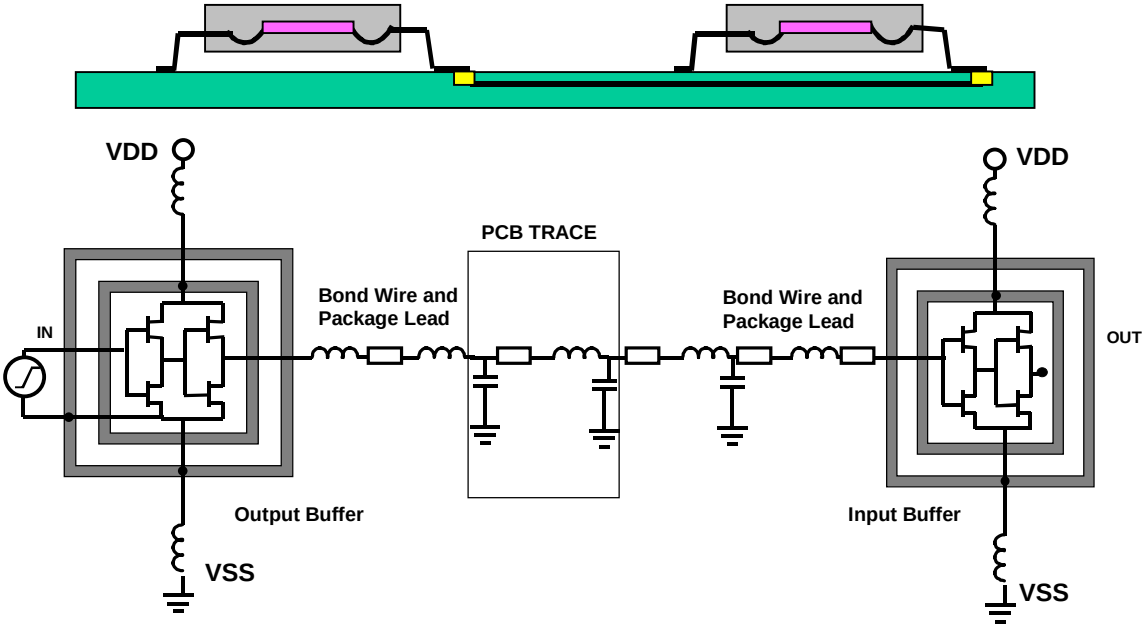
Now to show that the number of pins is important, in the second section of calculations in Figure 37, the 24 VDD and 24 VSS pads have been reduced to two, one at each corner. The effective inductance at Z1 jumps from 0.51nH to 3.86nH, almost an 8X increase. Comparing the Z7_5 location the effective inductance value jumps from 0.76nH with the 24 VDD and 24 VSS pins to 4.35nH with only one VDD and one VSS supply pin. That is often a higher inductance value than a bond wire.

What about the effects of core supply line widths? In the third section of Figure 37 there are the original 24 VDD and 24 VSS pads but the supply lines are made 2X wider. Earlier in the report, it was proven that wider lines would make a better Q inductor. With the 2X wide VDD/VSS rules, the real part of the impedance on Z8 drops from 5.68 ohms to 3.11 ohms, basically a reduction in resistance. The imaginary impedance value only drops from 0.66 ohms to 0.60 ohms. Therefore, you have a better Q inductor by increasing your power line widths by 2X. The resulting effective inductance value from the 2X wide lines simulation is 0.95 nH versus 1.05 nH. Although the effective inductance value was reduced, it made a slightly lower inductor value, but it made a better inductor with a higher Q.

As a result of this section's analysis, it can be concluded that the VDD/VSS pin locations and the number of supply pins are very important in determining the core on-chip inductance values which are seen at the buffer locations the VDD/VSS supplies. Using the OEA tools, the correct number and location of VDD/VSS supply locations can be determined. Pad location current balancing can be evaluated and the effective inductance to any point on the chip can be calculated for on-chip bus simultaneous switching noise and ground bounce analysis.

11. Off-Chip Inductance Path Analysis

Figure 38: Signal Path from Chip to Chip



Inductance effects can be extended off chip to do a complete model for system analysis or chip to chip communication. A complete model can include a VDD and VSS ring, on-chip buffer models and interconnect, bond wire and package lead models and a model for the PCB trace. This model can include the signal as well as the VDD/VSS path. OEA tools can be used to build this complete model.

12. Conclusions

On-chip inductance is a real phenomenon. It is real and you cannot ignore it. The effects of inductance and mutual inductance, whether or not they are important for on-chip modeling are very dependent on a number of factors including interconnect length, width, and frequency.

The general guidelines for inductance are as follows:

- Long and wide lines have to be modeled including inductors in the model.

- Mutual inductance coupling is real and significant on chip when calculating bus line and signal effective inductance return paths. There were 30% to 50% changes in inductance values depending on how inductance was modeled and which effects were included.

- Inductance effects on long wide lines can be avoided by segmenting or splitting the lines into segments that are less than approximately 4 mm. The actual length will depend on the technology, clock speed, width and other factors. Rules need to be simulated for each case. OEA tools can be used to generate these rules.

- Modeling I/O equalization rings and VDD/VSS lines with the on-chip inductance effects included is necessary to predict simultaneous switching noise and ground bounce effects. OEA has seen large fluctuations, approximately 6 Amps current spikes, for on-chip VDD/VSS when you have a very large on-chip bus structure. A 1024 wide bus that is simultaneous switching will definitely cause a bounce where your bus drivers are located if not properly tied. For situations such as that, one has to take into consideration fully coupled VDD/VSS network with the bus lines, with the non-linear (Spice model) of the buffers to do a realistic analysis.