RING Designer™

VLSI Power Distribution Ring Design Tool

OEA International, Inc.

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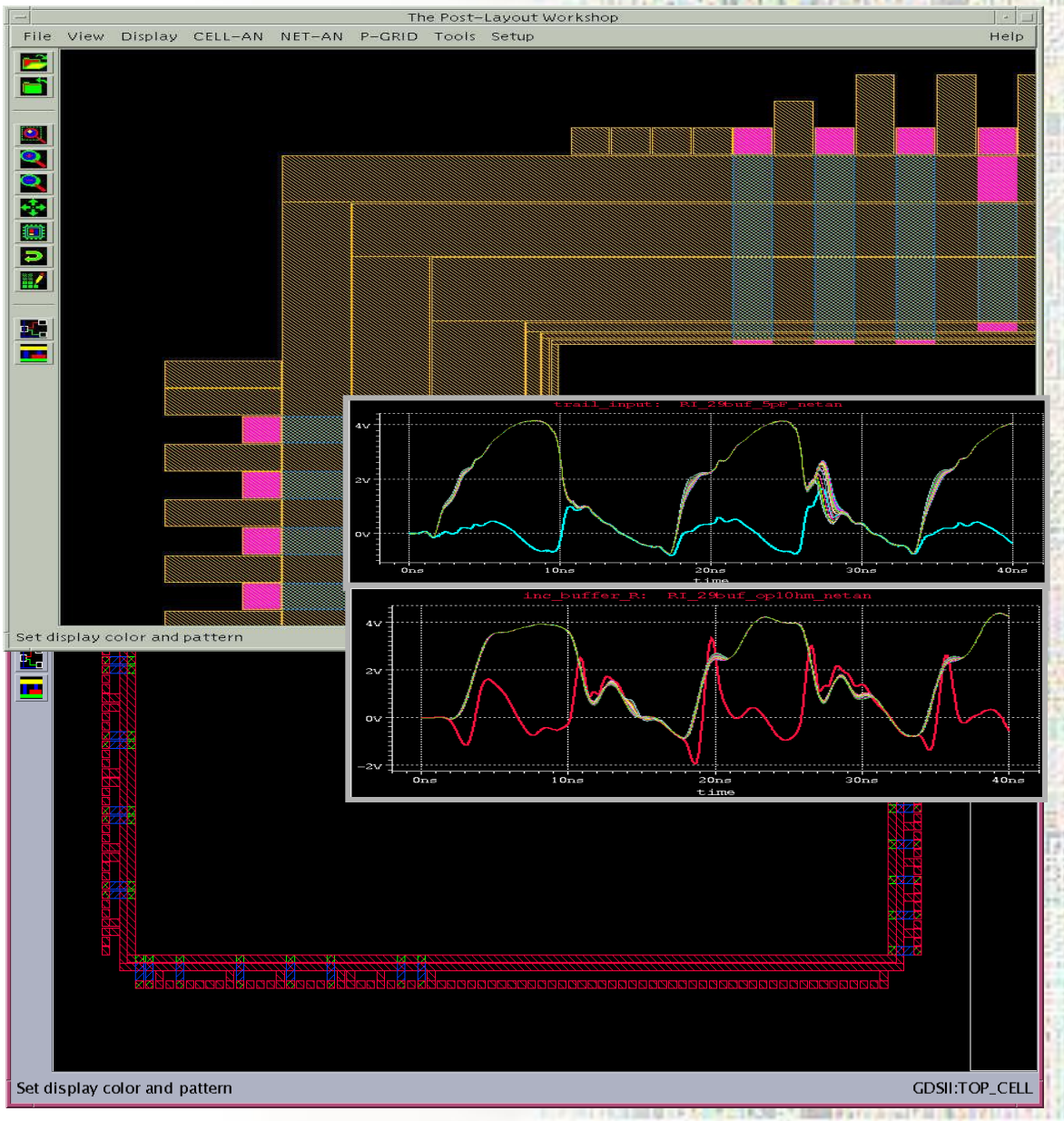
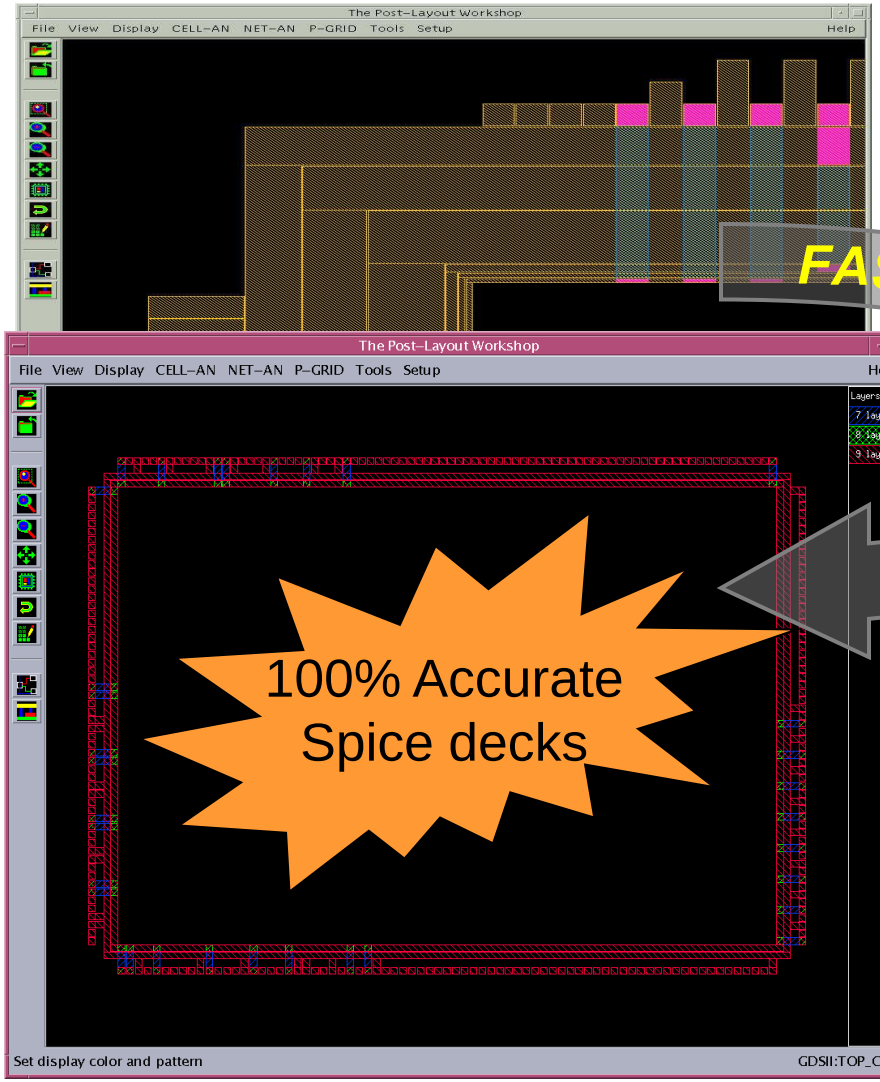
RING Designer Features

- Solves the problem of generating accurate Spice decks to analyze IO rings with packaging effects
- Helps with the optimization of power pin placement on complex IO ring designs
- Analyzes potential ground bounce and simultaneous switching noise problems
- Analyzes and assists in balancing current loads to I/O pad and voltage input pads
- Includes all ring and packaging inductance parasitics



Fast and Easy What-if Analysis for Optimization of IO Placement

RING Designer

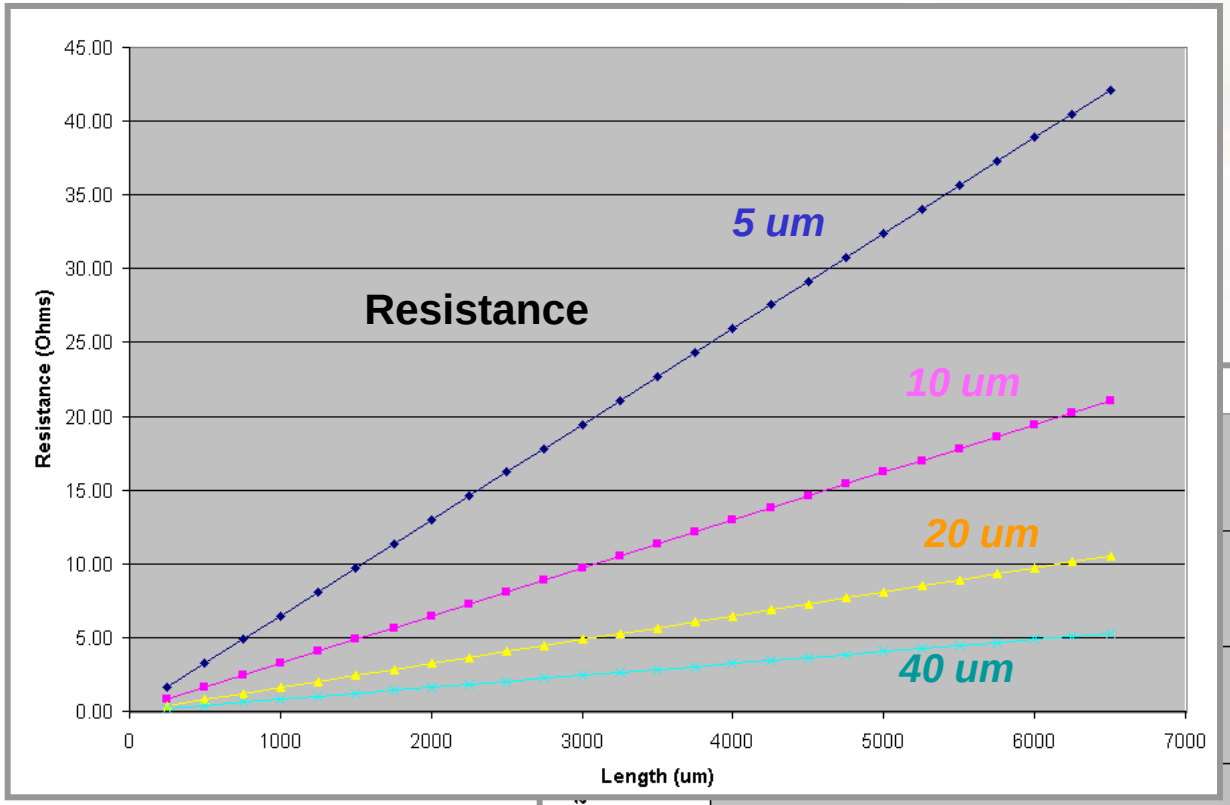


FAST CYCLE TIME

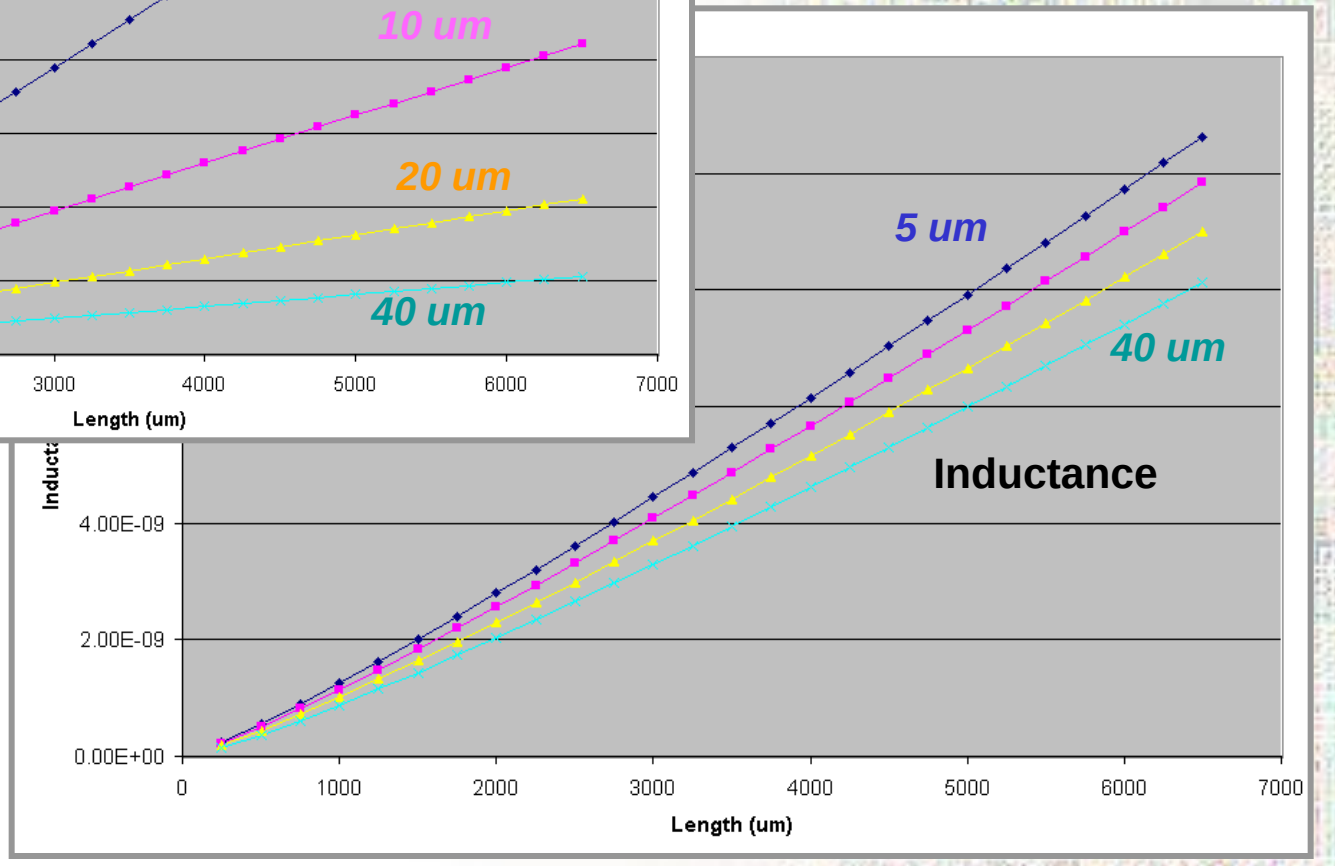
NET-AN Extraction & Spice

- **Analyzes Voltage Source and I/O Placement for Ringing & Simultaneous Switching Noise**
- **Uses full RCLM Ring & Package Parasitics for SPICE Analysis**

Why is it important to include inductance in IO analysis?

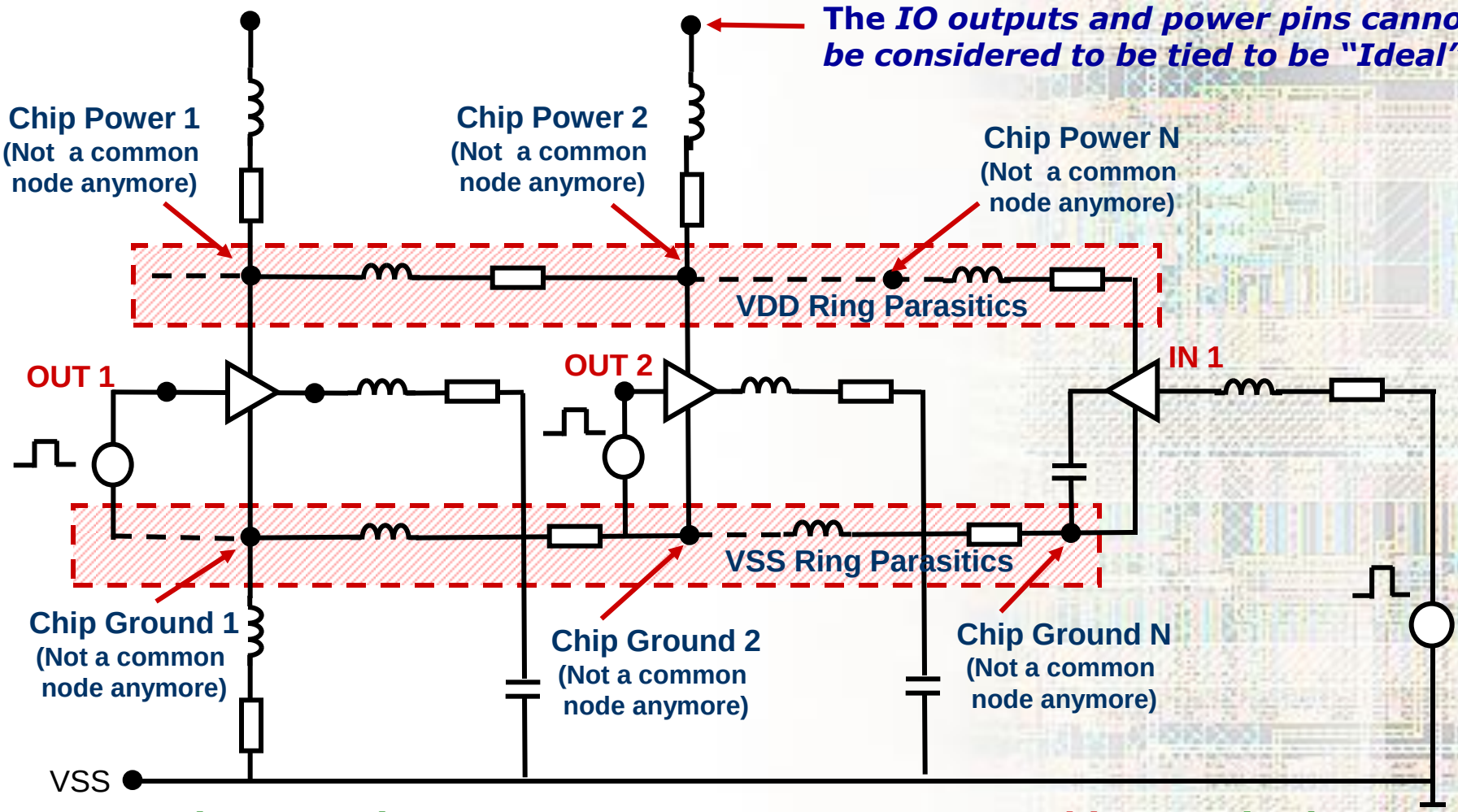


Ring Resistance and Inductance With Relation to Width and Length



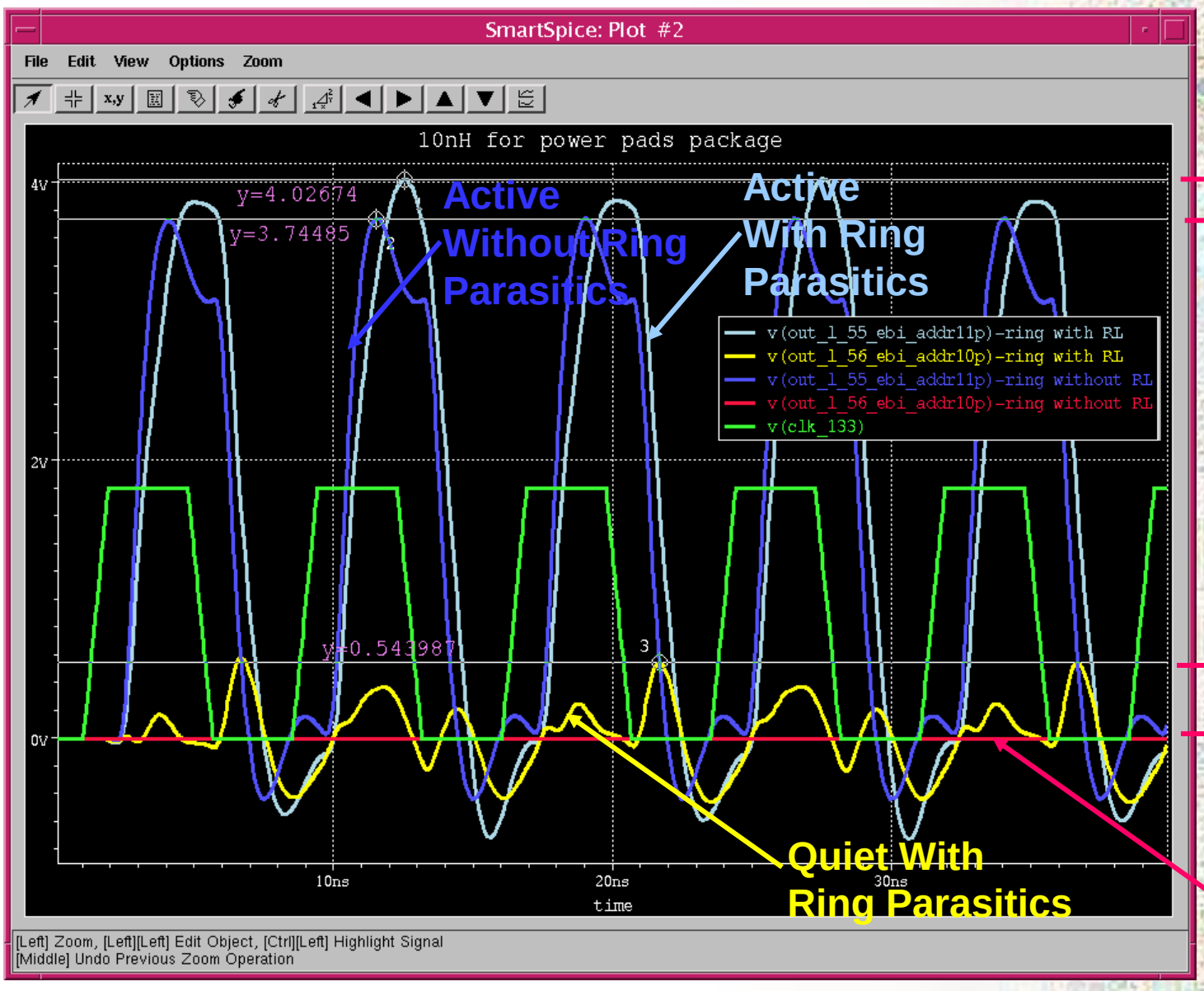
$$Q = \frac{L 2\pi f}{R}$$

The Origin of Ground Bounce and Simultaneous Switching Noise



- **Impedance to the power sources can cause ground bounce in the voltages tied to the IO pins**
- **Impedance in the rings between the IOs cause noise in the voltages supplied between switching IO pins.**

Comparison of Noise and Signal Integrity With and Without Ring Parasitics

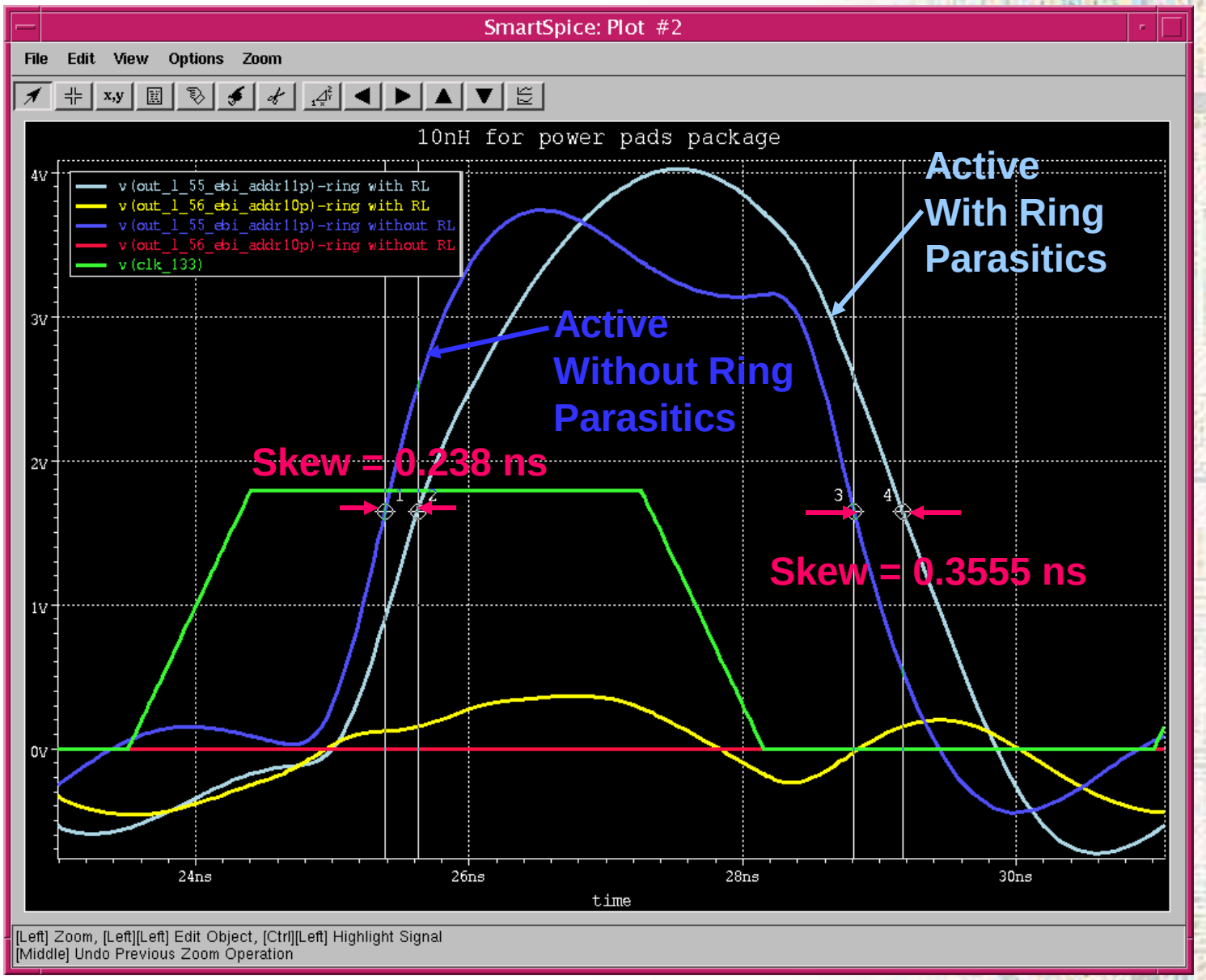


0.28 V

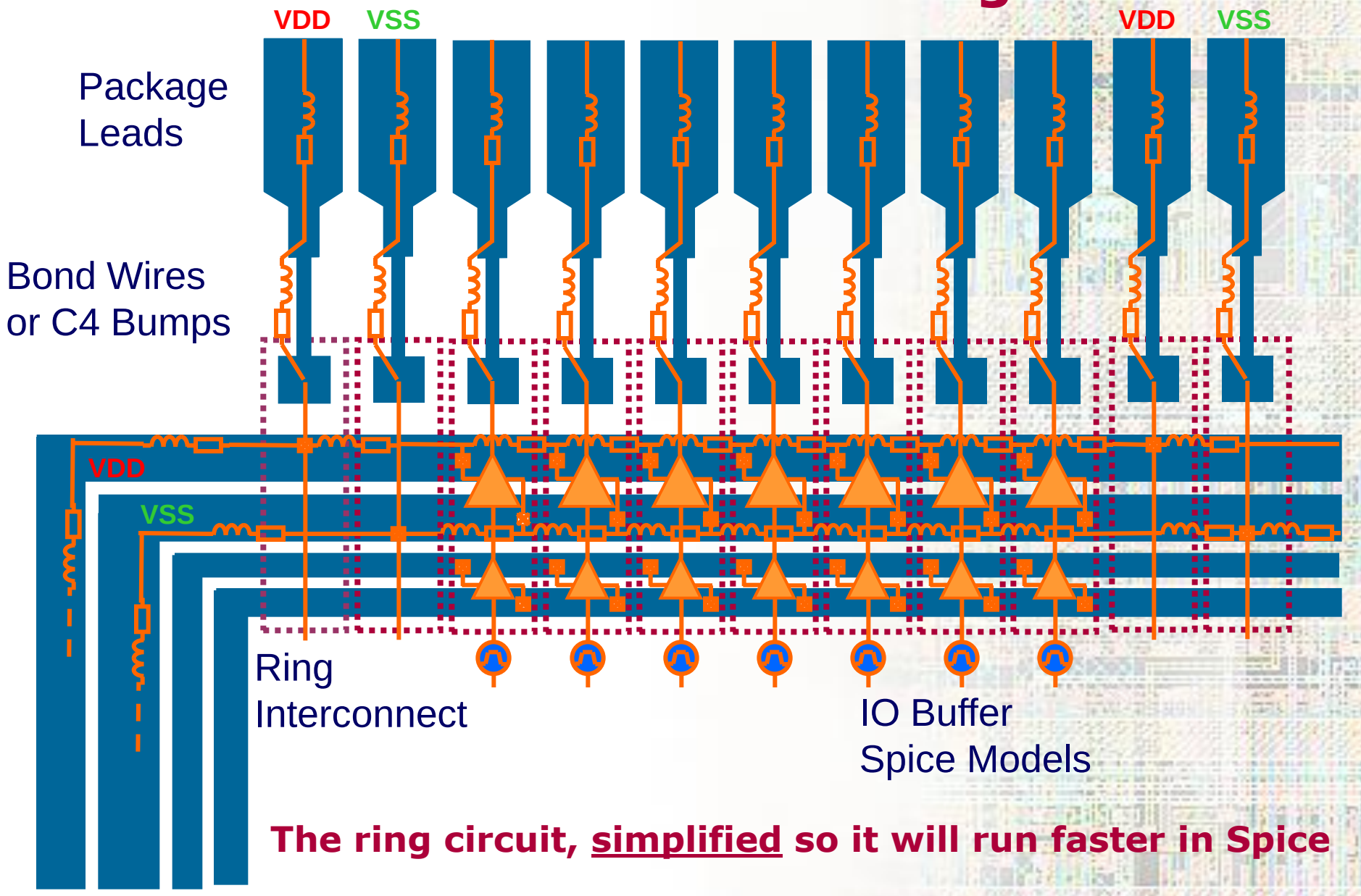
0.54 V

Quiet Without Ring Parasitics

Comparison of Skew With and Without Ring Parasitics

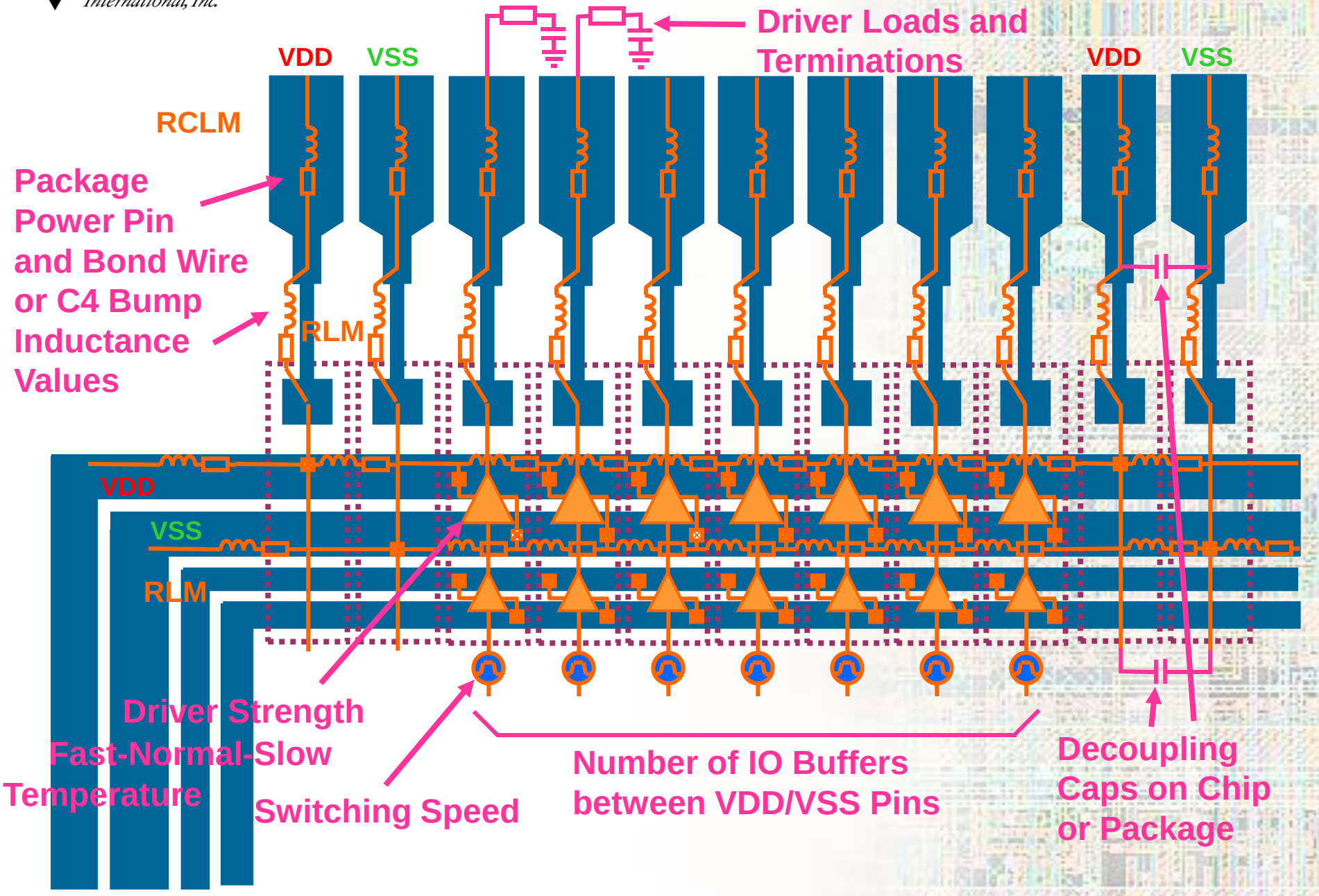


Modeling Elements of the Basic IO Ring



The ring circuit, <u>simplified</u> so it will run faster in Spice

SSN and Ground Bounce Factors



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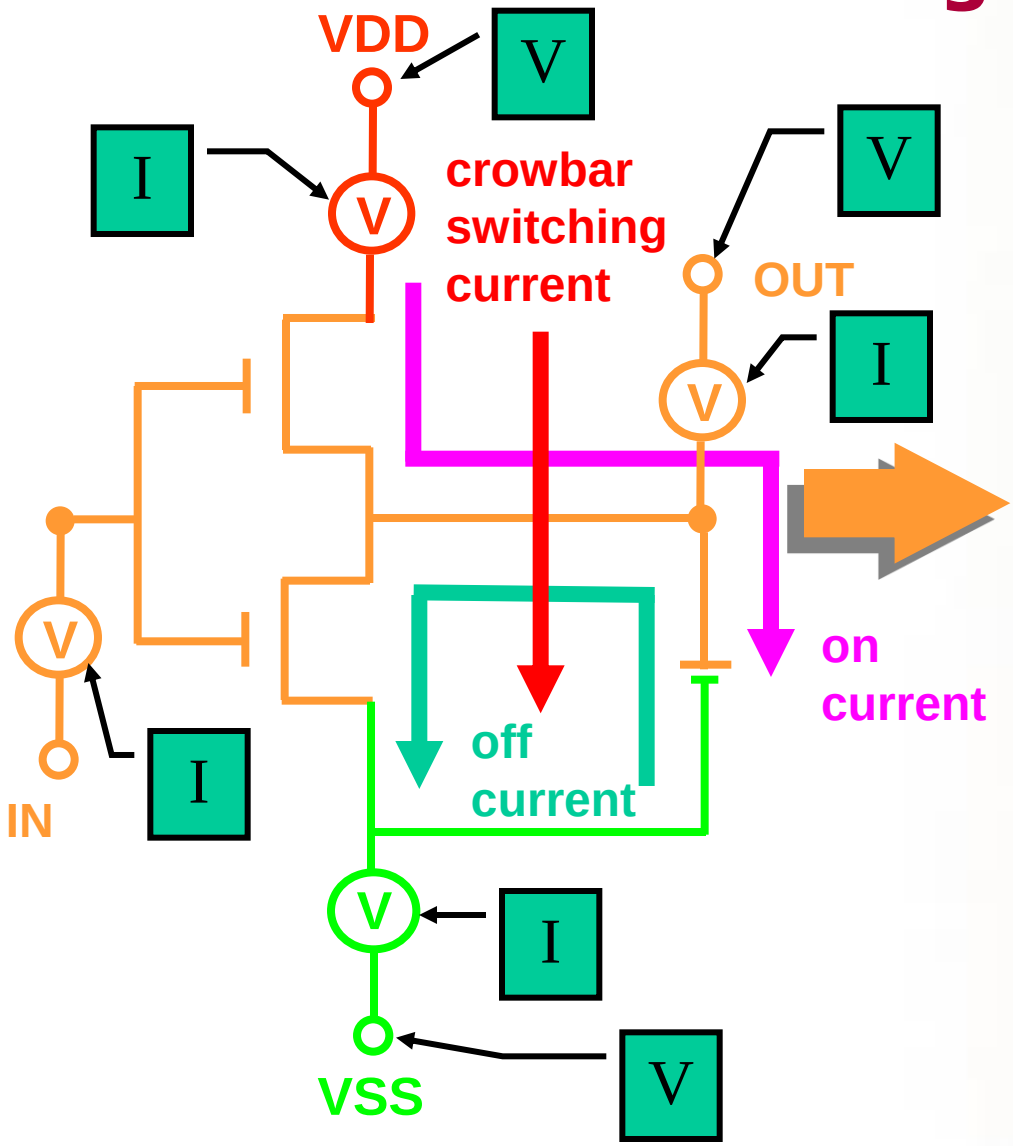
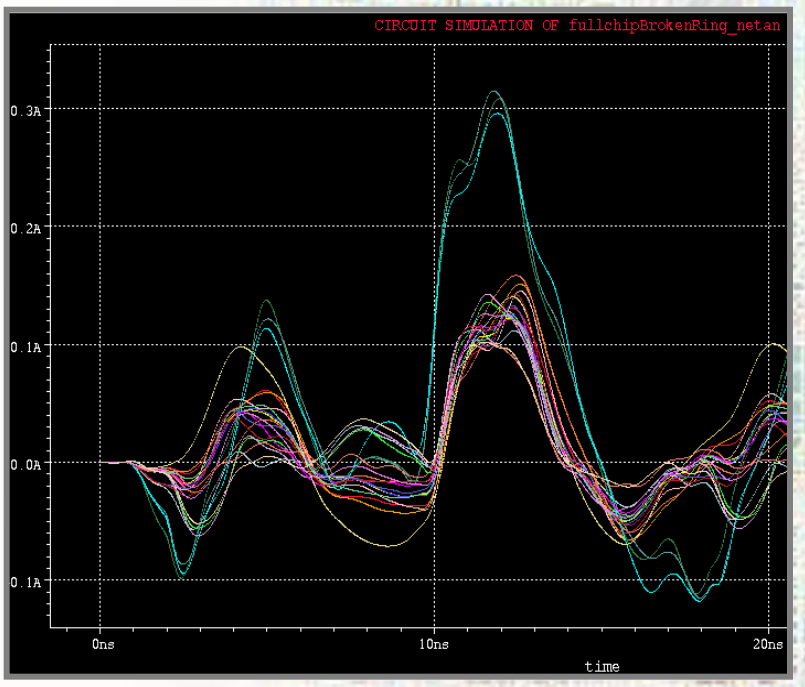
A Practical Approach to Analyzing the IO Ring

- **Build and Simulate a Spice model of the IO ring including:**
  - Accurate but Simplified Ring Parasitics
  - Significant Package Parasitics and Terminations
  - Full Spice IO Buffer Models
  - Lots of Measure Statements for all Outputs and Power and Ground Voltages and Currents
- **Simulate in Spice and Analyze Results**
- **Modify and Iterate until all the problems are solved**

Lots of Measure Statements are Needed to Monitor all IO Buffer Voltages & Currents





Example Showing Output of VSS Currents at Various Locations

Analysis Flow using RING Designer

Step 1
Gather the data and prepare the input files.

- Ring Designer Input
- IO Buffer Library
- Package Library

Step 2 Run RING Designer

- Generate 3D Geometry for Ring
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- Extract Parasitics

Step 3
Run Spice on the Master Circuit

- Build Spice Master Circuit
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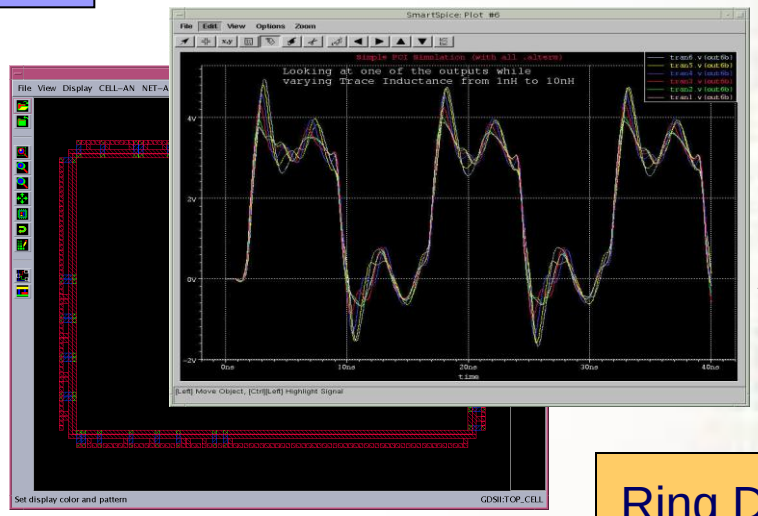
- Simulate in Spice

Step 4
Evaluate Results

- Evaluate Spice Output
- View Spice Waveform Output

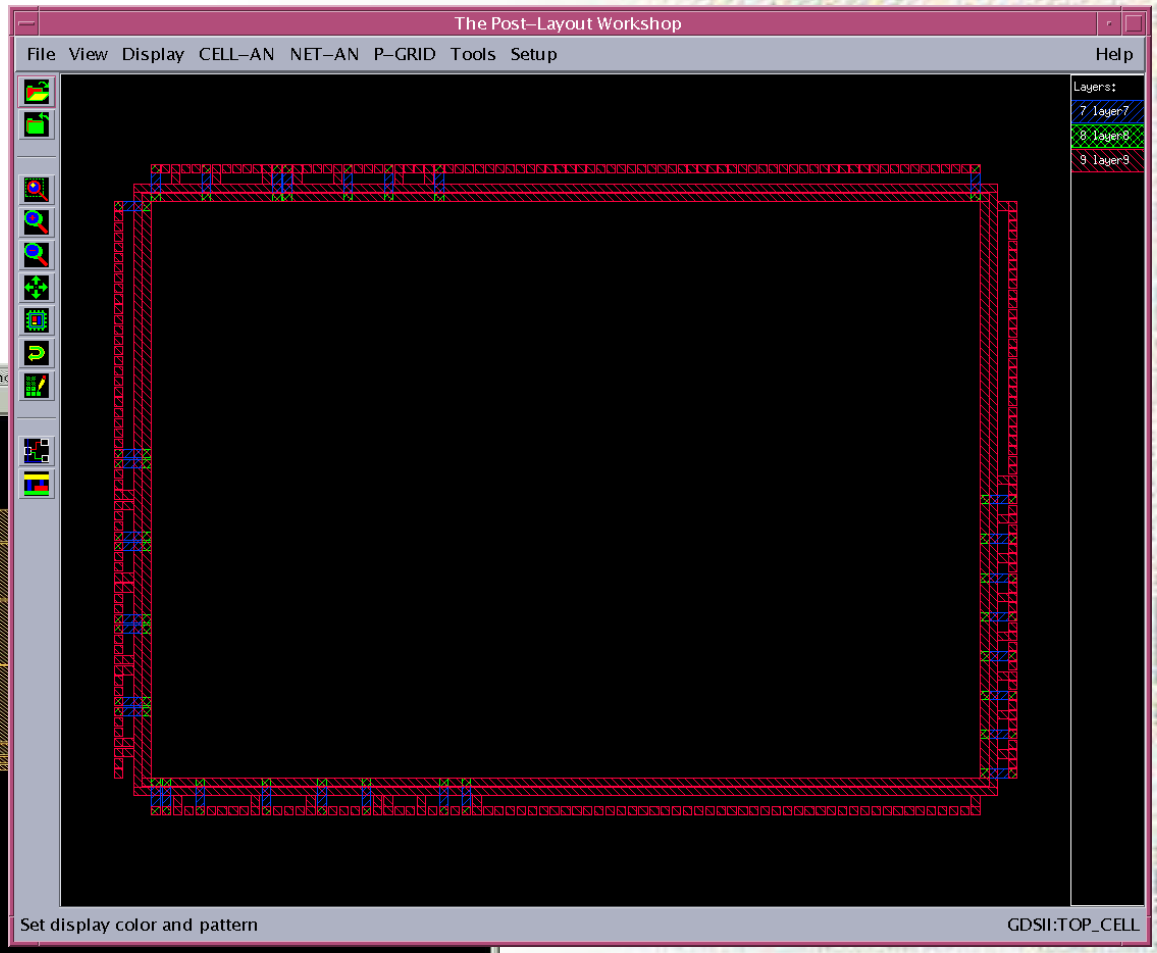
Step 5
Repeat if Necessary

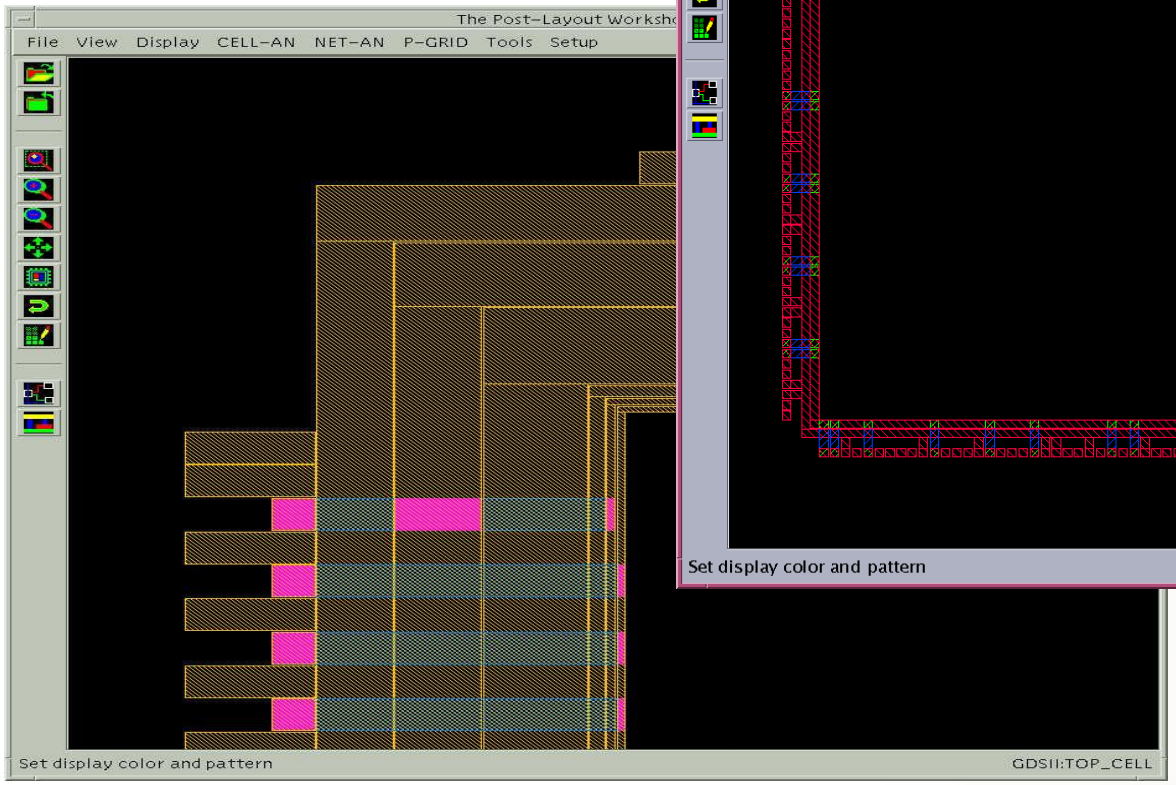
- Modify Input and Iterate



IO Ring Geometry Generated and Parasitics Extracted

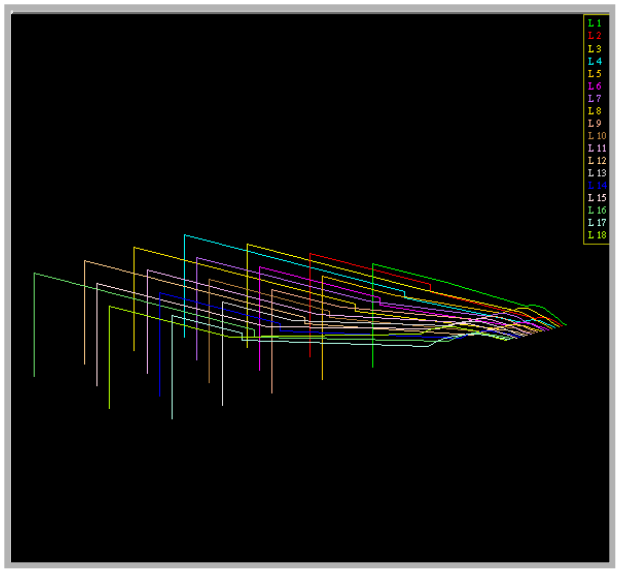
Structure is Simplified for Accurate but Faster Spice Simulation

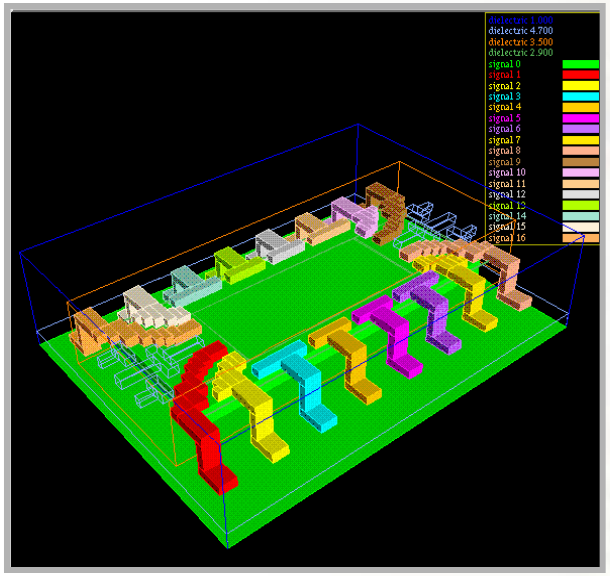


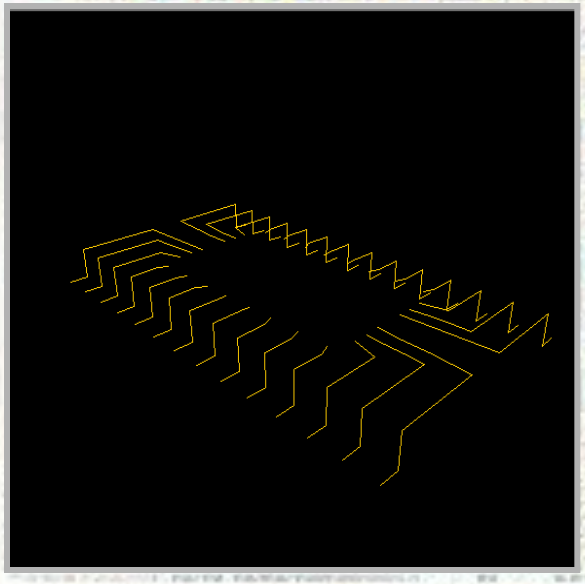


OEA *Ring Designer* generated data

Package Parasitics Can be Extracted, Obtained from Measurements or Acquired from the Vendor

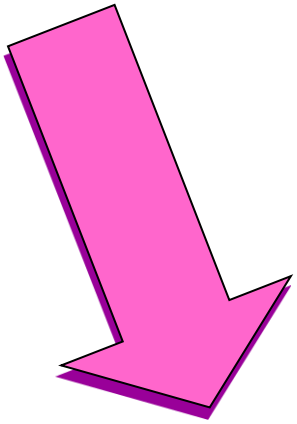


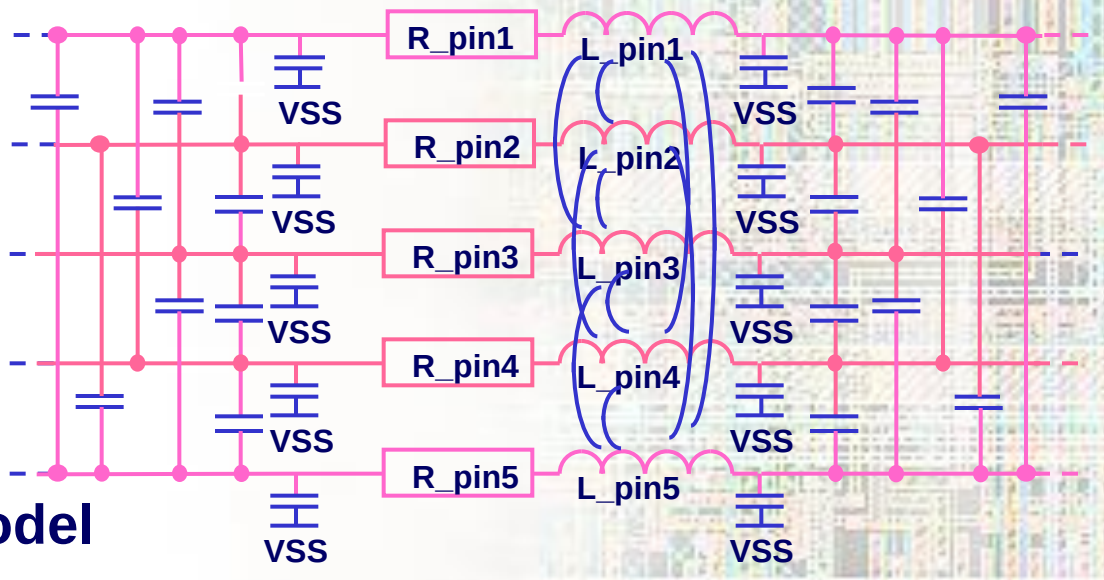




Graphic Models

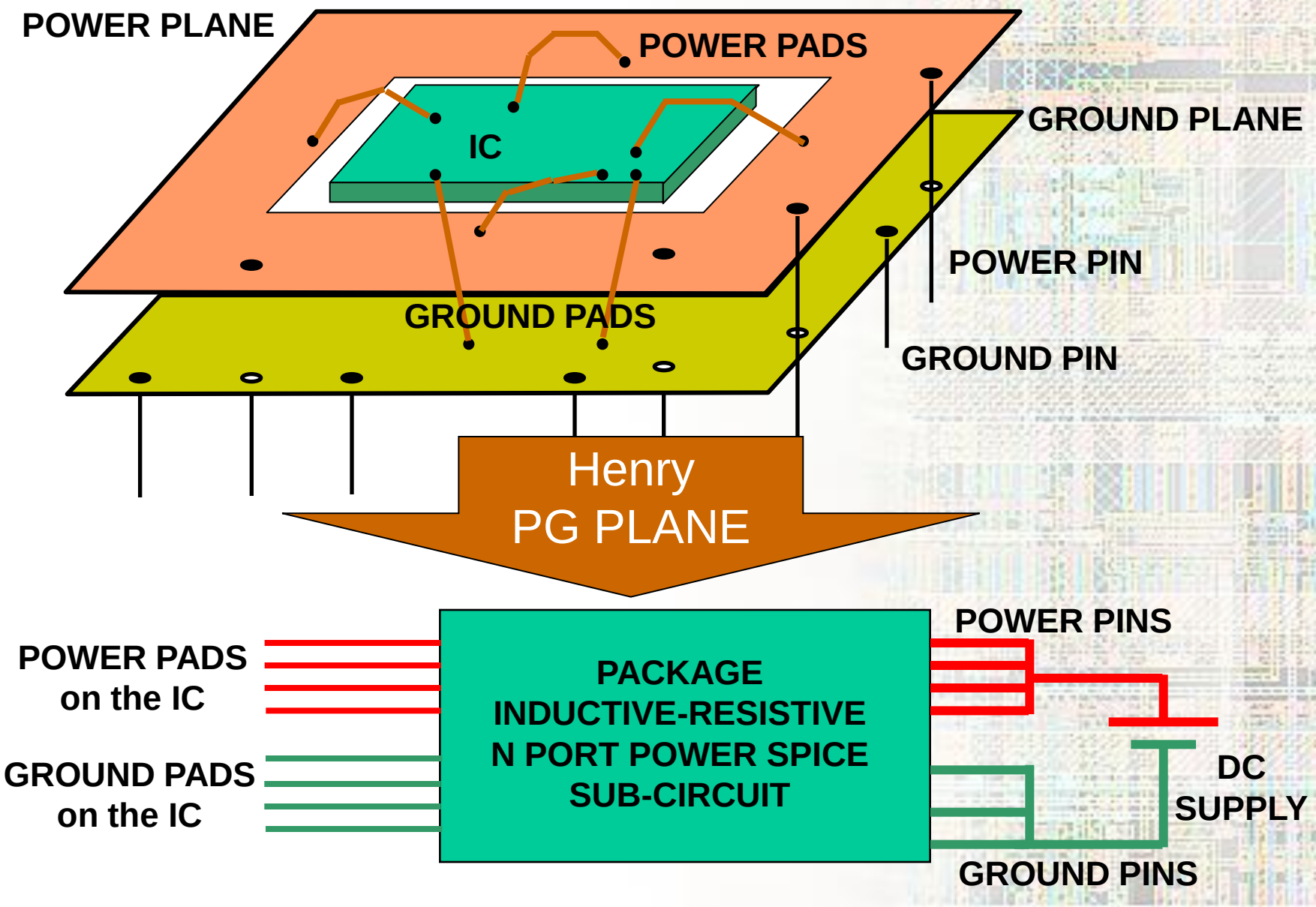
HENRY and METAL RCLM Extractors





RCLM Spice Model

Package Plane Models are Important for Simulation of Return Path Currents



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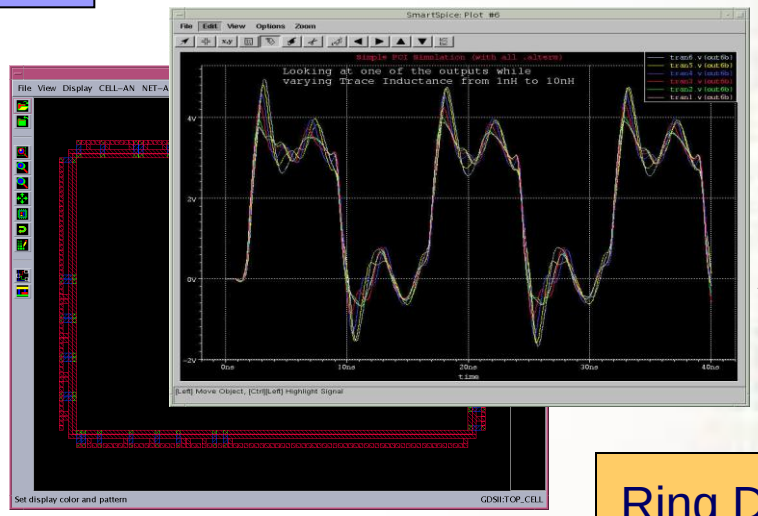


A Real Design Example

Pre-routing pin placements with estimate package parasitics

Package Pins

Power Pins

L=2nH, R=0.01Ω

Output Buffers

L=5nH, R=0.01Ω, C=10pF

Input Buffers

L=5nH, R=0.01Ω, C=0.5pF

Clocks

1ns Rise and Fall

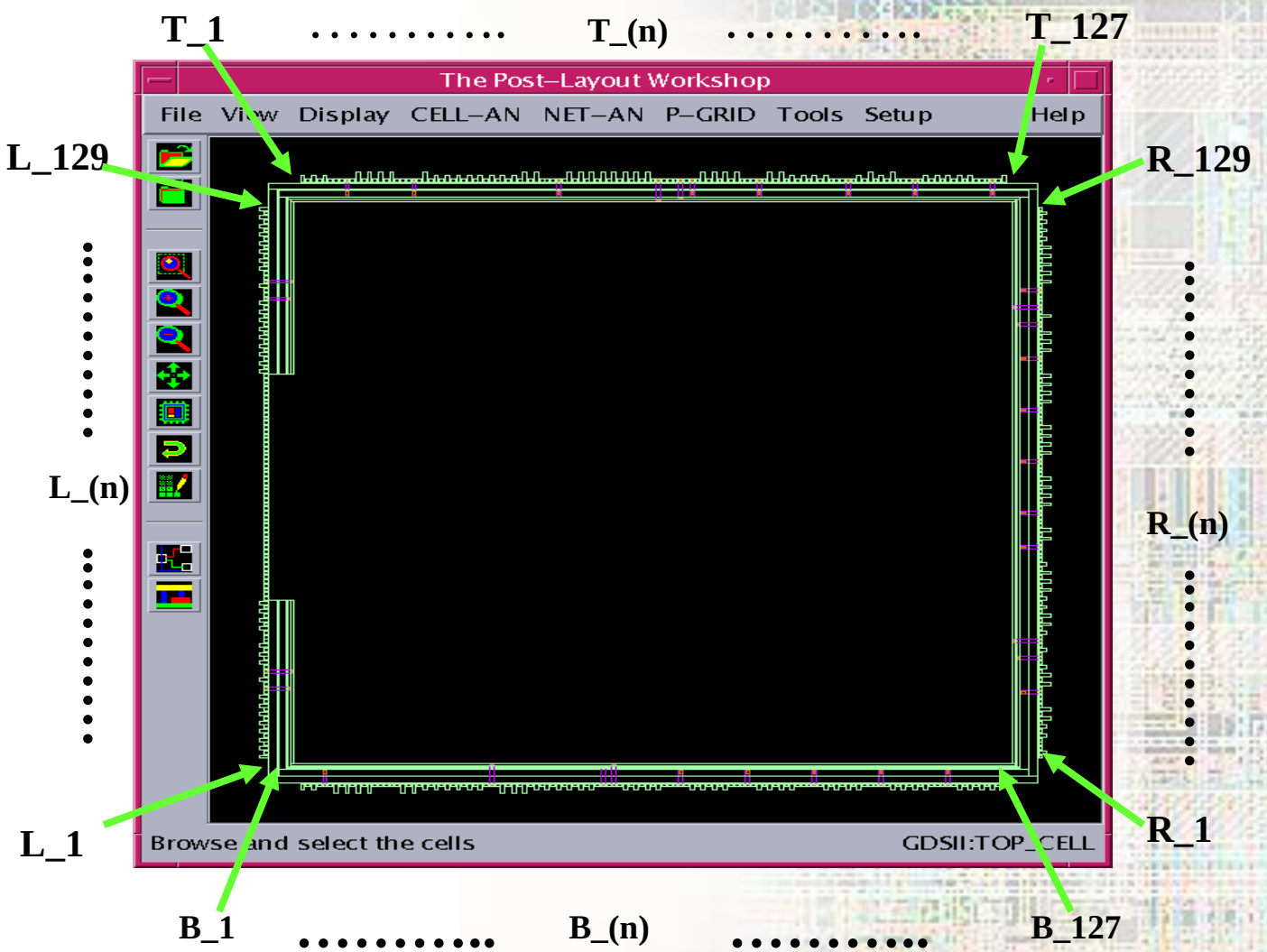
Rings & Voltages

VD33 = 3.3 V, 60µ

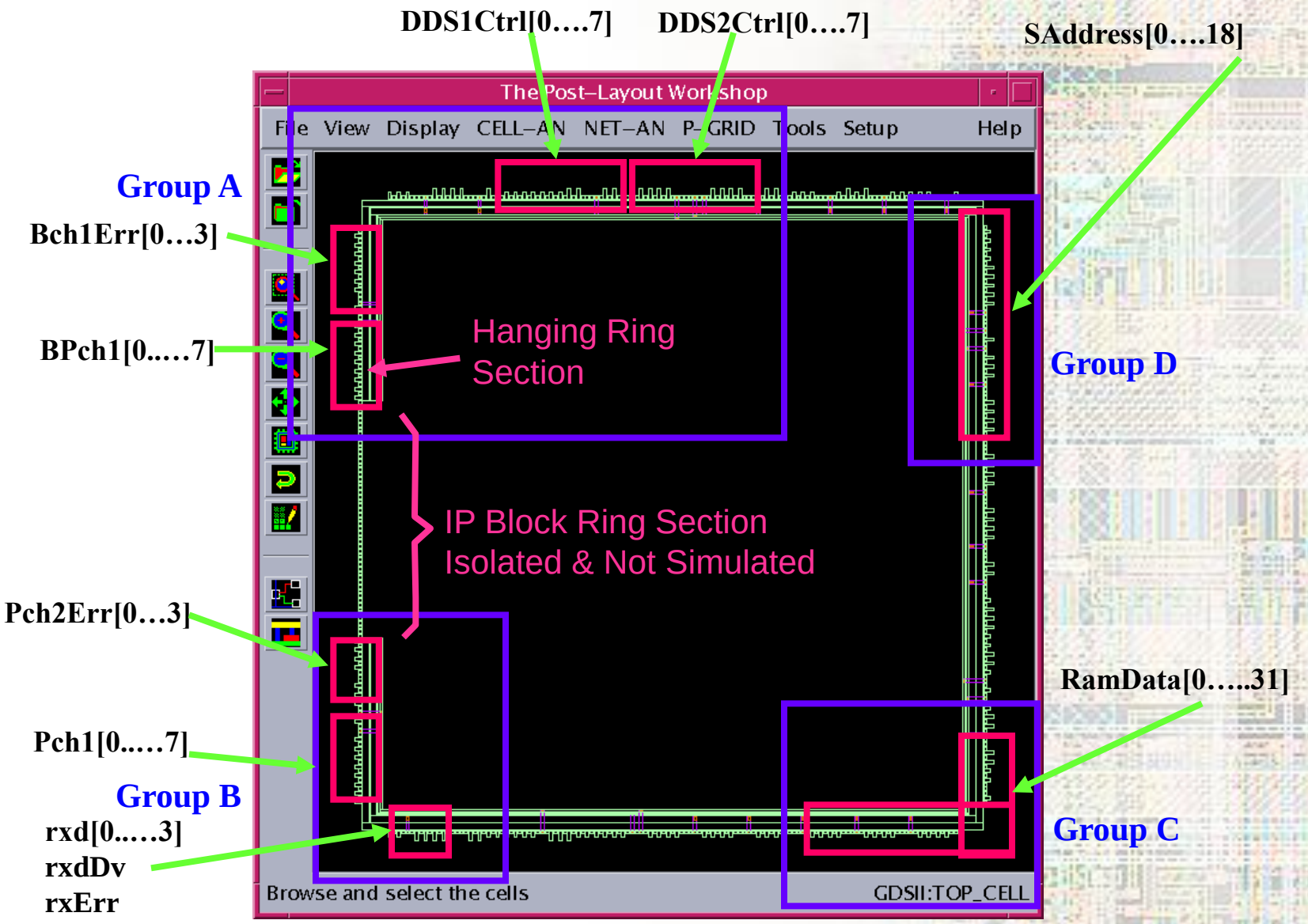
VSSPST = 0V, 60µ

VDD = 1.8 V, 20µ

VSS = 0V, 20µ



Grouping Simultaneous Switching Buffers Optimizes Simulation Time



Group A Spice Simulation Output

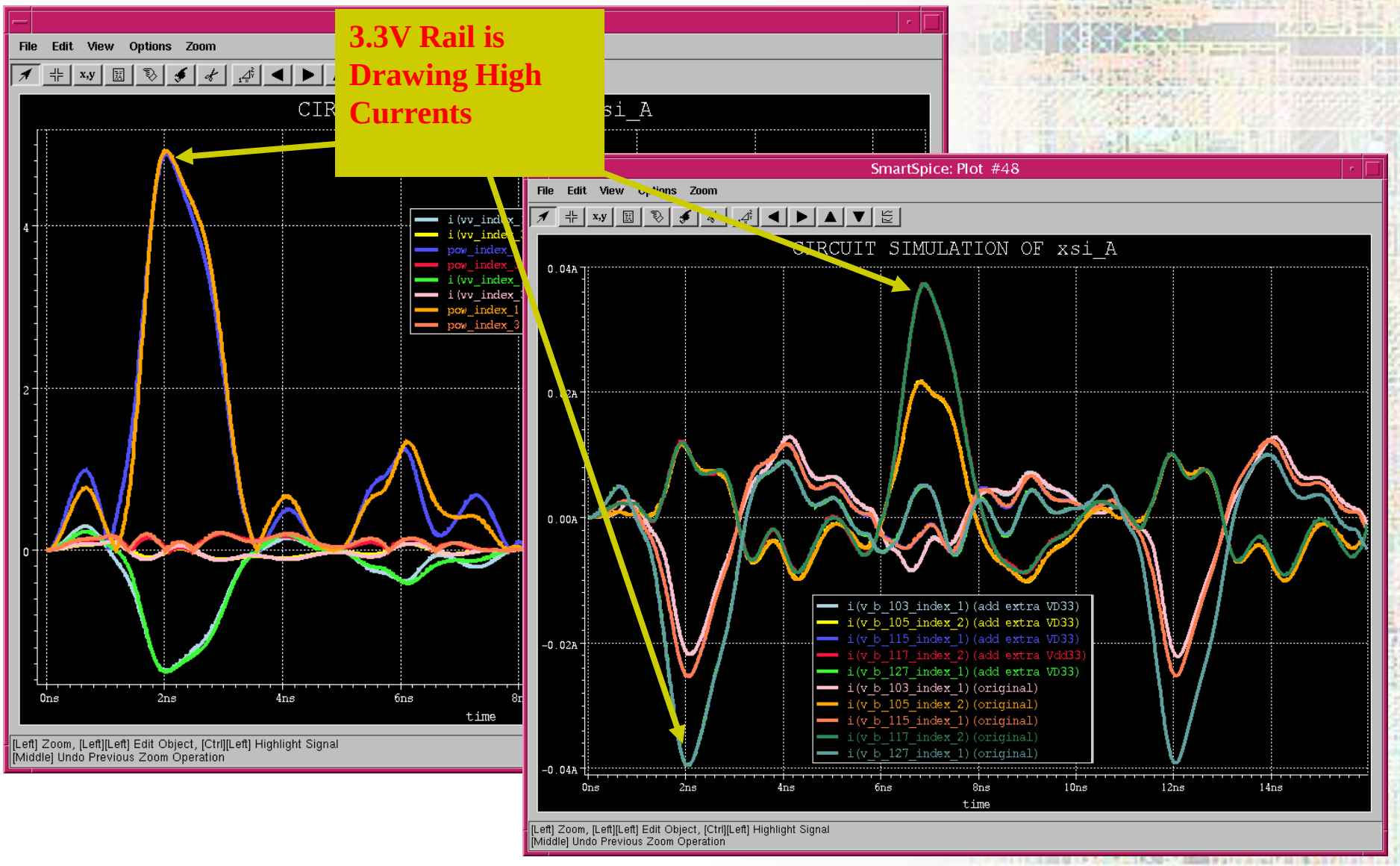
Problem Maintaining High on BPch1 Bus

Group A Spice Simulation Output

Problem Maintaining High on Bch1err Bus

Examining Group A Currents to Power and IO Pins

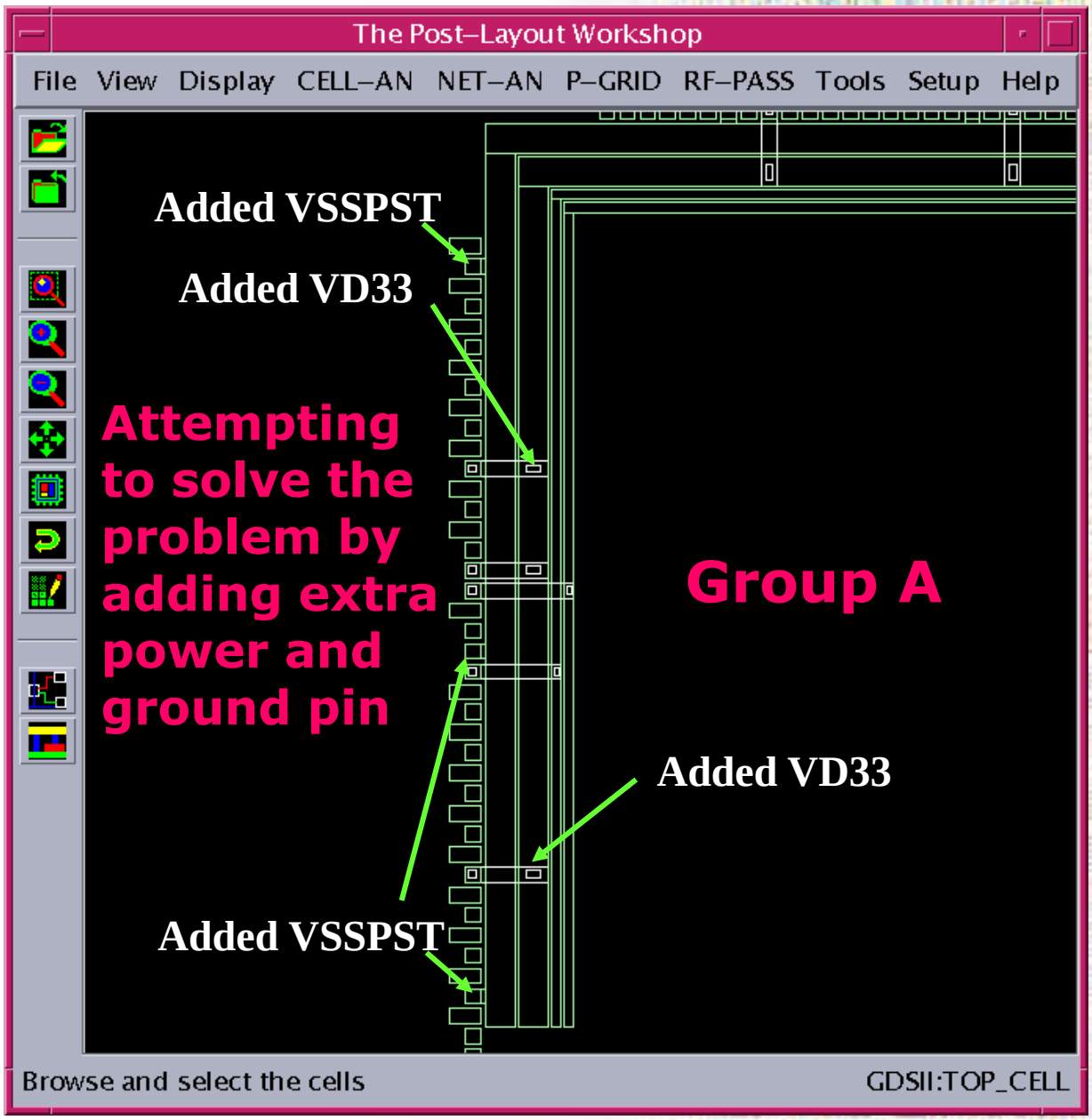
3.3V Rail is Drawing High Currents



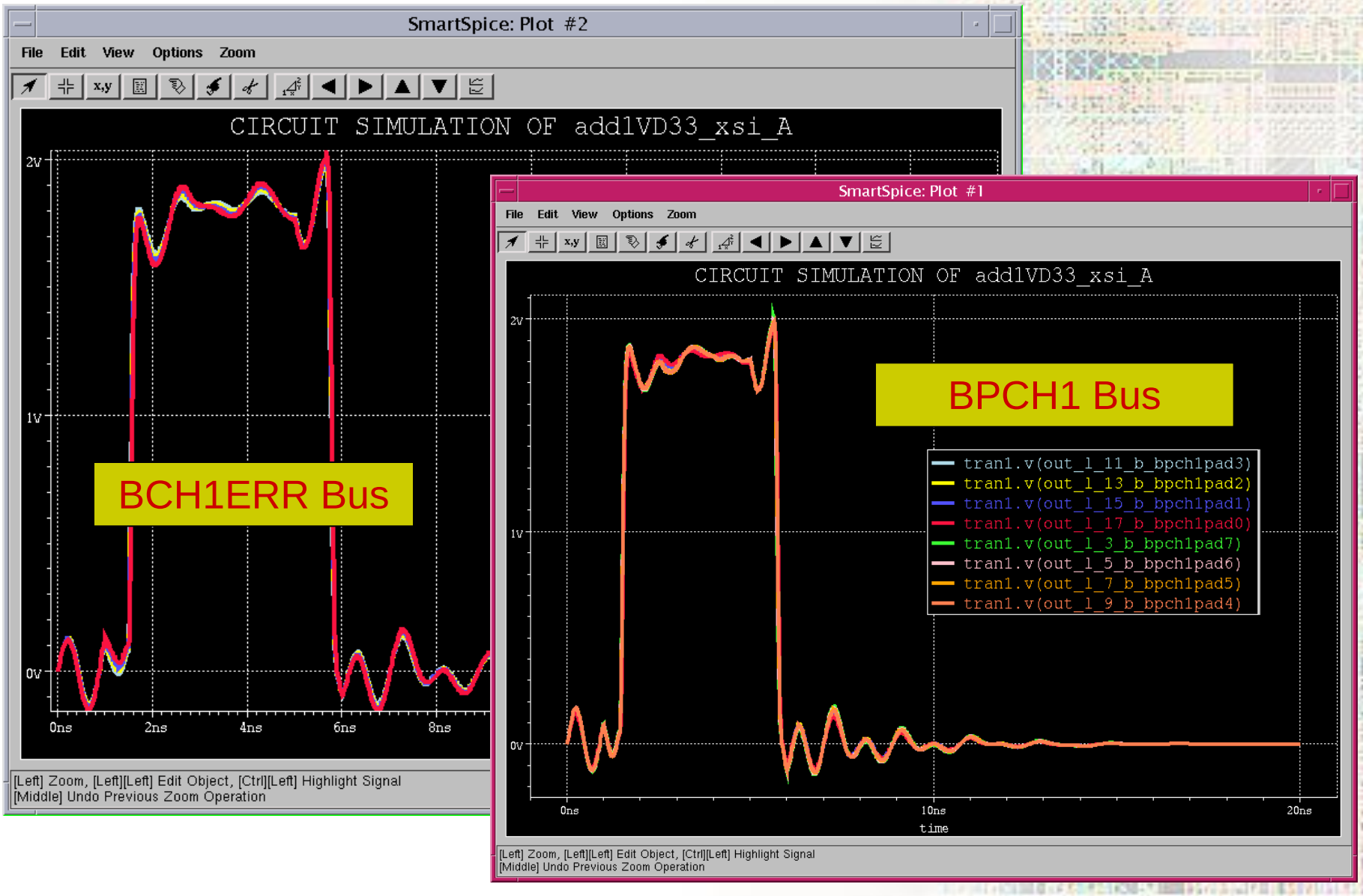
Fixing the Group A Bus Problem

There are a number of ways to solve any IO ring problem

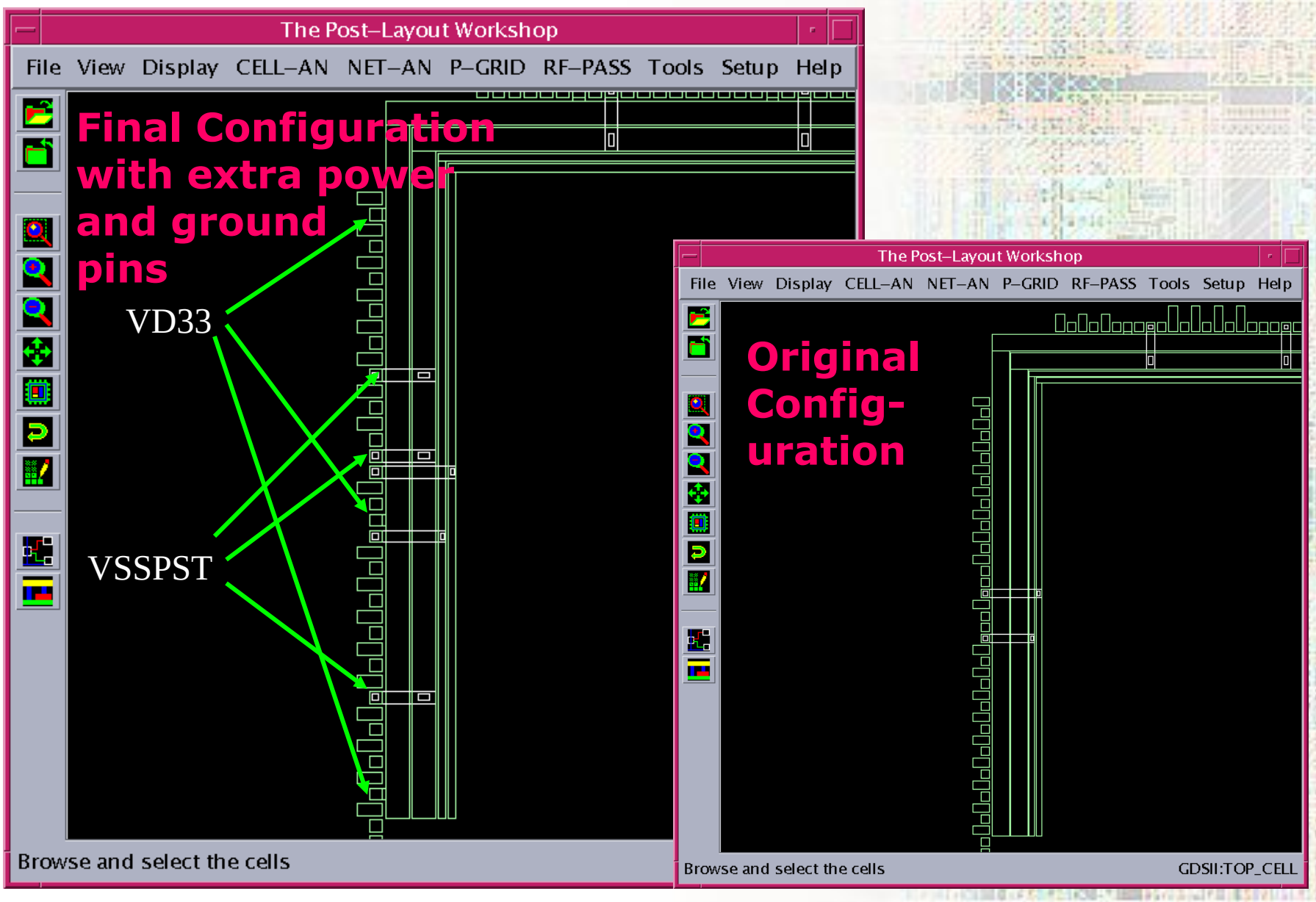
1. Lower L on power pins
2. Adding or moving power pins
3. Moving buses or spreading out simultaneously switching pins
4. Adding decoupling caps



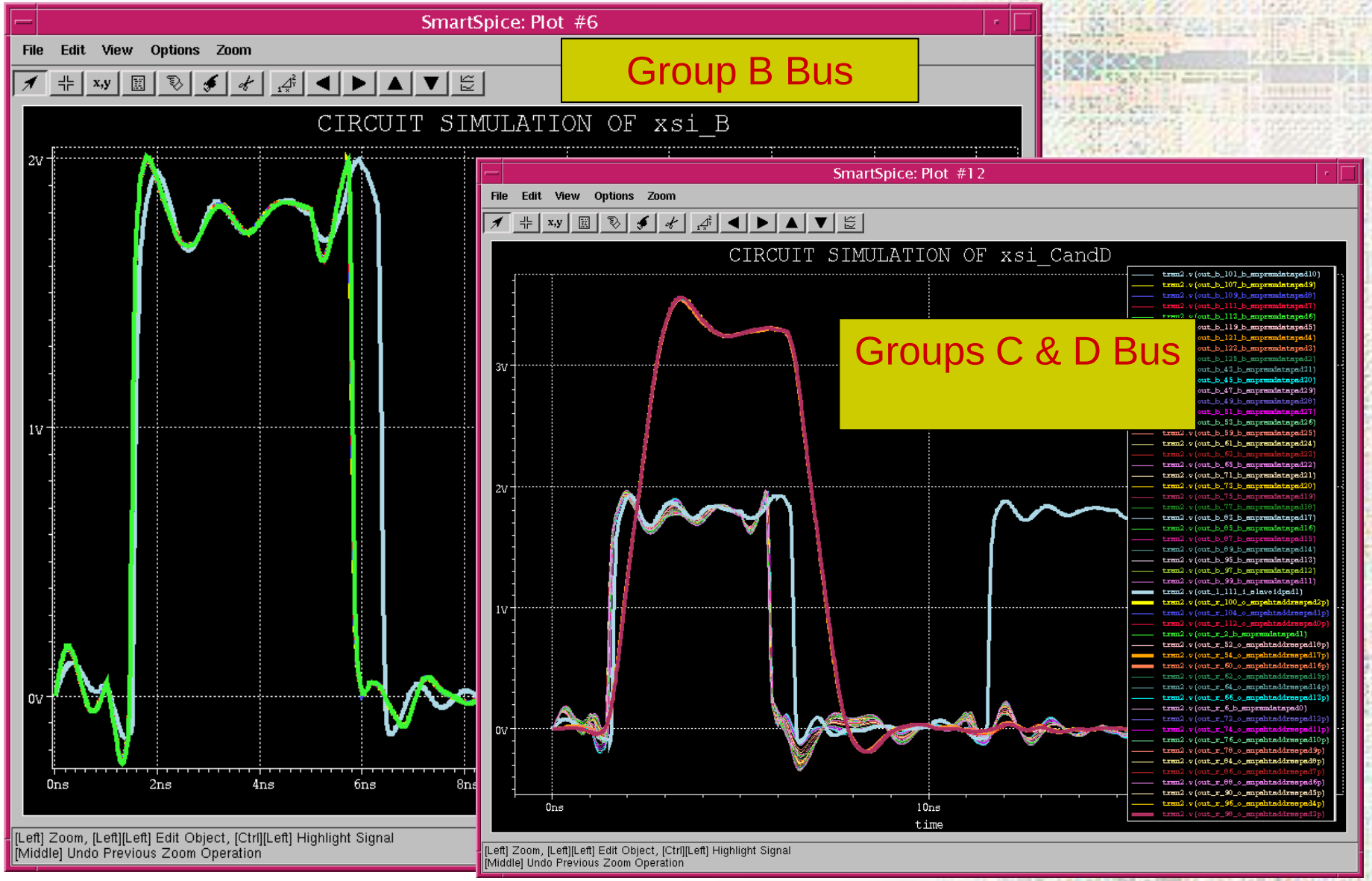
Group A Spice Re-Simulation After Adding Power Pins



Group A Power Pins Before and After the Fix



Groups B, C, & D Spice Simulations Showed No Similar Problems

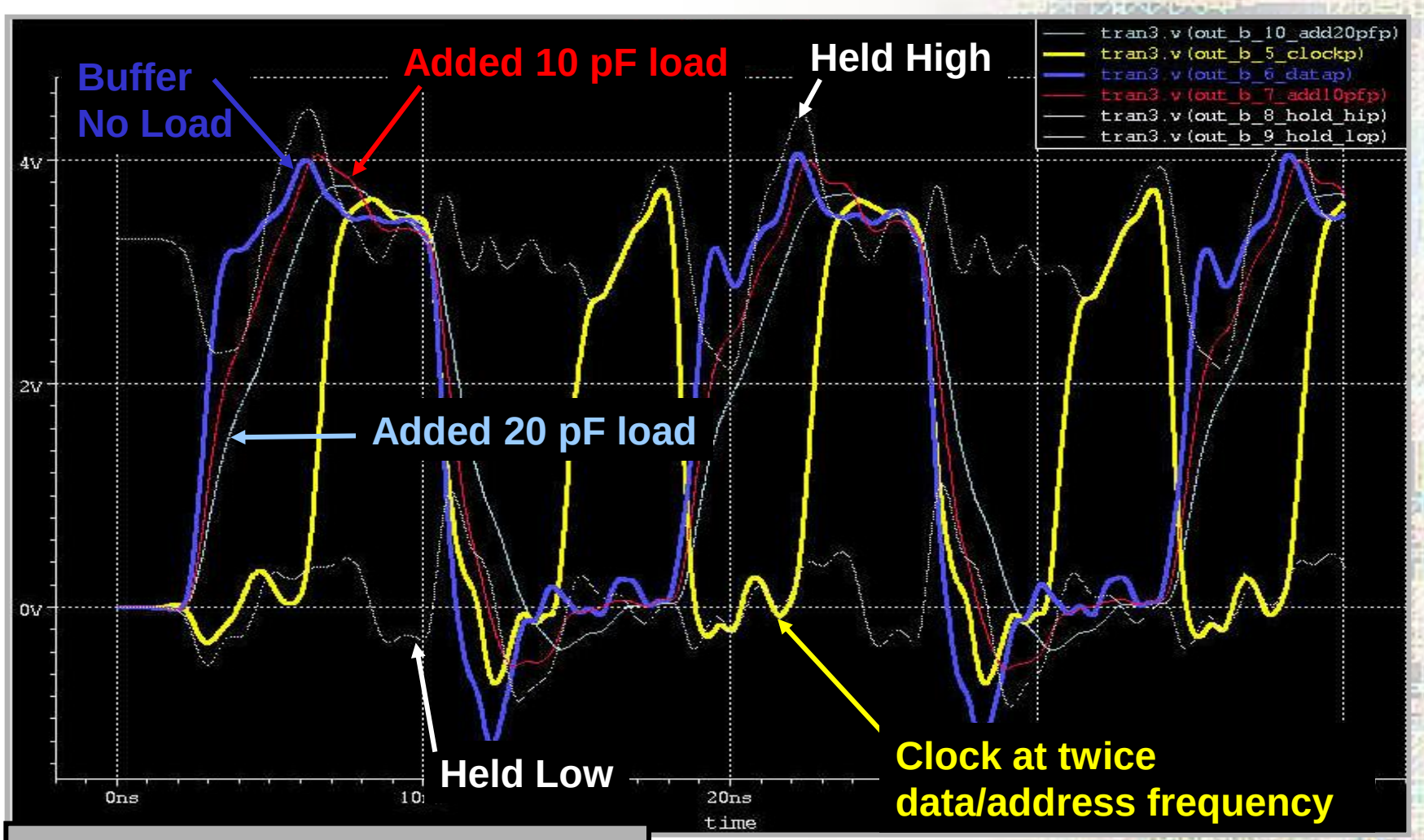


Other Analysis Examples Using Ring Designer

Once the initial input file is setup, iterations or variations only take a few minutes of time

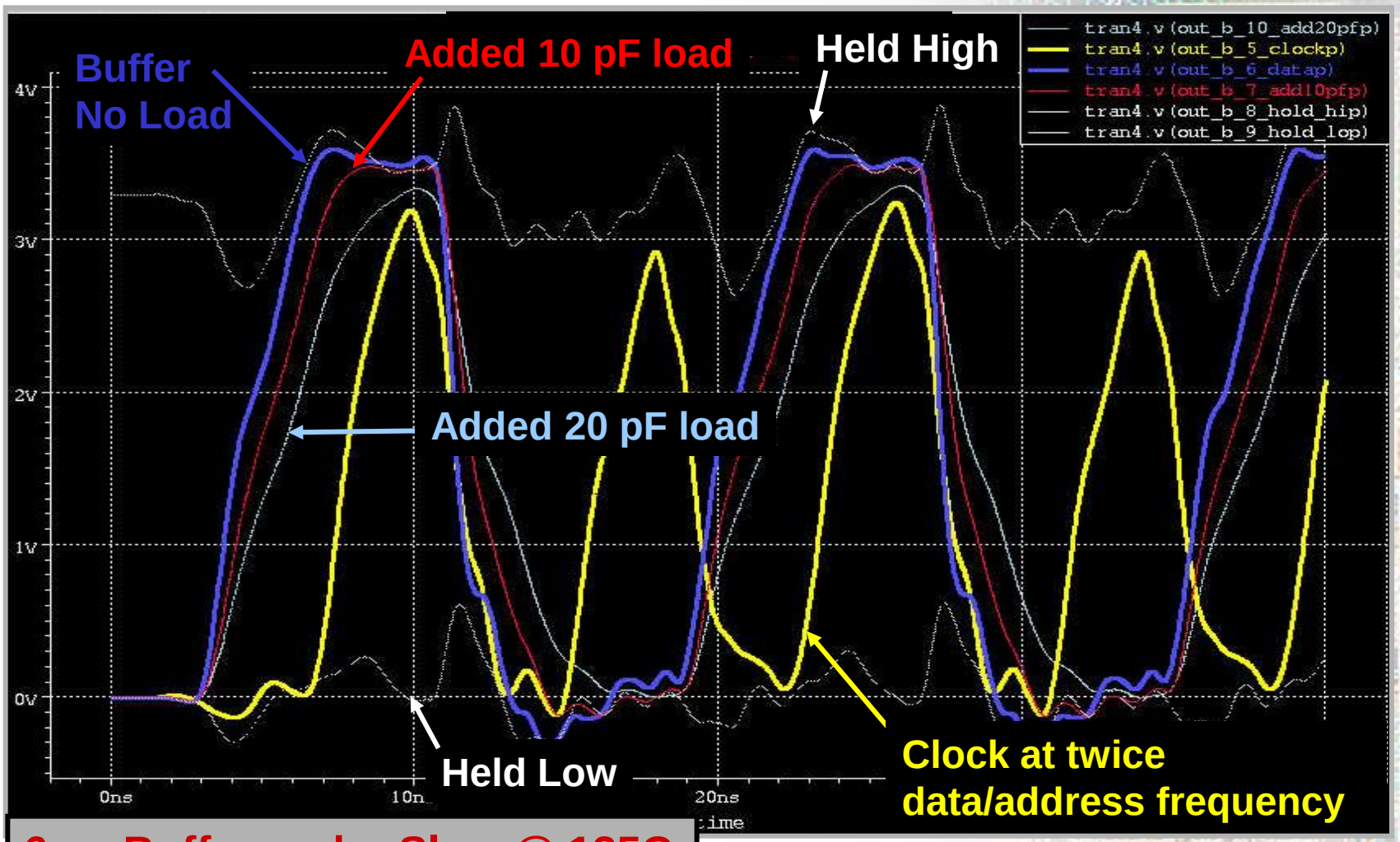
- Testing Different Possible Loading Conditions and Signal Integrity Under Different Switching Conditions
- Testing How Process Corners and Temperatures Relate to I/O Buffer Delay
- Examining Alternative Package Performance to Save Costs
- Examining Noise on Quiet Lines

Examining Different Possible Loading Conditions and Integrity of Signals Under Different Switching Conditions



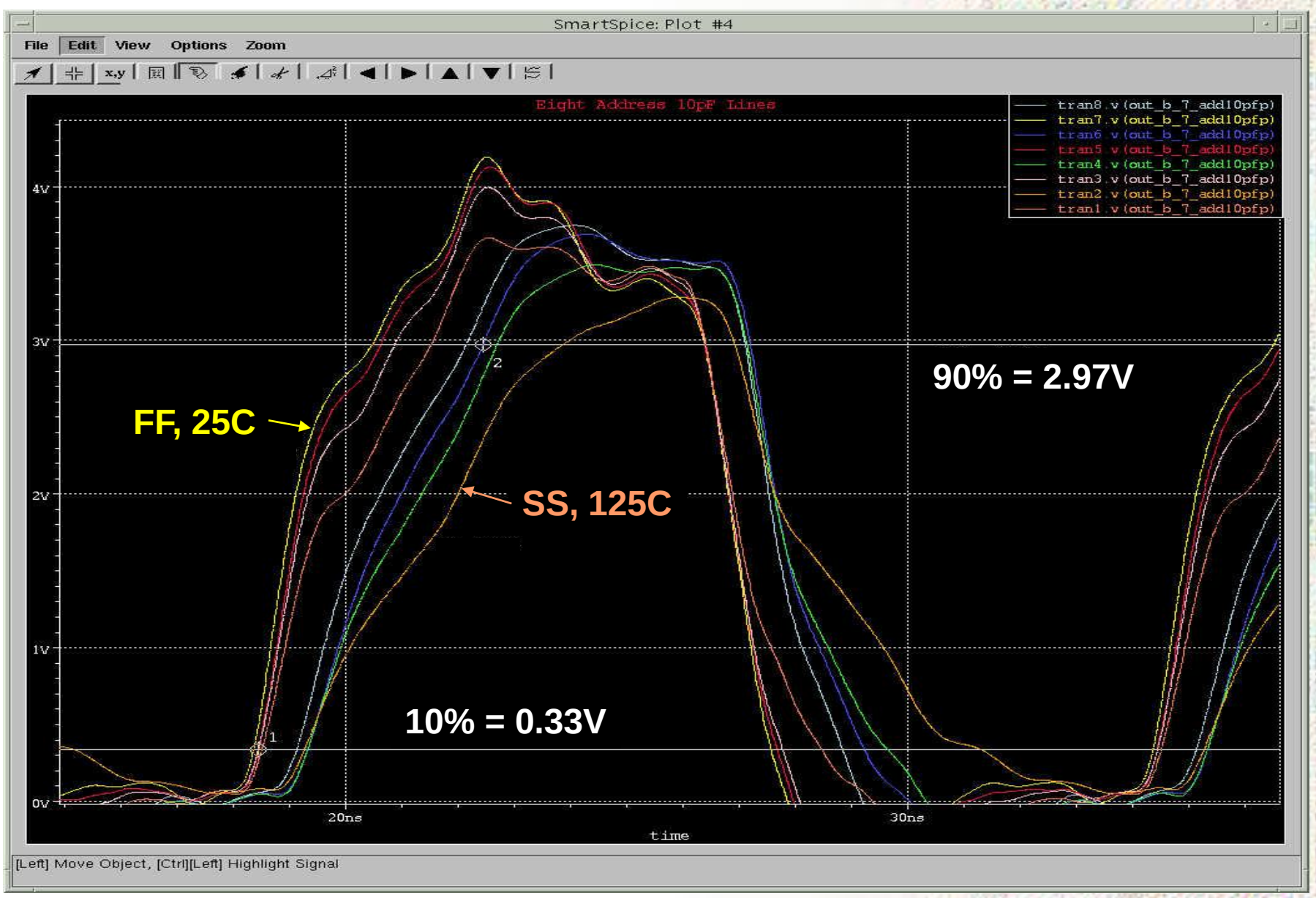
6ma Buffer under Fast @ 25C

Examining Different Possible Loading Conditions and Integrity of Signals Under Different Switching Conditions



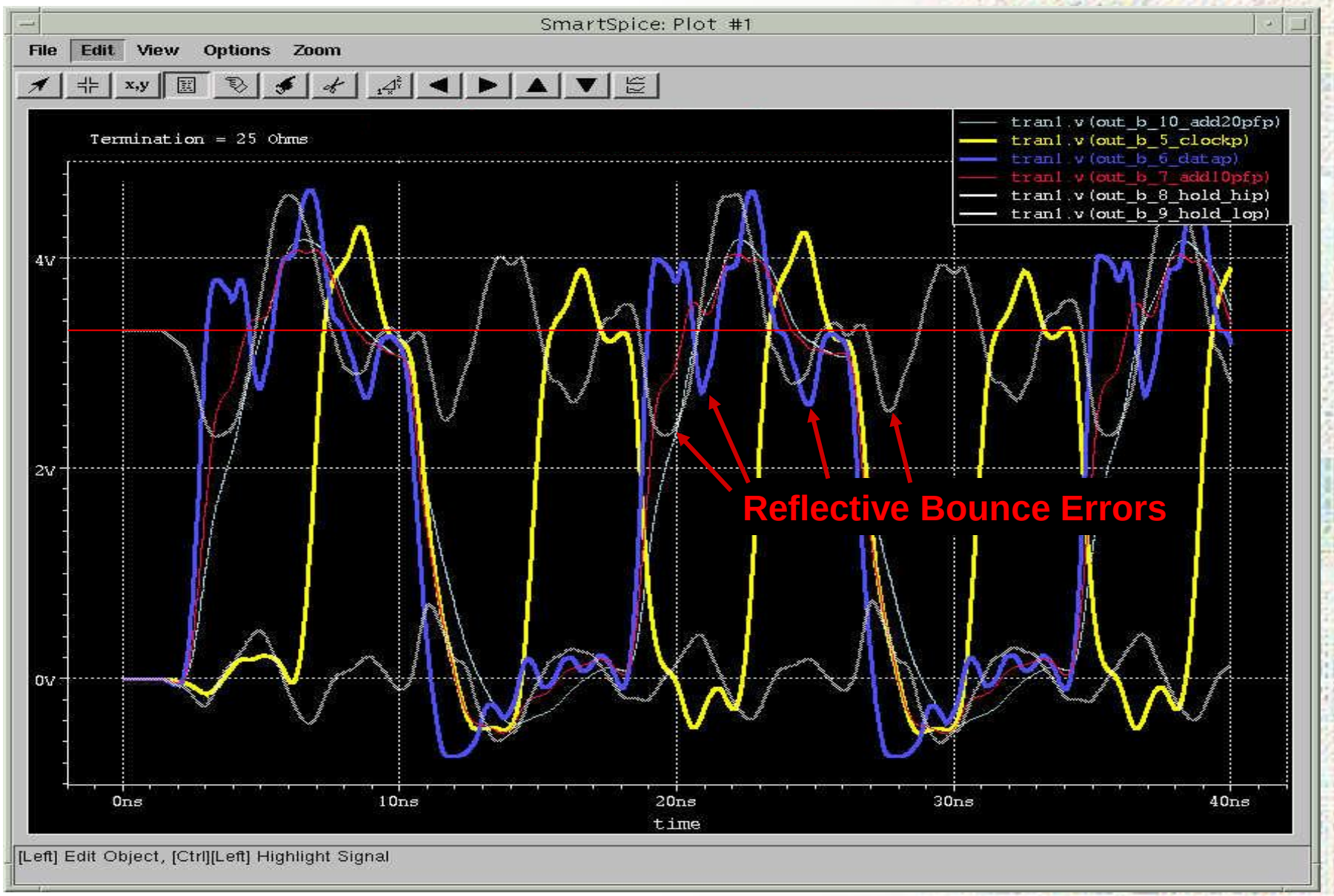
6ma Buffer under Slow @ 125C

The Extremes of Process Corners and Temperatures Versus I/O Buffer Delay

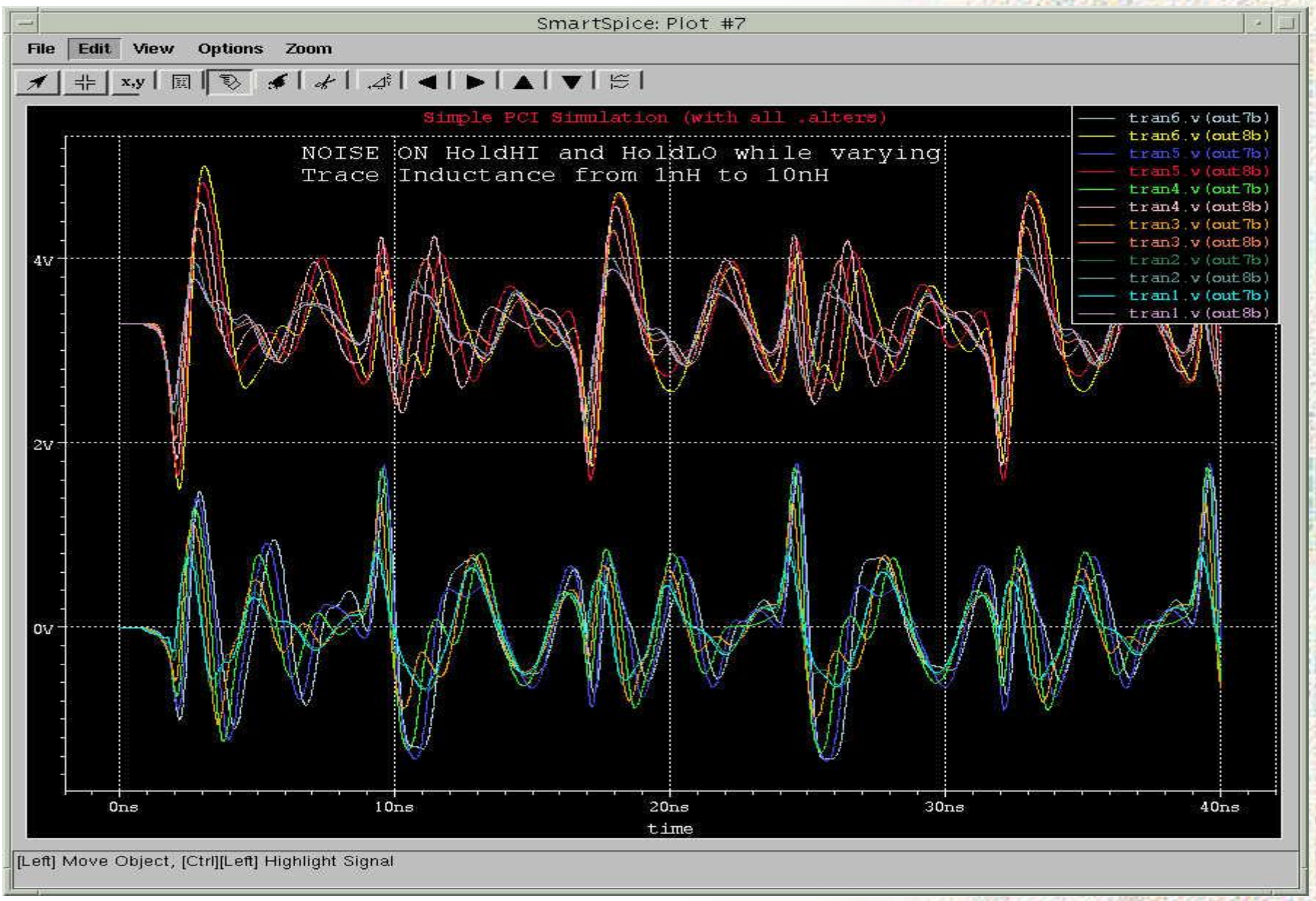


Examining Signal Integrity of Active and Quiet I/O Buffer Output Pins

Looking for I/O Buffer Output Pin Noise Errors



Examining Package Inductance Effects on Quiet Lines



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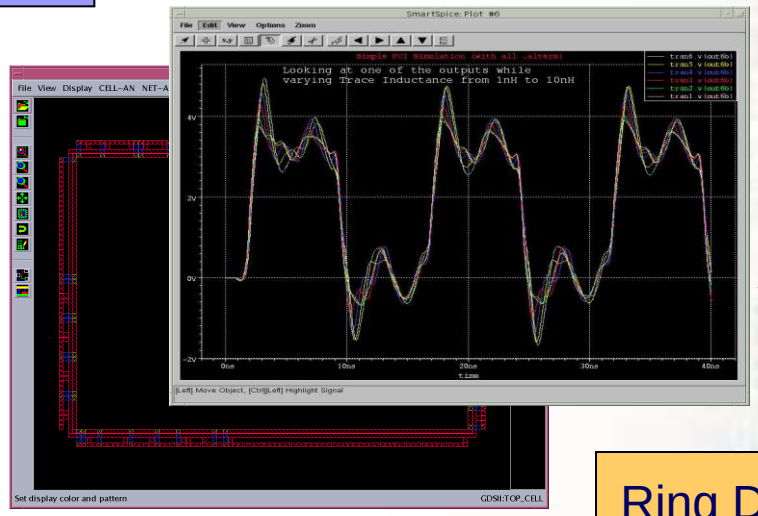
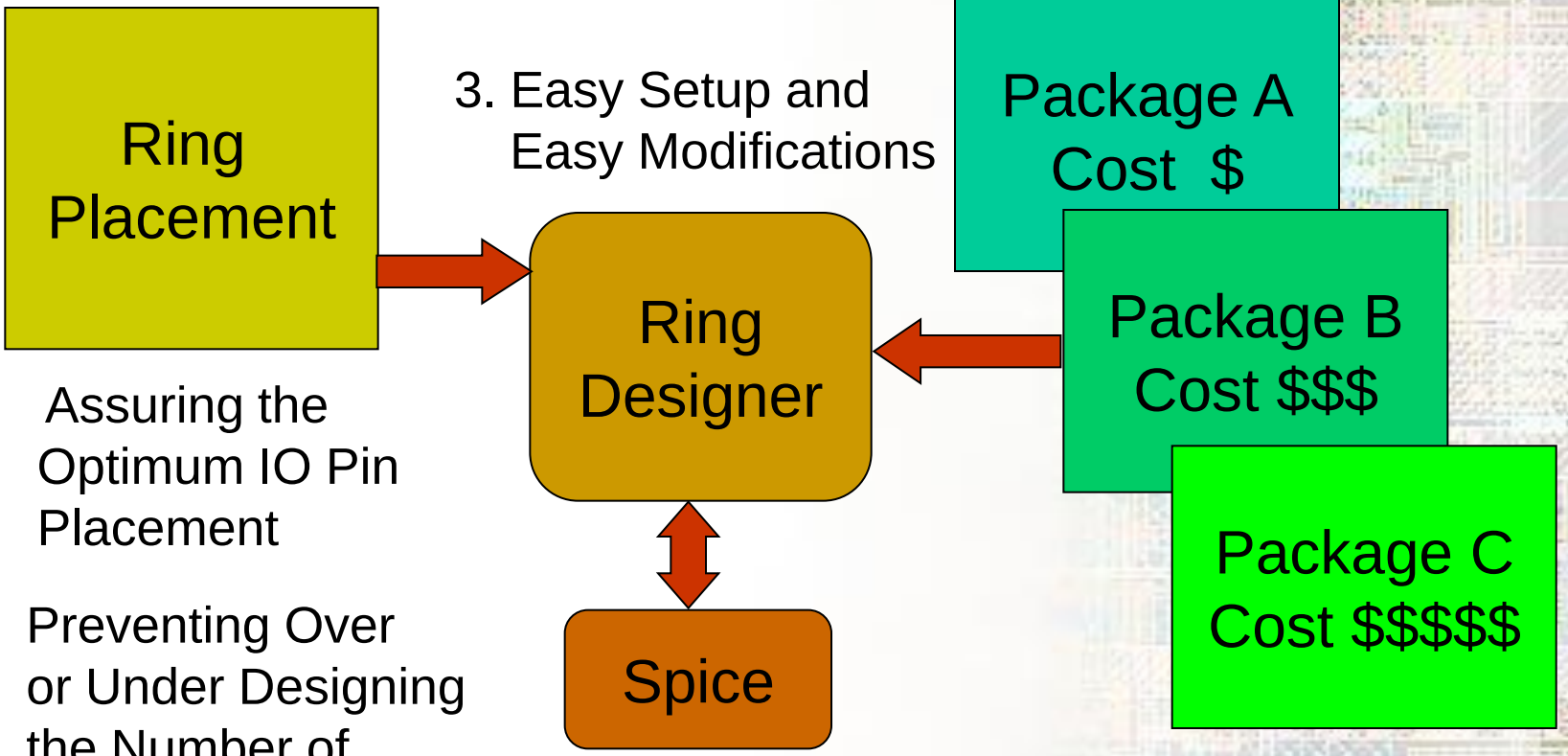


What are the Benefits to Using This Solution?



1. Assuring the Optimum IO Pin Placement
2. Preventing Over or Under Designing the Number of VDD/VSS IO pins
3. Easy Setup and Easy Modifications
4. Best Accuracy of Simulation by using Spice
5. Error Free Circuits
6. Assuring the Lowest Cost Package While Maintaining Performance

High Speed IO Ring and Package Analysis Review

- IO pre-planning using Spice is the best way to avoid problems.
  - Create the full circuit
    - Simulate or estimate package and include PCB parasitics & loading
    - Use simplified IO ring parasitics
    - Use real IO buffer spice models
- Model in Spice to find problems
  - Simultaneous switching noise
  - Ground bounce
  - Excessive group switching delays
  - Corner modeling
  - …
- Modify pin placement to remove problems and re-run
  - Add VDD/VSS pins
  - Add decoupling caps
  - Switching pin locations