SPIRAL™ 3D Spiral Inductance Synthesis and Design Tool

OEA International, Inc. 155 East Main Ave, Suite 110 Morgan Hill, CA 95037

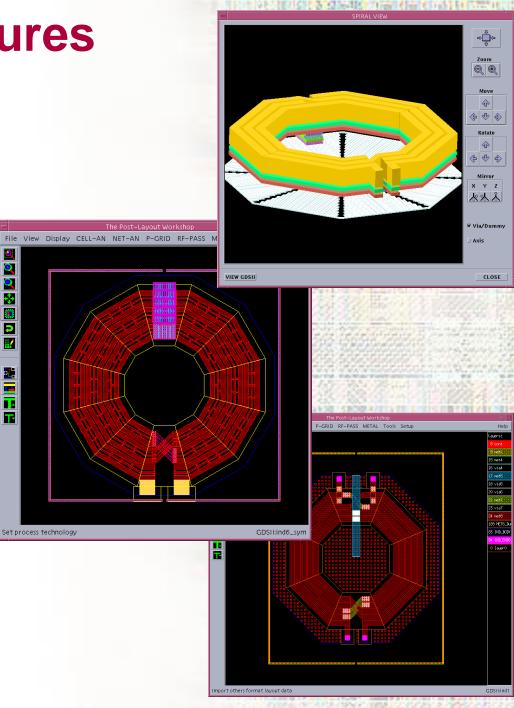
www.oea.com



SPIRAL Features

- Fully Automatic Synthesis of Spiral Inductors, Differential Inductors, Baluns, and Transformers
 - Full Physical DRC Clean Layout in GDSII or DF2 Format
 - Full Spice RCLK Output
 - Compact Model to Fit Narrow or Wide-Band Applications
 - S-, Y-, and Z-Parameter Models
 - Monte Carlo and EM Analysis
- Very High Accuracy & FAST
 - Matches Measured Silicon
 - Patterned Ground Shield Support
 - Substrate, Skin & Proximity Effect
- Ready for 90nm & 65nm Design
 - Dummy Metal Fill (for CMP)
 - Slotting to User DRC Rules
- Extremely Easy to Use
 - Targeted for RF Designer
 - Automatic Optimization for best Q at frequency and size
 - Automatic Design Space Exploration
- Multiple Use Models
 - Standalone Batch and Interactive Operation
 - Fully Integrated with Cadence





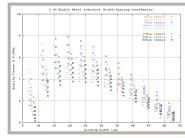
Spiral Value Proposition Significant Time/Effort-to-Model Reduction

Single Tool produces layout, S-, Y-, Z- Parameters, and Compact Spice Model

• Single Tool/Single Engineer vs. Multiple Tools/Multiple Engineers

Very Fast Runtime - Minutes vs. Hours

- Thorough Design Space Exploration
 - Ensures Optimum Device is Found



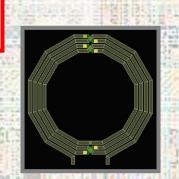
1e+08

1e+89

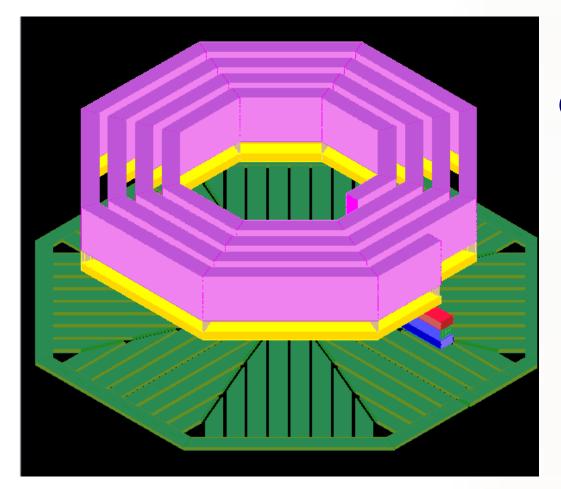
1e+16

- High Accuracy Simulations Match Measurements
- Make Alternative Spiral Types Readily Available
 - Provides significant performance and die size benefits





Standard Two Port Inductors

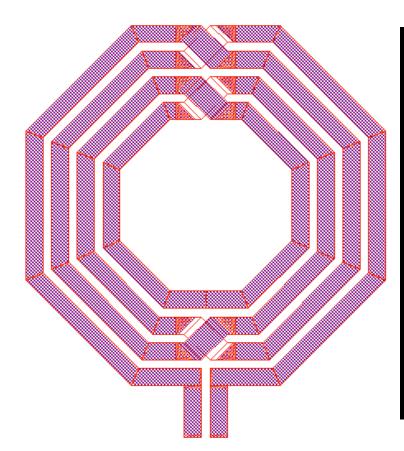


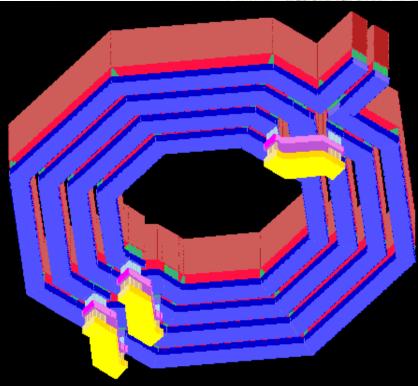
Optimization Requires Choosing:

- Metal layer(s)
- Radius
- Winding Width
- Bridge Width
- Spacing
- Etc...



Symmetric 3-Port Differential Inductors



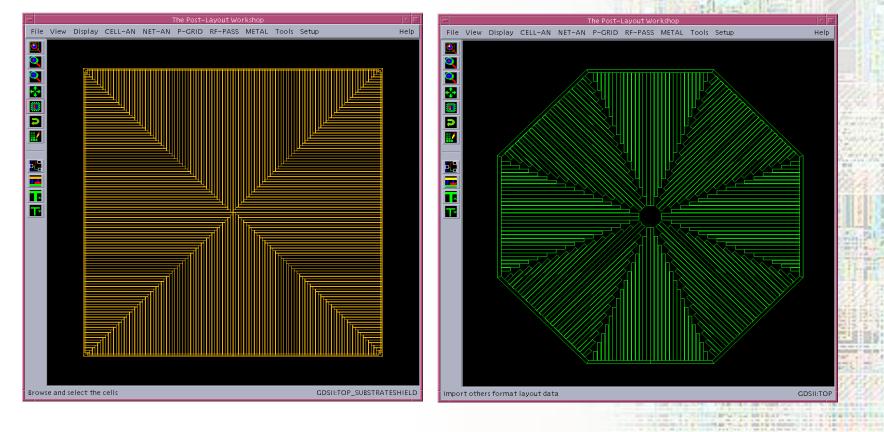


Symmetric Center Tapped Inductors instead of 2 'uncoupled' inductors:

- Easily defined center tap
- Reduced chip area
- Higher Q (reduced substrate losses)
- No need to model parasitic coupling

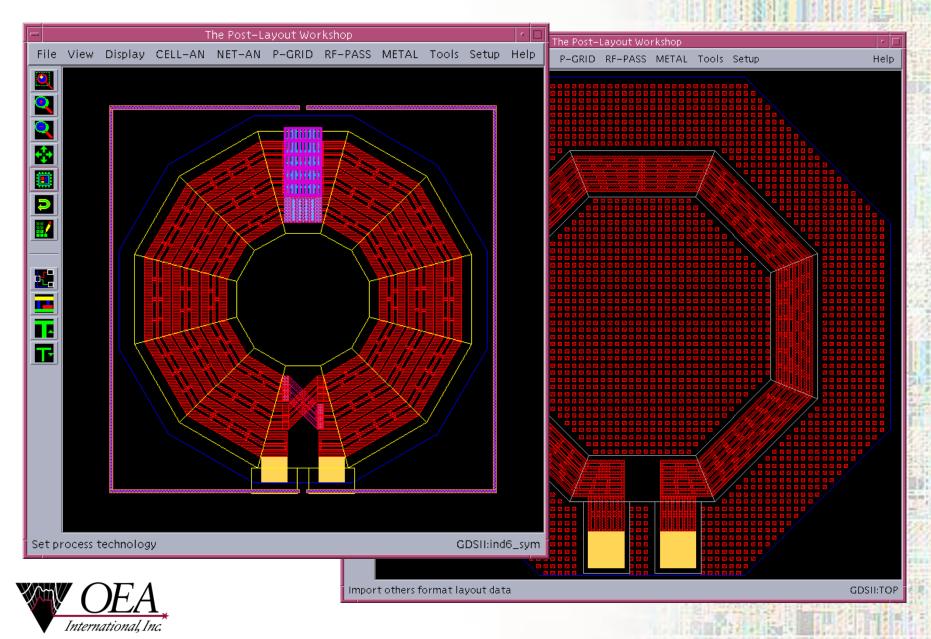


Patterned Ground Shields

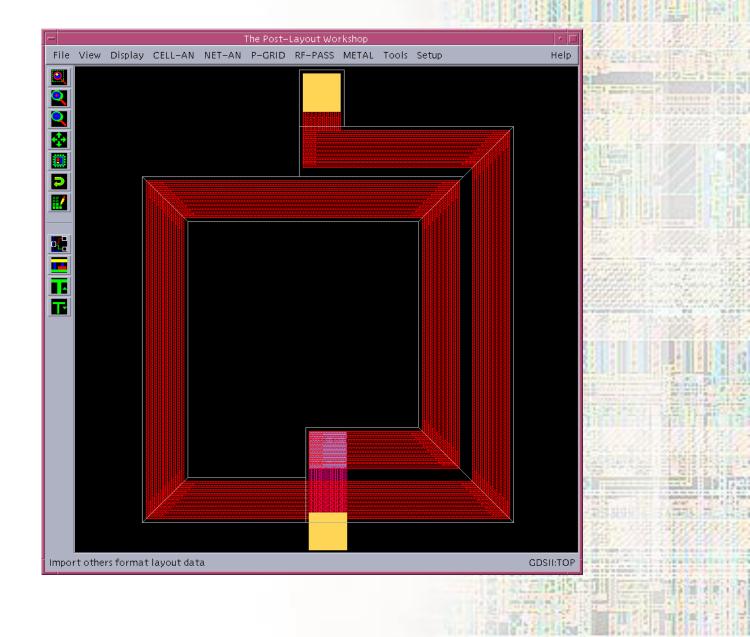




Slotted Spiral Inductors With or Without Dummy Metal Fill

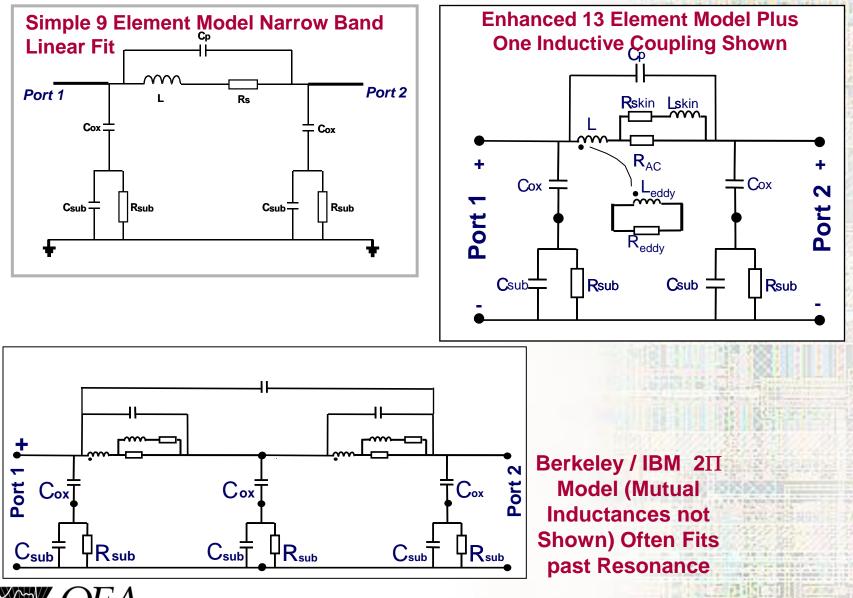


Striped Spiral Inductor with Connections at Corners





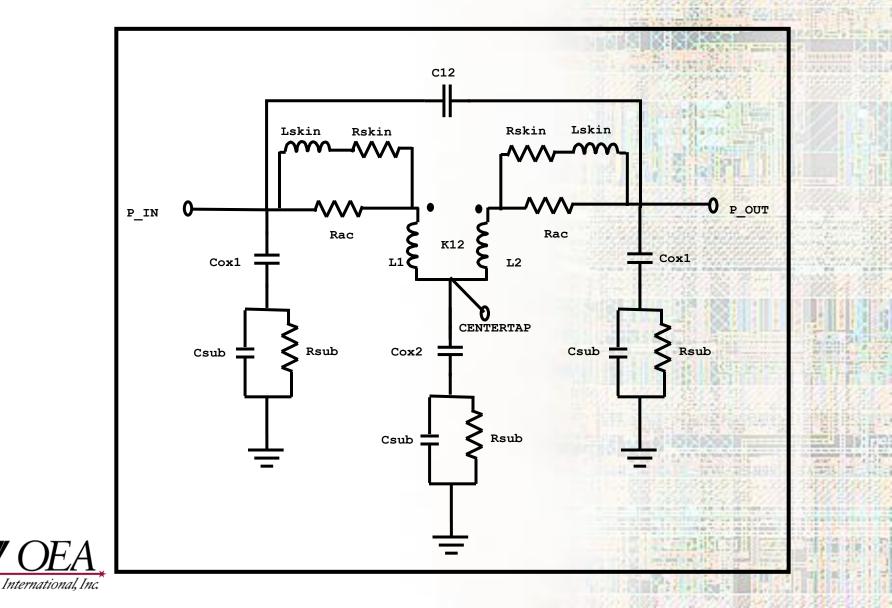
Compact Model Fitting



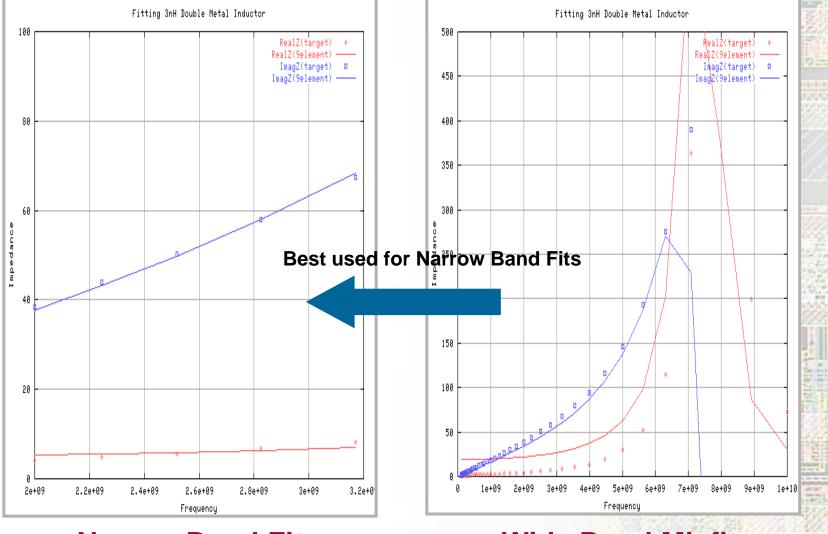
International, Inc.

S. 1.

Symmetric Inductor Lumped Model



9 Element Model Fit

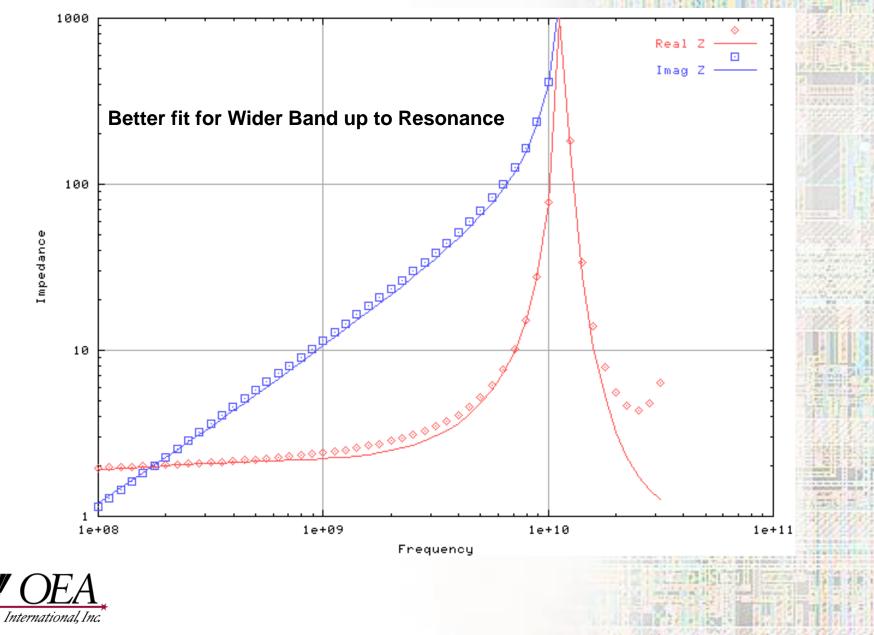


Narrow Band Fit

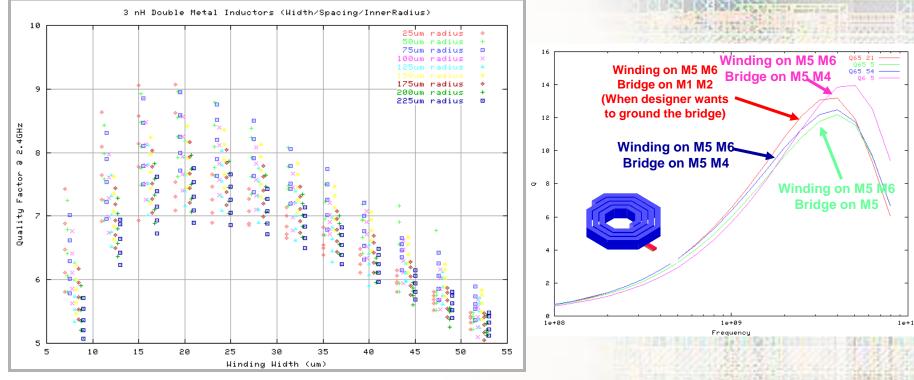
Wide Band Misfit



Broadband 13 Element Model Fit



Spiral Value Proposition Design Space Exploration & Optimum Device Synthesis



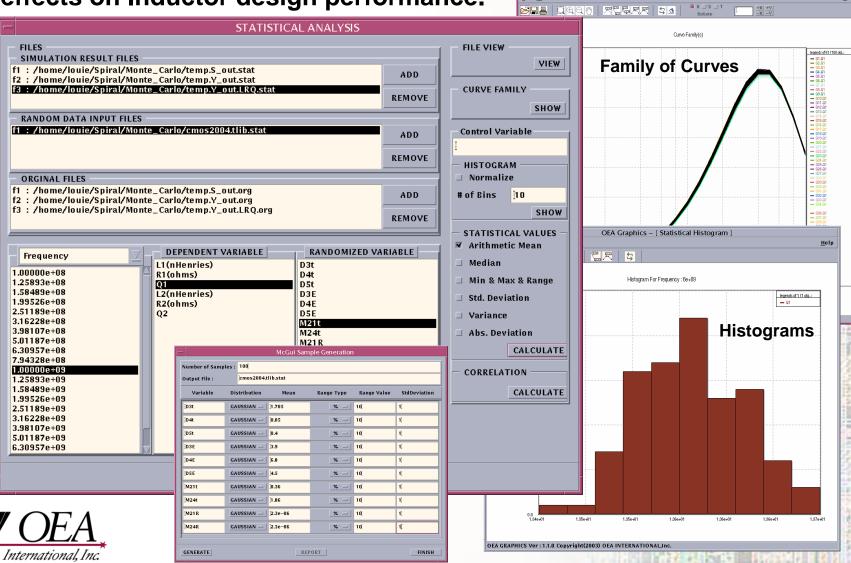
- Thousands of Solutions Synthesized
- Performance/Area Tradeoffs Easily Analyzed
- Guides Designer to Correct Implementation to Optimize



Spiral Monte Carlo Analysis

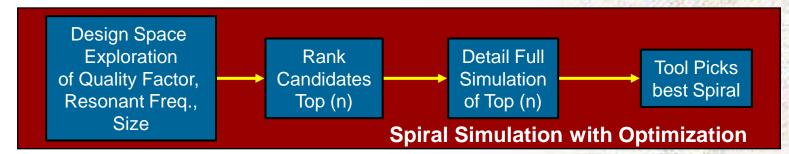
Help

Full support and reporting of process variation effects on Inductor design performance.



Spiral Value Proposition Improved Design Performance/Quality

- Ease of Use Enables Deployment to Designer's Desktop
 - Tight Integration with Cadence Composer and Artist
 - No EM Knowledge Required

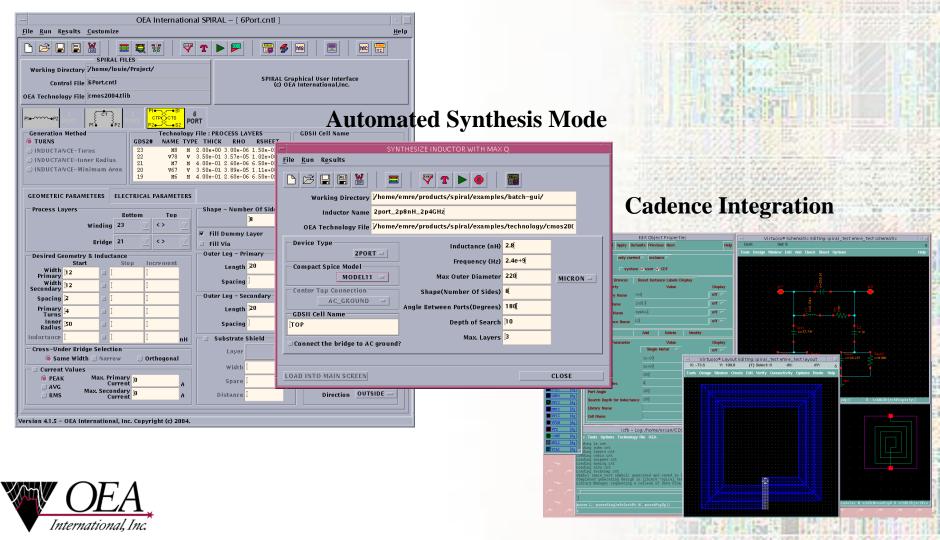


- Design Specific Component Optimization
 - By Frequency, Area, Port Locations
 - Better Yield: Models Include Process Variations



Spiral's Ease of Use Enables Widespread Deployment

User Defined Geometry Mode



Full Range of Parameter Definitions for Customizing Inductor

Insulating Substrate Model

▼ Topside Substrate Contact

Force to be Square

Z Mesh Distance 50

Substrate Circuit Model

🗆 High Level Model

Minimum K Value 0.1

X,Y Extension 50

Density LOW -

RCLK =

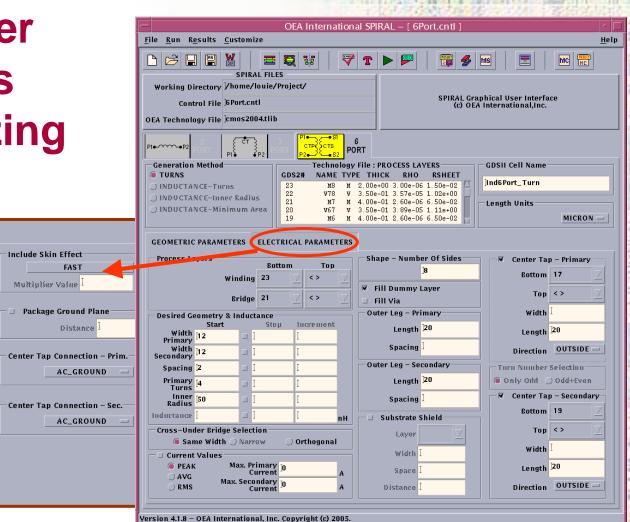
AC_GROUND ==

Substrate Metalization

Distance 75

₩idth

Substrate





SYMMETRIC ----

GEOMETRIC PARAMETERS ELECTRICAL PARAMETERS

Frequency Sweep LOG -

Start Freq. (Hz) 1e+08

Stop Freq. (Hz) 3e+10

🗆 Auto Stop Frequency

First Reseasance

🔵 2*First Resonance

Generate S,Y and Z parameters

🔵 Cougar Flow

Panther Flow

Compact Spice Model

Points per Decade 10

TECHNOLOGY CMOS99 # Units of microns apply to all length dimensions below UNIT MICRONS METAL les **#Order Layerno Name Type Z_min Thickness Resistivity J(PEAK** EdgeBias AVE RMS) POLY 0.350 0.200 1.56E-04 1.00E-03 0.00E+00 0.00E+00 0.00E+001 Ρ 2 2 СТ 3 2.90E-04 1.00E-03 0.00E+00 0.00E+00 0.00E+00 С 1 3 3 м1 1.050 0.530 4.13E-06 1.00E-03 0.00E+00 0.00E+00 0.00E+00 М Propert 4 4 ٧1 1.02E-04 1.00E-03 0.00E+00 0.00E+00 0.00E+00 V 3 5 5 5 м2 2.380 0.530 4.13E-06 1.00E-03 0.00E+00 0.00E+00 0.00E+00 М 6 6 **V**2 1.02E-04 1.00E-03 0.00E+00 0.00E+00 0.00E+00 V 5 7 7 3.710 0.530 1.00E-03 7 м3 4.13E-06 0.00E+00 0.00E+00 0.00E+00М 8 10 **V**3 1.02E-04 1.00E-03 0.00E+00 0.00E+00 0.00E+00 V 9 9 4.13E-06 45 м4 5.040 0.530 1.00E-03 0.00E+00 0.00E+00 0.00E+00 М 10 1.02E-04 1.00E-03 0.00E+00 0.00E+00 0.00E+00 8 **V4** V 9 11 11 50 М5 6.370 0.530 4.13E-06 1.00E-03 0.00E+00 0.00E+00 0.00E+00 М 12 V5 13 1.26E-04 1.00E-03 0.00E+00 0.00E+00 0.00E+00 9 11 V 51 7.700 13 м6 3.000 3.56E-06 1.00E-03 0.00E+00 0.00E+000.00E+00М ENDMETAL DIELECTRIC hysica **#Order Type Thickness** Epsilon(z y) Х 3.90E+00 Si usually starts with a field oxide 0.350 3.90E+00 3.90E+00 1 # р 2 0.700 4.00E+00 4.00E+00 4.00E+00 # р 3 6.650 3.80E+00 3.80E+00 # 3.80E+00 р 4 4.000 4.20E+00 4.20E+00 4.20E+00 # р 5 0.700 7.90E+00 7.90E+00 7.90E+00 **Passivation** layer # р 6 1.00E+00 # Air 10.000 1.00E+00 1.00E+00 D ENDDIELECTRIC SUBSTRATE Δ **#Order Name** DopingType Thickness Resistivity Epsilon(z x y) epi 2.0 0.1 11.9 11.9 11.9 -1 р -2 bulk 600.0 10.0 11.9 11.9 11.9 S р -3 metal 3.0 3.0e-6 1.0 1.0 1.0 р Φ ENDSUBSTRATE efin DRCRULES # Layer 51 (M6) encloses layer 9 (V5) by 0.5 um enclosure 51 9 0.5 enclosure 50 9 0.1 # Layer 50 (M5) encloses layer 9 (V5) by 0.1 um viasize 9 0.7 # Layer 9 (V5) size is 0.7 um 9 0.7 # Layer 9 (V5) spacing is 0.7 um between vias minspace minwidth 51 3.0 # Minimum width for layer 51 (M6) is 3.0 um minwidth \$ 1.0 # Minimum width for all non M6 metal or poly layers is 1.0 um minspace \$ # Minimum space for all remaining layers is 2.0 2.0 gridsnap 0.01 # Snap all vertices to the nearest hundreth of a micron ENDDRCRULES ENDTECHNOLOGY

File

Technology

Process

3 CHARTER TOWN (IN COMPANY)

Spiral Value Proposition Advantages Over Pre-Characterized Libraries

Pre-Characterized Libraries

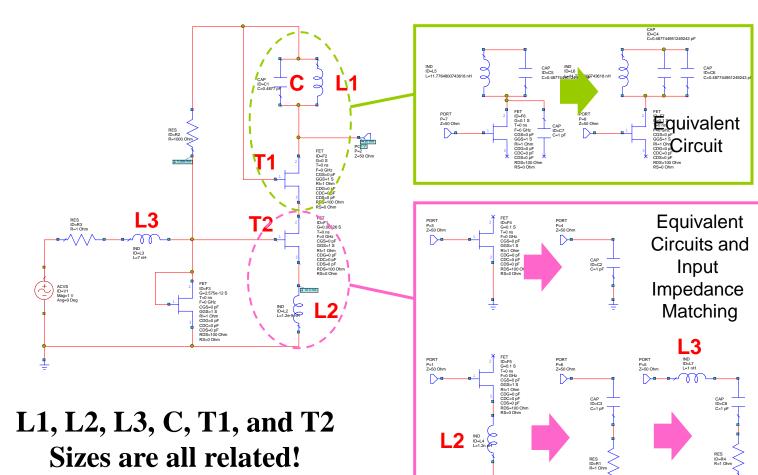
- 1. Accurate
- 2. Only specific Inductors Allowed can dramatically limit design
- 3. Very significant design and measurement effort
- 4. Available after running test chips only
- 5. Extensive rework if process is changed

SPIRAL

- 1. Accurate
- 2. Inductors optimized for particular design
- 3. Minimum possible effort
- 4. Available immediately
- 5. Process changes easily incorporated



Why Optimized Spirals are Critical in an LNA



OEA International, Inc. Tuning cannot easily be achieved with a predefined library of inductors

Spiral Value Proposition Advantages Over Full Wave Solvers

Full Wave Solvers

- 1. Analysis tool
- 2. Electromagnetic expertise required
- 3. Extensive tool experience
- 4. Accurate (for experts) beyond resonance but difficulty at very low frequencies
- 5. Hours to generate input plus several hours to run analysis on a single inductor
- 6. Output is S-Parameters requires separate fitting step to get SPICE
- 7. Not integrated with design environments

SPIRAL

- 1. Synthesis Tool
- 2. No EM expertise required easily used by RF designers
- 3. Minimum training required
- 4. Accurate up to resonance and very accurate low frequency results
- 5. Whole process runs in seconds or minutes including generation of fit models
- 6. Automated SPICE models both distributed and lumped available
- 7. Completely integrated with Cadence Composer & Artist



Spiral Value Proposition Advantages Over Analytical Tools

Analytical Tools

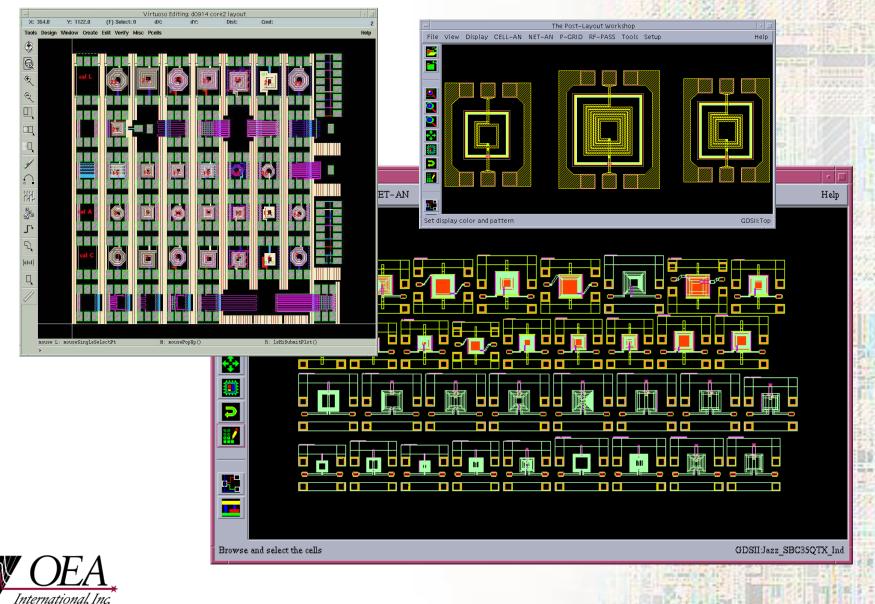
- 1. Analysis tool
- 2. Cheap sometimes free
- 3. Difficult to use
- 4. Accurate DC results, extreme difficulty with RF results
- Outputs are incomplete does not include S, Y and Z parameters, plots of LRQ, layouts, etc...
- 6. Separate fitting step to get lumped SPICE models
- 7. Not integrated with design environments

SPIRAL

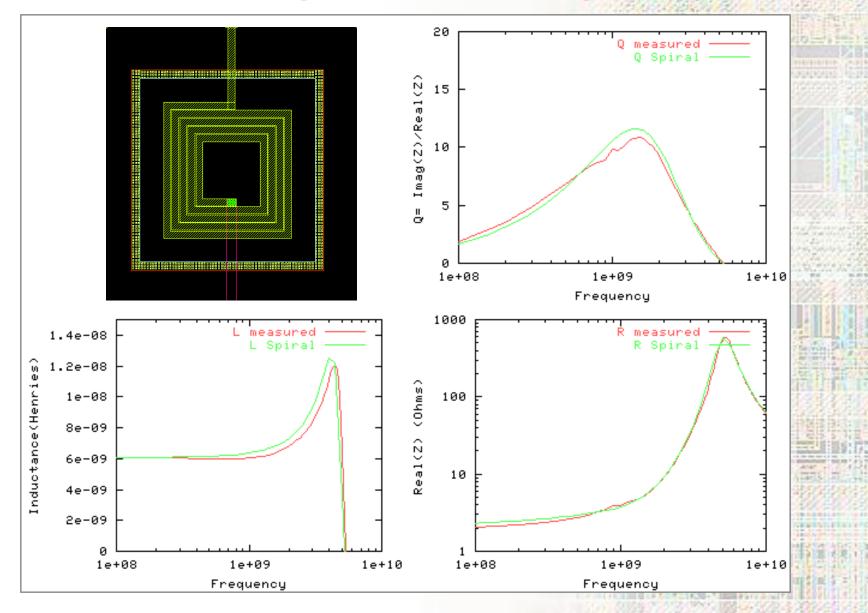
- 1. Synthesis Tool
- 2. Commercial Product
- 3. Very easy to use
- 4. Accurate DC results & highly accurate up to resonance
- 5. Complete set of outputs including S, Y and Z parameters, LRQ, DRC correct layouts etc...
- 6. Automated SPICE models both distributed and lumped available
- 7. Completely integrated with Cadence Composer & Artist



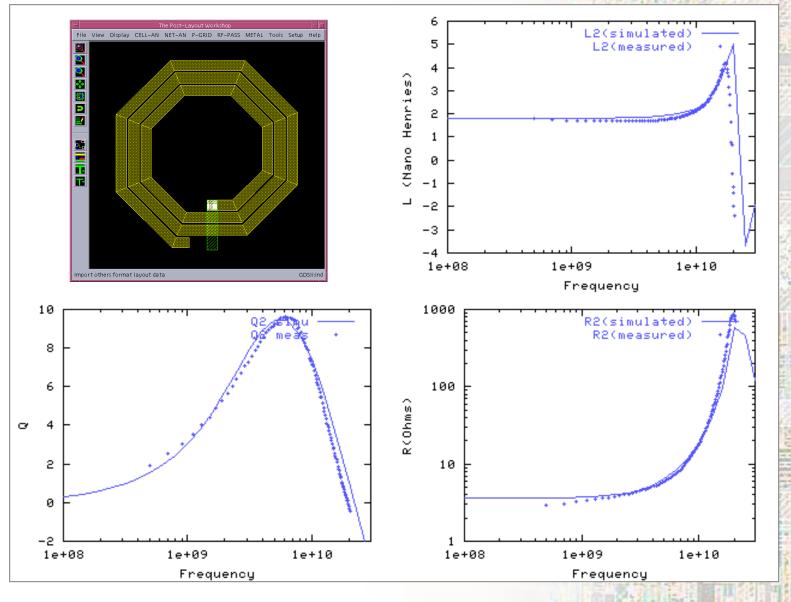
Sprial Extensively Validated Using With Customers and Test Chips



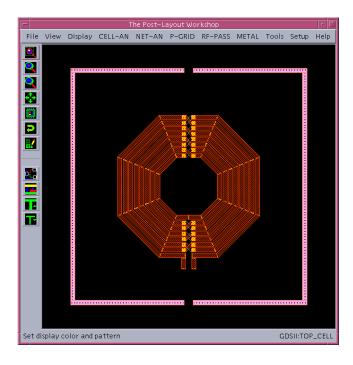
LRQ over Frequency Comparison Against Foundry Measurements (0.13 um Process)



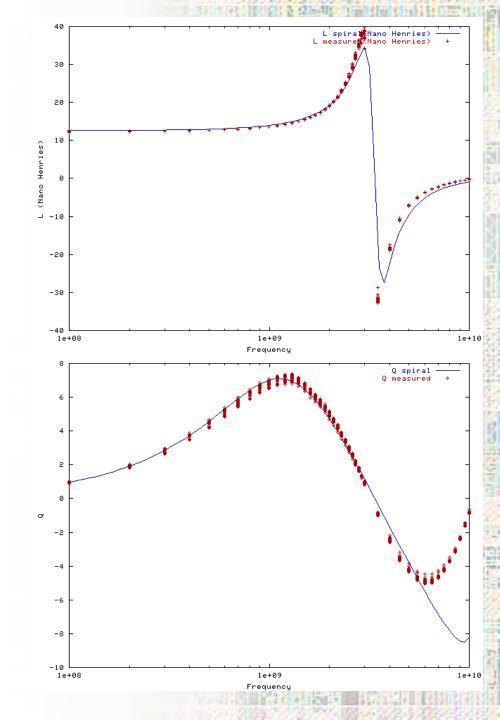
Asian Foundry: Measured Versus Simulated (0.18 um Process)



Measured versus simulated across multiple lots and wafers (0.18 um Process)







Summary

- Fully Automatic Inductor Synthesis
 - Circuit Specific Inductor Optimization
 - Evaluates 1000's of Alternatives in Seconds
 - Easy to Use and Deploy
 - Library Development or Designer's Desktop
- High Accuracy Models Match Silicon
 - Improves Overall Design Performance
- Ready for 90nm & 65nm Technologies

 Slotting and Dummy Metal Fill



Inductance Calculation in Spiral



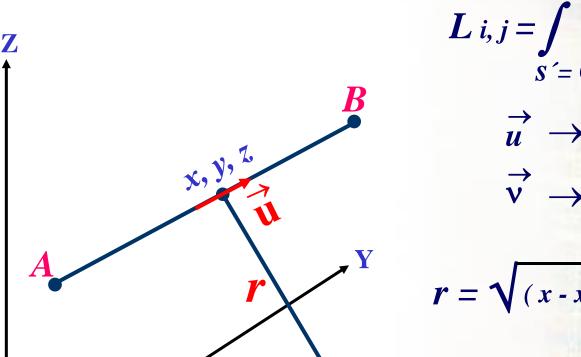
Partial Inductance Approach

Six Self Inductances: L1, L2, L3, L4, L5, L6 **Thirty Mutual Inductances:** Z L1 is coupled to L2, L3, L4, L5, L6 L2 is coupled to L1, L3, L4, L5, L6 L₃ 1.1 <u>⊿ef</u>f **L**5 L6



Neumann Formulation of Mutual Inductance $L i, j = \int_{a}^{D} \int_{a}^{B} \frac{\vec{u} \cdot \vec{v}}{r} ds ds$

x;



 $\overrightarrow{u} \rightarrow$ unit vector along AB

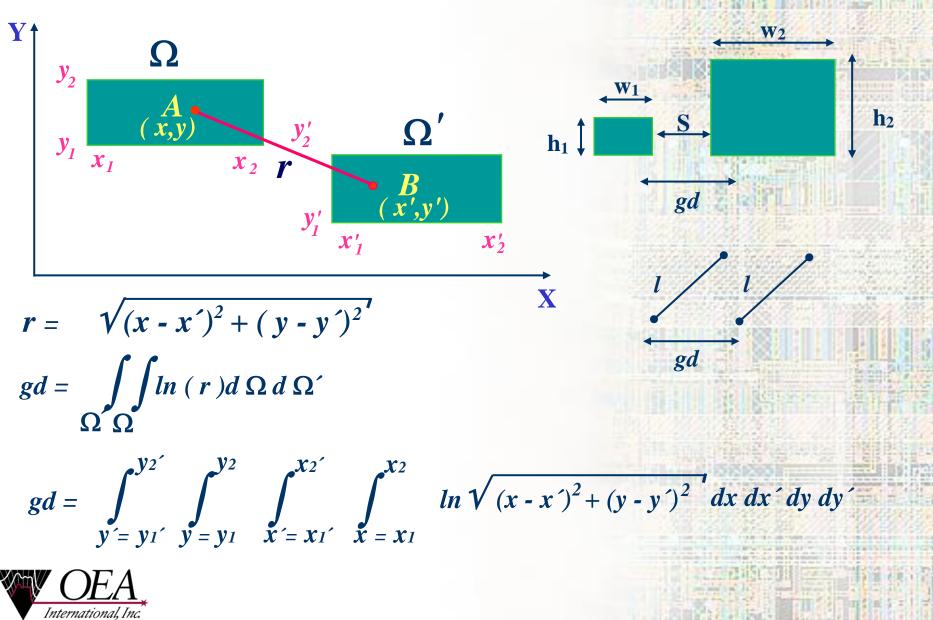
 \overrightarrow{v} \rightarrow unit vector along *CD*

 $r = \sqrt{(x - x')^2 + (y - y')^2 + (z - z')^2}$

 $s' = C \quad s = A$



Geometric Distance Between Objects



Current Distribution Due to Skin and Proximity Effects

2.5 Turn Square Spiral100 um Inner Diameter6.5 um Width4 um Thickness2.1 um Spacing

